Claims

What is claimed:

1. A method of ~~forming~~making a semiconductor device, comprising:

forming a semiconductor wafer ~~having~~including active areas separated from each other by saw street guides;

forming contact pads on a first surface of the semiconductor wafer within the active areas;

forming a trench in the saw street guides;

filling the trench with organic material;

forming first vias in the organic material;

forming second vias through the contact pads on the active areas of the ~~die~~semiconductor wafer;

forming conductive traces between the contact pads and first vias;

depositing conductive material in the first vias and second vias to form first conductive vias and second conductive vias, respectively; and

singulating the semiconductor wafer along the saw street guides to separate the active areas of the semiconductor wafer into die.

2. The method of claim 1, further including:

forming redistribution layers (RDLs) on a second surface of the semiconductor wafer that is opposite the first surface; and

forming ~~repassivation~~insulating layers between the RDLs.

3. The method of claim 1, further comprising:

stacking the die; and

electrically interconnecting the die using the first and

second conductive vias.

4. The method of claim 1, wherein forming first vias in the organic material comprises forming ~~at least one of the~~ a first via~~s~~ directly between a first contact pad disposed in a first active area and a second contact pad disposed in a second active area adjacent to the first active area.

5. The method of claim 4, wherein singulating the semiconductor wafer along the saw street guides comprises dicing through ~~one of the~~a first conductive via~~s~~ ~~that is~~ disposed in the ~~at least one of the~~ first via~~s~~ to form a third conductive via that is electrically connected to the first contact pad by a first conductive trace and a fourth conductive via that is electrically connected to the second contact pad by a second conductive trace.

6. The method of claim 1, wherein forming first vias in the organic material comprises forming two of the first vias side by side and directly between a first contact pad disposed in a first active area and a second contact pad disposed in a second active area adjacent to the first active area.

7. The method of claim 6, wherein singulating the semiconductor wafer ~~along~~ comprises cutting the semiconductor wafer between two of the first conductive vias ~~that are disposed in the two of the first vias~~.

8. A method of ~~fabricating~~ making a semiconductor package, comprising:

forming a semiconductor wafer including die, contact pads disposed on first surfaces of the die, first conductive vias disposed outside a perimeter of the die, second conductive vias disposed in the die, and conductive traces electrically

connecting the first conductive vias to the contact pads;

forming redistribution layers (RDLs) on second surfaces of the die opposite the first surfaces;

forming repassivation layers between the RDLs on the second surface of the die;

singulating the semiconductor wafer to separate the die;

stacking the die; and

electrically interconnecting the stacked die using the first and second conductive vias.

9. The method of claim 8, wherein singulating the semiconductor wafer comprises cutting through at least one of the first conductive vias to form a third conductive via electrically connected to a first contact pad by a first conductive trace and a third conductive via electrically connected to a second contact pad by a second conductive trace.

10. The ~~semiconductor package~~ method of claim 8, wherein two of the first conductive vias are formed side by side and directly between a first contact pad disposed on a first die and a second contact pad disposed on a second die adjacent to the first die.

11. The ~~semiconductor package~~ method of claim 10, wherein singulating the semiconductor wafer comprises cutting along a saw street guide disposed between the two of the first conductive vias.

12. A method of ~~fabricating~~ making a semiconductor package, comprising:

providing a first die ~~having~~including contact pads and first conductive vias formed along a perimeter of the first

die, the first

conductive vias electrically connected to the contact pads by conductive traces, the first die further including second conductive vias formed through an active area of the first die;

providing a second die disposed adjacent to the first die; and

electrically connecting the first and second die using bond wires and the first conductive vias.

13. The method of claim 12, wherein two of the first conductive vias are formed side by side.

14. The method of claim 13, further comprising:

providing a semiconductor wafer including the first die and second die and including a third conductive via formed along the perimeter of the second die; and

singulating the semiconductor wafer along a saw street guide disposed between the ~~two of the~~ first and third conductive vias.

15. A method of ~~fabricating~~ making a semiconductor device, comprising:

providing a semiconductor wafer including a plurality of semiconductor die and contact pads disposed on a first surface of ~~an active area of~~ each semiconductor die~~, the semiconductor wafer further including a saw street guide between each die~~;

forming a trench ~~in the saw street guide~~ completely through the semiconductor wafer;

~~filling the trench with~~ depositing an organic material in the trench;

forming first ~~conductive~~ vias ~~that are surrounded by~~ in the organic material;

forming second ~~conductive~~ vias in ~~the active area of~~ the

semiconductor die; ~~and~~

depositing a conductive material in the first vias and second vias to form first conductive vias and second conductive vias; and

~~connecting~~ forming a plurality of conductive traces to electrically connect the contact pads and the first conductive vias ~~using conductive traces~~.

16. The method of claim 15, further including:

forming redistribution layers (RDLs) on a second surface of the die opposite the first surface; and

forming ~~repassivation~~ insulatinglayers between the RDLs on the second surface of the die.

17. The method of claim 15, further comprising:

stacking the die;and

electrically interconnecting the stacked die using the first and second conductive vias.

18. The method of claim 15, wherein at least one of the first conductive vias is formed directly between a first contact pad disposed on a first die and a second contact pad disposed on a second die that is adjacent to the first die.

19. The method of claim 18, further comprising singulating the semiconductor wafer through the at least one of the first conductive vias to form a third conductive via that is electrically connected to the first contact pad by a first conductive trace and to form a fourth conductive via that is electrically connected to the second contact pad by a second conductive trace.

20. The method of claim 15, wherein two of the first conductive vias are formed side by side and directly between a first contact pad disposed on a first die and a second contact pad disposed on a second die that is adjacent to the first die.

21. The method of claim 20, further comprising singulating the semiconductor wafer along a saw street guide disposed between the two of the first conductive vias.

22. The method of claim ~~15~~16, further comprising forming conductive bumps that are electrically connected to the RDLs.

23. A method of making a semiconductor device, comprising:
providing a plurality of semiconductor die;
forming a trench to completely sever the semiconductor die;
depositing an organic material in the trench between the severed semiconductor die;
forming a first conductive via through the organic material; and
singulating the semiconductor die through the first conductive via to form a second and third conductive via.

24. The method of claim 23, further including:
forming a contact pad over the semiconductor die; and
forming a conductive trace over the semiconductor die to electrically connect the contact pad and second conductive via.

25. The method of claim 23, further including:
stacking the plurality of semiconductor die; and
electrically connecting the stacked semiconductor die through the second and third conductive vias.

26. The method of claim 23, wherein the first conductive via is formed directly between a first contact pad of a first semiconductor die and a second contact pad of a second semiconductor die.

27. A method of making a semiconductor device, comprising:
providing a first semiconductor die;
forming a first via outside a footprint of the first semiconductor die;
forming a second via in the first semiconductor die; and

depositing a conductive material in the first via and second via to form a first conductive via and a second conductive via.

28. The method of claim 27, further including:

forming a contact pad on a first surface of the first semiconductor die;

forming redistribution layers (RDLs) on a second surface of the die opposite the first surface; and

forming insulating layers between the RDLs on the second surface of the die.

29. The method of claim 27, further comprising:

stacking the die; and

electrically interconnecting the stacked die using the first and second conductive via.

30. The method of claim 27, wherein the first conductive via is formed directly between a first contact pad disposed on the first semiconductor die and a second contact pad disposed on a second semiconductor die adjacent to the first die.