

Description

The invention relates to power supply system and, preferably, to a drive circuitry of a push-pull stage in a DC-to-DC converter power supply of, for example, a television apparatus.

In some television power supply applications, such as in a battery operated television system, it may be desirable to convert an input source of direct voltage, such as a battery, to a supply of direct output voltage that is at, for example, a higher voltage level. This is conventionally achieved using a circuit known as a DC-to-DC converter. In such a converter the available input DC voltage is chopped to generate an AC voltage which can, in turn, be stepped up or down to a desired voltage level using a transformer. The AC voltage is rectified and filtered to obtain a DC output voltage that is coupled to energize various stages in the television system.

Chopping of the input DC voltage may be done in a push-pull manner by transistor switches that are coupled to a corresponding pair of terminals of a primary winding of the transformer. The input DC voltage is coupled to a terminal located intermediate the pair of terminals. The transistor switches are alternately turned on and off by control signals at corresponding control electrodes of the transistor switches to form the corresponding alternately changing polarities of the AC voltage. The AC voltage is then transformer coupled and rectified to form the output voltage.

It has been recognized that it is desirable to prevent the transistor switches from being simultaneously conductive, since simultaneous conduction produces very high currents. It has been also recognized that the conduction time of each transistor switch may be a function of various circuit parameters which may vary. It is known to inhibit simultaneous conduction in a manner that automatically takes into account the pertinent parameters that affect switching delays. Such parameters may be different for different transistor switches and may be affected by environmental conditions such as temperature.

JP-A-56-103971 discloses a circuit comprising two bipolar transistors operated in push-pull manner. In order to prevent simultaneous conduction of the two transistors, each transistor has a detector which detects the base-emitter voltage thereof. The detected base-emitter voltage of one transistor is sent, via a delay circuit to an AND gate. The AND gate allows a drive signal to be applied to the other transistor only when the detected and delayed base-emitter voltage indicates the one transistor is non-conductive. The delay needs to be chosen for worst-case conditions resulting in excessive dead times.

It may be desirable to control the conduction time of the transistor switches using control signals that are nonoverlapping in a manner that, advantageously, reduces the dead time that occurs when neither of the transistor switches conducts. Reducing the dead time, advantageously, increases the power efficiency. Reducing the dead time also, advantageously, reduces the amplitude of, for example, the second harmonic relative to the fundamental frequency of the AC voltage. Reduced harmonics reduces the need for filtering out of AC components from the DC output voltage. It may be desirable to dynamically reduce the dead time in a manner that takes into account the values of the pertinent parameters of, for example, the transistor switches, which parameters may vary and affect the switching conduction and delay times.

According to the present invention, there is provided a power supply apparatus having an output stage that operates in a push-pull manner, comprising: a load having first and second terminals; a source of an input supply voltage coupled (through T_1) to said load; a first transistor of said output stage having corresponding first and second main current conducting electrodes that form a main current path, said first main current conducting electrode of said first transistor being coupled (through T_1) to said first terminal of said load; a second transistor of said output stage having corresponding first and second main current conducting electrodes, said first main current conducting electrode of said second transistor being coupled (through T_1) to said second terminal of said load; a source of first and second switching signals coupled to corresponding control electrodes of said first and second transistors such that said first signal determines in a given period thereof a first instant when said first transistor begins changing from being conductive to being nonconductive and said second signal determines in said given period when said second transistor becomes conductive so as to cause said push-pull manner operation by said first and second transistors; characterized by means responsive to a third signal that is developed at the control electrode of the conductive one of said first and second transistors and that is indicative of a magnitude of a current that flows between said main current conducting electrodes of said conductive transistor for generating a fourth signal that is coupled to the control electrode of the non-conductive one of said first and second transistors to prevent said non-conductive transistor from conducting in said given period while the magnitude of said current that flows in said conductive transistor is greater than a first predetermined level, thereby avoiding simultaneous conduction of said first and second transistors, wherein said third signal at said control electrode of said

conductive transistor is applied to said fourth signal generating means via a signal path that does not include the main current path of said conductive transistor.

The third signal may be developed as a result of capacitive coupling of a signal from the main current conducting electrode of, for example, the first transistor, that may be of the MOSFET type, to the control electrode of the first transistor via, for example, an inter-electrode capacitance. The inter-electrode capacitance coupling occurs mainly during a transition time from conduction to nonconduction in the first transistor because of input capacitance multiplication phenomenon, known as the Miller effect or Miller capacitance.

In the Drawing:

FIGURE 1 illustrates a drive circuit, embodying aspects of the invention, of a push-pull stage in a DC-to-DC converter power supply; and

FIGURES 2a-2c illustrate waveforms useful in explaining the operation of the circuit of FIGURE 1.

FIGURE 1 illustrates a battery operated television apparatus power supply. The power supply includes an oscillator 50 that generates signals 50a and 50b of substantially opposite phases, at, for example, approximately 70 kHz that are coupled via corresponding driver stages 51 and 52 to form corresponding signals V_1 and V_2 . Signals V_1 and V_2 each have a square waveform of 50% duty cycle, and are of opposite phases. All the transitions in signals V_1 and V_2 occur substantially simultaneously. Signals V_1 and V_2 are coupled via corresponding current limiting and sampling resistors R_{11} and R_{12} to corresponding gate electrodes of MOSFET power transistors Q_4 and Q_5 . Consequently, signals V_3 and V_4 that are at substantially opposite phases are formed at the gates of transistors Q_4 and Q_5 , respectively. The waveforms of signals V_3 and V_4 , are waveshaped, embodying an aspect of the invention, in a manner that is described in detail later on.

A pair of corresponding main current conducting electrodes Q_{4a} and Q_{5a} of transistors Q_4 and Q_5 , respectively, are each coupled to ground. A second pair of corresponding main current conducting electrodes of transistors Q_4 and Q_5 are coupled to corresponding end terminals 58 and 59 of a primary winding T_{1P} of a step-up transformer T_1 . A terminal 53 of primary winding T_{1P} of transformer T_1 , coupled intermediate terminals 58 and 59, is coupled to a battery generated DC voltage V_5 that is referenced to ground. As a result of the push-pull operation of transistors Q_4 and Q_5 , an AC voltage V_6 is developed across a secondary winding T_{1S} of transformer T_1 . AC voltage V_6 is coupled via a conventional voltage doubler 56 to a load 57 for generating a DC output voltage that is, for

example, substantially higher than battery voltage V_5 and that is developed between a terminal 60 of load 57 and a terminal 54. Load 57 may represent the equivalent load formed by a television circuitry, not shown in the FIGURES, that is energized by the power supply of FIGURE 1.

FIGURES 2a-2c illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1. Similar numbers and symbols in FIGURES 1 and 2a-2c indicate similar items of functions.

A waveshaping arrangement 100 of FIGURE 1, embodying an aspect of the invention, receives signals V_1 and V_2 and generate signals V_3 and V_4 , that are coupled to the gate electrodes of transistors Q_4 and Q_5 , respectively. Arrangement 100, advantageously, automatically prevents simultaneous conduction of transistors Q_4 and Q_5 .

Prior to time t_1 of FIGURE 2a, transistor Q_4 of FIGURE 1 is maintained nonconductive by signal V_1 that is zero and transistor Q_5 is maintained conductive by signal V_2 that is 10 volts. At time t_1 of FIGURE 2a, signal V_1 changes rapidly from substantially zero volts to 10 volts. Simultaneously, signal V_2 changes from 10 volts to zero volts. As a result of signal V_2 changing to zero volts, signal V_4 of FIGURE 2b begins changing in a fast transition from a value of that is approximately 10 volts toward a lower value. At time t_2 , when signal V_4 has reached a level of approximately 5 volts, transistor Q_5 of FIGURE 1 begins operating in its active region that causes the impedance between its main current conducting electrodes to increase and the voltage at terminal 59 to become a positive high voltage. This increase in the voltage at terminal 59 is capacitively coupled back to the control, or gate electrode of transistor Q_5 through an interelectrode capacitance C_{IE} that is shown in FIGURE 1 by a dashed line. The result is an equivalent large input capacitance at the gate of transistor Q_5 . The large input capacitance is referred to as the Miller capacitance.

Each of transistors Q_4 and Q_5 of FIGURE 1 employs, illustratively, a MOSFET transistor of the type BUZ 72A that has a gate input capacitance of 440 pF at $V_{GS} = 0V$ and at $V_{DS} = 25V$. During the transition time from conduction to nonconduction of transistor Q_5 , for example, the input capacitance is increased to 25,000 pF, as a result of the Miller effect. The Miller capacitance that is large causes signal V_4 of FIGURE 2b to remain at approximately 5 volts for a relatively long duration that is from time t_2 and until time t_3 . Consequently, transistor Q_5 of FIGURE 1 remains conductive during the interval t_1 - t_3 .

Embodying an aspect of the invention, signal V_4 is coupled via a voltage divider that includes a series arrangement of resistors R_3 , R_4 and R_5 to develop a voltage across resistor R_5 that is coup-

led between the base and emitter electrodes of a transistor Q_1 . The collector electrode of transistor Q_1 is coupled to the gate electrode of transistor Q_4 and to a corresponding terminal of resistor R_{11} . Thus, resistor R_{11} and transistor Q_1 , operating as a controllable impedance, function as a voltage attenuator that attenuates the level of signal V_3 as long as transistor Q_5 and, hence, as long as transistor Q_1 , remain conductive. As long as signal V_4 is above a predetermined level that is indicative of transistor Q_5 being conductive, the voltage attenuator that includes resistor R_{11} and transistor Q_1 automatically holds down the level of signal V_3 to prevent signal V_3 from exceeding the threshold level of transistor Q_4 . Thus, advantageously, the attenuator inhibits conduction in transistor Q_4 until the input capacitance of transistor Q_5 is discharged and transistor Q_5 ceases conduction.

Embodying another aspect of the invention, the control terminal, or the base electrode, of transistor Q_1 is coupled to the gate of transistor Q_5 in a control signal path that does not include the drain electrode main current path of transistor Q_5 . Thus, sensing of the current that flows in transistor Q_5 is performed, advantageously, without the need for a current sensing resistor in the current path that includes the source and drain electrodes of transistor Q_5 . Therefore, the current sensing arrangement, advantageously, does not affect any of the peak current in, for example, transistor Q_5 and the impedance that is coupled in series with primary winding T_{1P} .

A diode D_8 having an anode that is coupled at a junction between resistors R_3 and R_4 and having a cathode that is coupled to the collector of transistor Q_1 forms a negative feedback arrangement that, advantageously, keeps transistor Q_1 out of being in saturation. The feedback arrangement that includes diode D_8 limits the level of signal V_3 of FIGURE 2b, prior to time t_3 , to, approximately, 2 volts, which is sufficiently low to prevent conduction of transistor Q_4 . After time t_3 of FIGURE 2b, signal V_4 ramps down to a level that is below 4 volts that causes the current between the main current conducting electrodes of transistor Q_5 of FIGURE 1 to decrease rapidly to zero, resulting in transistor Q_5 becoming nonconductive. After time t_3 , when the level of signal V_4 of FIGURE 2b ramps downward, transistor Q_1 of FIGURE 1 is, advantageously, quickly turned off because it is not in saturation. The fast turn-off of transistor Q_1 enables transistor Q_4 to quickly turn on to its saturation state after time t_3 of FIGURE 2b. Thus, the saturation state of transistor Q_4 occurs only after transistor Q_5 becomes nonconductive.

During the interval t'_1 - t'_3 of FIGURES 2a-2c, when transistor Q_4 of FIGURE 1 switches from conduction to nonconduction, transistor Q_2 controls

the waveform shape of signal V_4 in a similar manner, as described above, so as to inhibit overlapping conduction of transistors Q_4 and Q_5 , as illustrated in FIGURE 2b during the interval t'_1 - t'_3 . Thus, simultaneous conduction of transistors Q_4 and Q_5 is advantageously, prevented. Furthermore, because waveshaping arrangement 100 responds automatically to the levels of signals V_4 and V_3 , variation of circuit parameters such as, for example, the Miller capacitance, advantageously, will not defeat the operation of arrangement 100 that dynamically waveshapes signals V_3 and V_4 .

As explained before, arrangement 100 prevents any significant simultaneous conduction in transistors Q_4 and Q_5 while, advantageously, maximizing the duration of conduction of transistors Q_4 and Q_5 . By maximizing the duration of conduction time, the peak current that flows in each of transistors Q_4 and Q_5 , that corresponds with a given level of a load current at secondary winding T_{1S} , may be, advantageously, reduced relative to that required when less than maximum conduction time occurs. Therefore, less stringent peak current requirements are imposed on transistors Q_4 and Q_5 .

FIGURE 2c illustrates the waveform of a current i_1 that flows into terminal 53 of primary winding T_{1P} of transformer T_1 of FIGURE 1. Current i_1 of FIGURE 2c flows, prior to time t_3 , through the lower portion of primary winding T_{1P} of transformer T_1 of FIGURE 1 between terminals 53 and 58 and through transistor Q_5 . During the interval t_3 - t'_3 of FIGURE 2c, current i_1 of FIGURE 1 flows through the upper portion of primary winding T_{1P} between terminals 53 and 59. Note that during switching intervals t_1 - t_3 and t'_1 - t'_3 of FIGURE 2c, current i_1 is interrupted, as shown by the negative going notches, for only a short time. Therefore, advantageously, both current i_1 and the resistive losses are small. The positive peaks of current i_1 of FIGURE 2c, appearing just after times t_3 and t'_3 , respectively, are caused by the operation of voltage doubler 56 that charges capacitors C_8 and C_{11} .

It should be understood that, advantageously, the operation frequency may be increased without causing a significant change in the peak of current i_1 . This is so because, in each cycle, the dead times that occurs at, for example, times t_3 and t'_3 of FIGURE 2c, when neither transistor Q_4 nor Q_5 of FIGURE 1 is conductive, are, each, substantially small relative to the conduction intervals.

Arrangement 100 of FIGURE 1 employs general purpose NPN transistors with an f_t of 200 MHz. It should be understood that, for example, fast small signal MOSFET transistors may be employed in place of transistors Q_1 and Q_2 .

Claims

1. A power supply apparatus having an output stage that operates in a push-pull manner, comprising:

a load (57) having first (60) and second (54) terminals;

a source of an input supply voltage (24V) coupled (through T_1) to said load (57);

a first transistor (Q_4) of said output stage having corresponding first and second main current conducting electrodes that form a main current path, said first main current conducting electrode of said first transistor being coupled (through T_1) to said first terminal (60) of said load (57);

a second transistor (Q_5) of said output stage having corresponding first and second main current conducting electrodes, said first main current conducting electrode of said second transistor being coupled (through T_1) to said second terminal (54) of said load (57);

a source (50) of first (V_1) and second (V_2) switching signals coupled to corresponding control electrodes of said first (Q_4) and second (Q_5) transistors such that said first signal (V_1) determines in a given period thereof a first instant when said first transistor (Q_4) begins changing from being conductive to being non-conductive and said second signal (V_2) determines in said given period when said second transistor (Q_5) becomes conductive so as to cause said push-pull manner operation by said first (Q_4) and second (Q_5) transistors; characterized by

means (Q_1, Q_2) responsive to a third signal that is developed at the control electrode of the conductive one of said first and second transistors (Q_4, Q_5) and that is indicative of a magnitude of a current that flows between said main current conducting electrodes of said conductive transistor for generating a fourth signal that is coupled to the control electrode of the non-conductive one of said first and second transistors (Q_4, Q_5) to prevent said non-conductive transistor from conducting in said given period while the magnitude of said current that flows in said conductive transistor is greater than a first predetermined level, thereby avoiding simultaneous conduction of said first (Q_4) and second (Q_5) transistors, wherein said third signal at said control electrode of said conductive transistor is applied to said fourth signal generating means via a signal path that does not include the main current path of said conductive transistor.

2. An apparatus according to Claim 1 characterized in that said first (V_1) and second (V_2) switching signals are substantially anti-phased signals such that all the transition times in both occur simultaneously.

3. An apparatus according to Claim 1 characterized in that said first transistor (Q_4) comprises a MOSFET power transistor.

4. An apparatus according to Claim 1 characterized in that, during an interval that occurs when said first transistor (Q_4) changes from being conductive to being nonconductive, a Miller capacitance couples one of said first and second main current conducting electrodes to said control electrode of said first transistor (Q_4) that causes a delay in a transition of said third signal (V_3) at said control electrode thereof.

5. An apparatus according to Claim 1 characterized in that said load (57) is coupled through a transformer (T_1) and wherein an output supply voltage (V_6) is developed at a secondary winding (T_{1S}) of said transformer (T_1).

6. An apparatus according to Claim 1 characterized in that said fourth signal generating means comprises, a first controllable attenuator (Q_2, R_{12}) responsive to said third signal (V_3) and coupled between a terminal (5) that develops said second switching signal (V_2) and said control electrode of said second transistor (Q_5) for coupling said fourth signal (V_4) that is representative of a portion of said second switching signal (V_2) to said control electrode of said second transistor (Q_5) such that as long as a difference signal developed between said control and said second main current conducting electrodes of said first transistor (Q_4) is larger than a predetermined value that is indicative of a current level in said first transistor (Q_4) being greater than said predetermined level, said first controllable attenuator (Q_2, R_{12}) attenuates said signal portion that is developed at said control electrode of said second transistor (Q_5) for delaying conduction in said second transistor.

7. An apparatus according to Claim 6, characterized in that said first controllable attenuator comprises a voltage divider (R_6, R_7, R_8) coupled to said control electrode of said first transistor (Q_4), and a third transistor (Q_2) having a main current conducting electrode that is coupled to said control electrode of said second transistor (Q_5) and having a control electrode that is coupled to an output terminal of said voltage



divider, said third transistor (Q_2) forming a controllable shunting impedance at said control electrode of said second transistor (Q_5) that varies in accordance with a signal that is developed at said output terminal of said voltage divider and that is proportional to said third signal (V_3) developed at said control electrode of said first transistor (Q_4) so as to attenuate said signal that is developed at said control electrode of said second transistor (Q_5) as long as said first transistor is conductive, and when said first transistor becomes nonconductive, said controllable shunting impedance (Q_2, R_{11}) changes in a manner that causes said second transistor (Q_5) to become conductive.

8. An apparatus according to Claim 7 characterized in that said impedance that is formed by said third transistor (Q_2) assumes a substantially lower value as long as said third signal (V_3) at said control electrode of said first transistor (Q_4) is greater than a predetermined value.

9. An apparatus according to Claim 7 characterized in that said voltage divider comprises a resistive network (R_6, R_7, R_8) and wherein said first controllable attenuator further comprises feedback means (D_3) coupled between said third transistor (Q_2) and a second output terminal of said resistive network (R_6, R_7, R_8) for generating a signal that prevents said third transistor (Q_2) from being in saturation, so as to render said second transistor (Q_5) conductive immediately after said first transistor (Q_4) becomes nonconductive.

10. An apparatus according to Claim 6 characterized in that said first controllable attenuator comprises a resistor (R_{12}) coupled between a terminal (5) where said second switching signal (V_2) is developed and said control electrode of said second transistor (Q_5), and a third transistor (Q_2) having a main current conducting electrode that is coupled at a junction between said resistor (R_{12}) and said control electrode of said second transistor (Q_5) such that said resistor (R_{12}) and said third transistor (Q_2) attenuate a portion of said second switching signal (V_2) that is coupled to said control electrode of said second transistor (Q_5) as long as said first transistor (Q_4) is conductive, and when said first transistor (Q_4) becomes nonconductive a greater portion of said second switching signal (V_2) is coupled to said control electrode of said second transistor (Q_5).

11. An apparatus according to Claim 10 characterized by a fourth transistor (Q_1) having a main current conducting electrode that is coupled to said control electrode of said first transistor (Q_4) and having a control electrode that is coupled to said control electrode of said second transistor (Q_5), said fourth transistor (Q_1) attenuating said third signal (V_3) that is developed at said control electrode of said first transistor (Q_4) to prevent simultaneous conduction in both said first (Q_4) and second (Q_5) transistors.

Patentansprüche

1. Stromversorgungsvorrichtung mit einer Ausgangsstufe, die im Gegentakt arbeitet, mit einer Last (57), die erste (60) und zweite (54) Klemmen hat;

mit einer Quelle für eine Eingangs-Versorgungsspannung (24V), die (über T_1) mit der Last (57) verbunden ist;

mit einem ersten Transistor (Q_4) der Ausgangsstufe, der entsprechende erste und zweite haupt-stromführende Elektroden hat, die einen Hauptstromweg bilden, wobei die erste haupt-stromführende Elektrode des ersten Transistors (über T_1) mit der ersten Klemme (60) der Last (57) verbunden ist;

mit einem zweiten Transistor (Q_5) der Ausgangsstufe, der entsprechende erste und zweite haupt-stromführende Elektroden hat, wobei die erste haupt-stromführende Elektrode des zweiten Transistors (über T_1) mit der zweiten Klemme (54) der Last (57) verbunden ist;

mit einer Quelle (50) von ersten (V_1) und zweiten (V_2) Schaltsignalen, die entsprechenden Steuerelektroden des ersten (Q_4) und des zweiten (Q_5) Transistors zugeführt werden, so daß das erste Signal (V_1) in einer gegebenen Periode einen ersten Augenblick bestimmt, wenn der erste Transistor (Q_4) beginnt, sich vom leitenden Zustand in einen nicht-leitenden Zustand zu ändern, und das zweite Signal (V_2) in der gegebenen Periode bestimmt, wenn der zweite Transistor (Q_5) leitend wird, um dadurch den Gegentaktbetrieb des ersten (Q_4) und zweiten (Q_5) Transistors zu bewirken; gekennzeichnet durch

Mittel (Q_1, Q_2), die auf ein drittes Signal ansprechen, das an der Steuerelektrode des von den beiden Transistoren (Q_4, Q_5) leitenden Transistors entwickelt wird, und das ein Maß für die Größe eines Stromes ist, der zwischen den haupt-stromführenden Elektroden des leitenden Transistors fließt, um ein viertes Signal zu erzeugen, das der Steuerelektrode des von den beiden Transistoren (Q_4, Q_5) nicht leitenden



den Transistors zugeführt wird, um zu verhindern, daß der nicht leitende Transistor in der gegebenen Periode leitend wird, wenn die Größe des in dem leitenden Transistor fließenden Stroms größer ist als ein erster vorgegebener Pegel, und um dadurch das gleichzeitige Leitendwerden des ersten (Q_4) und zweiten (Q_5) Transistors zu vermeiden, wobei das dritte Signal an der Steuerelektrode des leitenden Transistors den vierten signalerzeugenden Mitteln über einen Signalweg zugeführt wird, der nicht den Hauptstromweg des leitenden Transistors einschließt.

2. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß das erste (V_1) und das zweite (V_2) Schaltsignal im wesentlichen gegenphasige Signale sind, so daß alle Übergangszeiten in beiden Signalen gleichzeitig auftreten.
3. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß der erste Transistor ein MOFSET-Leistungstransistor ist.
4. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß während eines Intervalls, das auftritt, wenn der erste Transistor (Q_4) vom leitfähigen Zustand in den nicht-leitfähigen Zustand übergeht, eine Miller-Kapazität eine der ersten und zweiten haupt-stromführenden Elektroden mit der Steuerelektrode des ersten Transistors (Q_4) verbindet, der eine Verzögerung in einem Übergang des dritten Signals (V_3) an seiner Steuerelektrode bewirkt.
5. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß die Last (57) über einen Transformator (T_1) angeschlossen ist, und daß eine Ausgangs-Versorgungsspannung (V_6) an einer Sekundärwicklung (T_{1S}) des Transformators (T_1) entwickelt wird.
6. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß die das vierte Signal erzeugenden Mittel ein erstes steuerbares Dämpfungsglied (Q_2 , R_{12}) enthalten, das auf das dritte Signal (V_3) anspricht und zwischen einer Klemme (5), die das zweite Schaltsignal (V_2) erzeugt und der Steuerelektrode des zweiten Transistors (Q_5) liegt, um das vierte Signal (V_4), das ein Maß für einen Teil des zweiten Schaltsignals (V_2) ist, der zweiten Elektrode des zweiten Transistors (Q_5) zuzuführen, so daß, solange ein zwischen der Steuerelektrode und der zweiten haupt-stromführenden Elektrode des ersten Transistors (Q_4) entwickeltes Differenzsignal größer ist als ein vorgegebener

Wert, der anzeigt, daß ein Strompegel in dem ersten Transistor (Q_4) größer als der vorgegebene Pegel ist, wobei das erste steuerbare Dämpfungsglied (Q_2 , R_{12}) den an der Steuerelektrode des zweiten Transistors (Q_5) entwickelten Signalanteil dämpft, um die Leitfähigkeit in dem zweiten Transistor zu verzögern.

7. Vorrichtung nach Anspruch 6, dadurch gekennzeichnet, daß das erste steuerbare Dämpfungsglied einen Spannungsteiler (R_6 , R_7 , R_8) enthält, der mit der Steuerelektrode des ersten Transistors (Q_4) verbunden ist, und daß ein dritter Transistor (Q_2) vorgesehen ist, der eine haupt-stromführende Elektrode, die mit der Steuerelektrode des zweiten Transistors (Q_5) verbunden ist und eine mit einer Ausgangsklemme des Spannungsteilers verbundene Steuerelektrode aufweist, daß der dritte Transistor (Q_2) eine steuerbare Nebenschlußimpedanz an der Steuerelektrode des zweiten Transistors (Q_5) bildet, die sich gemäß einem Signal ändert, das an der Ausgangsklemme des Spannungsteilers entwickelt wird, und das proportional zu dem an der Steuerelektrode des ersten Transistors (Q_4) entwickelten dritten Signals (V_3) ist, um so das Signal zu dämpfen, das an der Steuerelektrode des zweiten Transistors (Q_5) entwickelt wird, solange der erste Transistor leitend ist und daß bei Nicht-Leitendwerden des ersten Transistors die steuerbare Nebenschlußimpedanz (Q_2 , R_{11}) sich so ändert, daß der zweite Transistor (Q_5) leitend wird.
8. Vorrichtung nach Anspruch 7, dadurch gekennzeichnet, daß die von dem dritten Transistor (Q_2) gebildete Impedanz einen nennenswert niedrigeren Wert annimmt, solange das dritte Signal (V_3) an der Steuerelektrode des ersten Transistors (Q_4) größer ist als ein vorgegebener Wert.
9. Vorrichtung nach Anspruch 7, dadurch gekennzeichnet, daß der Spannungsteiler aus einem Widerstandsnetzwerk (R_6 , R_7 , R_8) besteht, und daß das erste steuerbare Dämpfungsglied ferner Rückkopplungsmittel (D_3) enthält, die zwischen dem dritten Transistor (Q_2) und einer zweiten Ausgangsklemme des Widerstandsnetzwerks (R_6 , R_7 , R_8) liegen, um ein Signal zu erzeugen, das verhindert, daß der dritte Transistor (Q_2) in die Sättigung gelangt, um so den zweiten Transistor (Q_5) leitend zu machen, unmittelbar nachdem der erste Transistor (Q_4) nichtleitend wird.



10. Vorrichtung nach Anspruch 6, dadurch gekennzeichnet, daß das erste steuerbare Dämpfungsglied einen Widerstand (R_{12}) enthält, der zwischen einer Klemme (5), an der das zweite Schaltsignal (V_2) entwickelt wird, und der Steuerelektrode des zweiten Transistors (Q_5) liegt, und daß ein dritter Transistor (Q_2) vorgesehen ist, der eine haupt-stromführende Elektrode hat, die mit einer Verbindung zwischen dem Widerstand (R_{12}) der Steuerelektrode des zweiten Transistors (Q_5) so verbunden ist, daß der Widerstand (R_{12}) und der dritte Transistor (Q_2) einen Teil des zweiten Schaltsignals (V_2) das der Steuerelektrode des zweiten Transistors (Q_5) zugeführt wird, dämpfen, solange der erste Transistor (Q_4) leitend ist, und daß bei Nicht-Leitendwerden des ersten Transistors (Q_4) ein größerer Teil des zweiten Schaltsignals (V_2) der Steuerelektrode des zweiten Transistors (Q_5) zugeführt wird.

11. Vorrichtung nach Anspruch 10, gekennzeichnet durch einen vierten Transistor (Q_1), der eine haupt-stromführende Elektrode hat, die mit der Steuerelektrode des ersten Transistors (Q_4) verbunden ist, und der eine Steuerelektrode hat, die mit der Steuerelektrode des zweiten Transistors (Q_5) verbunden ist, und daß der vierte Transistor (Q_1) das dritte Signal (V_3) dämpft, das an der Steuerelektrode des ersten Transistors (Q_4) entwickelt wird, um eine gleichzeitige Leitfähigkeit im ersten (Q_4) und zweiten Transistor (Q_5) zu verhindern.

Revendications

1. Dispositif d'alimentation de puissance comportant un étage de sortie qui fonctionne selon un mode push-pull comprenant :

- une charge (57) ayant une première (60) et une seconde (54) bornes ;
- une source de tension d'alimentation d'entrée (24V) couplée (par T_1) à ladite charge (57) ;
- un premier transistor (Q_4) dudit étage de sortie ayant des première et seconde électrodes T correspondantes conductrices de courant principal qui forment une trajectoire de courant principal, ladite électrode conductrice de courant principal dudit premier transistor étant couplée (par T_1) à ladite première borne (60) de ladite charge (57) ;
- un second transistor (Q_5) dudit étage de sortie ayant des première et seconde électrodes correspondantes conductrices de courant principal, ladite première électrode conductrice de courant principal

pal du second transistor étant couplée (par T_1) à ladite seconde borne (54) de ladite charge (57) ;

- une source (50) de premier (V_1) et de second (V_2) signaux de commutation, couplée aux électrodes correspondantes de commande dudit premier (Q_4) et second (Q_5) transistors, de manière que ledit premier signal (V_1) détermine dans une période donnée de ce signal, un premier instant durant lequel ledit premier transistor (Q_4) commence à changer de l'état conducteur vers l'état non-conducteur et ledit second signal (V_2) détermine, dans ladite période donnée, lorsque ledit second transistor (Q_5) devient conducteur, afin d'obtenir ledit mode de fonctionnement push-pull par lesdits premier (Q_4) et second (Q_5) transistors ;

caractérisé par des moyens (Q_1 , Q_2) agissant en réponse à un troisième signal qui est développé sur l'électrode de commande de celui des premier et second transistors (Q_4 , Q_5) qui est conducteur, et qui constituent une indication d'une amplitude d'un courant qui circule entre lesdites électrodes conductrices de courant principal dudit transistor conducteur pour générer un quatrième signal qui est couplé à l'électrode de commande de celui des premier et second transistors (Q_4 , Q_5) qui est non-conducteur, pour empêcher ledit transistor non-conducteur de conduire pendant ladite période donnée, alors que l'amplitude dudit courant qui circule dans ledit transistor conducteur est plus grande qu'un premier niveau prédéterminé, ce qui évite ainsi une conduction simultanée desdits premier (Q_4) et second (Q_5) transistors, ledit troisième signal sur ladite électrode de commande du transistor conducteur étant appliqué auxdits moyens générant le quatrième signal, par l'intermédiaire d'une trajectoire de signal qui n'inclue pas la trajectoire de courant principal dudit transistor conducteur.

2. Dispositif selon la revendication 1, caractérisé en ce que lesdits premier (V_1) et second (V_2) signaux de commutation sont essentiellement des signaux anti-phase tels que toutes les périodes de transition se produisent simultanément dans les deux signaux.

3. Dispositif selon la revendication 1 caractérisé en ce que ledit premier transistor (Q_4) com-



prend un transistor de puissance MOS FET.

4. Dispositif selon la revendication 1 caractérisé en ce que, pendant l'intervalle qui se situe lorsque le premier transistor (Q_4) change de l'état conducteur à l'état non conducteur, une capacité Miller couple l'une desdites première et seconde électrodes conduisant le courant principal, à ladite électrode de commande dudit premier transistor (Q_4), ce qui introduit un retard dans une transition dudit troisième signal (V_3), sur ladite électrode de commande. 5 10
5. Dispositif selon la revendication 1, caractérisé en ce que ladite charge (57) est couplée à l'aide d'un transformateur (T_1) et dans lequel une tension d'alimentation de sortie (V_6) est développée sur un enroulement secondaire (T_{15}) dudit transformateur (T_1). 15 20
6. Dispositif selon la revendication 1 caractérisé en ce que lesdits moyens générant le quatrième signal comprennent, un premier atténuateur pouvant être commandé (Q_2 , R_{12}) agissant en réponse audit troisième signal (V_3) et qui est couplé entre une borne (5) qui développe ledit second signal de commutation (V_2) et ladite électrode de commande dudit second transistor (Q_5) pour coupler ledit quatrième signal (V_4) qui constitue une représentation d'une portion dudit second signal de commutation (V_2) à ladite électrode de commande dudit second transistor (Q_5) de manière telle que, aussi longtemps qu'une différence de signaux développée entre ladite électrode de commande et ladite seconde électrode conductrice de courant principal dudit premier transistor (Q_4), est plus grande qu'une valeur prédéterminée qui est une indication qu'un niveau de courant dans le premier transistor (Q_4) est supérieur audit niveau prédéterminé, ledit premier atténuateur commandable (Q_2 , R_{12}) affaiblit ladite portion de signal qui est développée sur ladite électrode de commande du second transistor (Q_5) pour retarder la conduction dans ledit second transistor. 25 30 35 40 45
7. Dispositif selon la revendication 6, caractérisé en ce que ledit premier atténuateur commandable comprend un diviseur de tension (R_6 , R_7 , R_8), couplé à ladite électrode de commande du premier transistor (Q_4), et un troisième transistor (Q_2) ayant une électrode conductrice de courant principal qui est couplée à l'électrode de commande dudit second transistor (Q_5) et ayant une électrode de commande qui est couplée à une borne de sortie dudit diviseur de tension, ledit troisième transistor (Q_2) for-

mant une impédance de shunt commandable sur l'électrode de commande dudit second transistor (Q_5) qui varie selon un signal qui est développé sur ladite borne de sortie du diviseur de tension et qui est proportionnel audit troisième signal (V_3) développé sur l'électrode de commande dudit premier transistor (Q_4) afin d'atténuer ledit signal qui est développé sur l'électrode de commande du second transistor (Q_5) tant que ledit premier transistor est conducteur, et lorsque ledit premier transistor devient non-conducteur, ladite impédance de shunt commandable (Q_2 , R_{11}) change de manière que le second transistor (Q_5) devienne conducteur.

8. Dispositif selon la revendication 7 caractérisé en ce que ladite impédance qui est formée par ledit troisième transistor (Q_2) présente une valeur sensiblement inférieure tant que ledit troisième signal (V_3), sur l'électrode de commande dudit premier transistor (Q_4) est plus grand qu'une valeur prédéterminée. 20
9. Dispositif selon la revendication 7 caractérisé en ce que ledit diviseur de tension comprend un réseau résistif (R_6 , R_7 , R_8) et dans lequel ledit premier atténuateur commandable comprend en outre des moyens de réaction (D_9), couplés entre ledit troisième transistor (Q_2) et une seconde borne de sortie dudit réseau résistif (R_6 , R_7 , R_8), pour générer un signal qui empêche ledit troisième transistor (Q_2) d'être saturé, afin de rendre ledit second transistor (Q_5), conducteur immédiatement après que le premier transistor (Q_4) devient non-conducteur. 25 30 35 40 45
10. Dispositif selon la revendication 6 caractérisé en ce que ledit premier atténuateur commandable comprend une résistance (R_{12}), couplée entre une borne (5) où est développé ledit second signal de commutation (V_2), et ladite électrode de commande du second transistor (Q_5) et un troisième transistor (Q_2) ayant une électrode conduisant le courant principal qui est couplée à une jonction entre ladite résistance (R_{12}) et ladite électrode de commande du second transistor (Q_5), de manière que ladite résistance (R_{12}) et ledit troisième transistor (Q_2) affaiblissent une portion dudit second signal de commutation (V_2) qui est couplé à ladite électrode de commande du second transistor (Q_5) tant que ledit premier transistor (Q_4) est conducteur, et lorsque ledit premier transistor (Q_4) devient non conducteur, une portion plus importante dudit second signal de commutation (V_2) est couplée à l'électrode de commande du second transistor (Q_5). 50 55



11, Dispositif selon la revendication 10 caractérisé par un quatrième transistor (Q_1) ayant une électrode conduisant le courant principal qui est couplée à ladite électrode de commande dudit premier transistor (Q_4) et comportant une électrode de commande qui est couplée à l'électrode de commande du second transistor (Q_5), ledit quatrième transistor (Q_1) affaiblissant ledit troisième signal (V_3) qui est développé sur ladite électrode de commande dudit premier transistor (Q_4) pour empêcher une conduction simultanée à la fois dans le premier (Q_4) et dans le second transistor (Q_5).

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