WHAT IS CLAIMED IS:

1. A method comprising:

providing a first N+ region and a first P+ region in a substrate for a silicon control rectifier (SCR);

providing first and second n-well regions in the substrate proximate the first N+ and P+ regions;

providing a second N+ region in the first n-well region, and a second P+ region in the second n-well region; and

coupling the first N+ and P+ regions to a ground rail, the second N+ region to a power rail, and the second P+ region to an I/O pad.

2. The method according to claim 1, further comprising:

providing a holding voltage of the SCR that is greater than a maximum operating voltage of the SCR during a latch-up event.

3. The method according to claim 2, further comprising:

providing the holding voltage of the SCR by turning on the power rail.

4. The method according to claim 1, further comprising:

providing a third P+ region in the second n-well region.

5. The method according to claim 4, further comprising:

providing the third P+ region between the second N+ and P+ regions.

6. The method according to claim 5, further comprising:

providing a third N+ region between the second and third P+ regions.

7. The method according to claim 4, further comprising:

providing a resistor having first and second resistor terminals;

providing a capacitor having first and second capacitor terminals; and

coupling the third P+ region to the first resistor and capacitor terminals, the second resistor terminal to the ground rail, and the second capacitor terminal to the I/O pad.

8. The method according to claim 1, further comprising:

providing the first N+ and P+ regions on a first side of the first n-well region; and

providing the second n-well region on a second side of the first n-well region, wherein the first side is opposite the second side.

9. The method according to claim 1, further comprising:

providing a holding current, a trigger current, or a combination thereof of the SCR that is greater than 100 milliamps (mA) during a latch-up event.

10. A device comprising:

a first N+ region and a first P+ region in a substrate;

first and second n-well regions in the substrate proximate the first N+ and P+ regions;

a second N+ region in the first n-well region; and

a second P+ region in the second n-well region, wherein the first N+ and P+ regions are coupled to a ground rail, the second N+ region is coupled to a power rail, and the second P+ region is coupled to an I/O pad.

11. The device according to claim 10, wherein a holding voltage of the device is greater than a maximum operating voltage of the device during a latch-up event.

12. The device according to claim 11, wherein the holding voltage of the device is provided by the power rail being turned on.

13. The device according to claim 1, further comprising:

a third P+ region in the second n-well region.

14. The device according to claim 13, wherein the third P+ region is between the second N+ and P+ regions.

15. The device according to claim 14, further comprising:

a third N+ region between the second and third P+ regions.

16. The device according to claim 13, further comprising:

a resistor having first and second resistor terminals; and

a capacitor having first and second capacitor terminals, wherein the third P+ region is coupled to the first resistor and capacitor terminals, the second resistor terminal is coupled to the ground rail, and the second capacitor terminal is coupled to the I/O pad.

17. The device according to claim 1, wherein the first N+ and P+ regions are on a first side of the first n-well region, and the second n-well region is on a second side of the first n-well region that is opposite the first side.

18. The device according to claim 1, wherein a holding current, a trigger current, or a combination thereof of the SCR is greater than 100 milliamps (mA) during a latch-up event.

19. A method comprising:

providing a first n-well region in a substrate for a silicon control rectifier (SCR);

providing a first N+ region and a first P+ region in the substrate on a first side of the first n-well region;

providing a second n-well on a second side of the first n-well region that is opposite the first side;

providing a second N+ region in the first n-well region, and a second P+ region in the second n-well region;

coupling the first N+ and P+ regions to a ground rail, the second N+ region to a power rail, and the second P+ region to an I/O pad;

providing a holding voltage of the SCR that is greater than a maximum operating voltage of the SCR during a latch-up event by turning on the power rail.

20. The method according to claim 19, further comprising:

providing a third P+ region between the second N+ and P+ regions;

providing a resistor having first and second resistor terminals;

providing a capacitor having first and second capacitor terminals; and

coupling the third P+ region to the first resistor and capacitor terminals, the second resistor terminal to the ground rail, and the second capacitor terminal to the I/O pad.

WHAT IS CLAIMED IS:

1. A method comprising:

providing a first n-well region in a substrate for a silicon control rectifier (SCR);

providing a first N+ region and a first P+ region in the substrate on a first side of the first n-well region;

providing a second n-well region on a second side of the first n-well region that is opposite the first side;

providing a second N+ region in the first n-well region, and a second P+ region in the second n-well region;

coupling the first N+ and P+ regions to a ground rail, the second N+ region to a power rail, and the second P+ region to an I/O pad;

providing a holding voltage of the SCR that is greater than a maximum operating voltage of the SCR during a latch-up event by turning on the power rail;

providing a third P+ region between the second N+ and P+ regions;

providing a resistor having first and second resistor terminals;

providing a capacitor having first and second capacitor terminals; and

coupling the third P+ region to the first resistor and capacitor terminals, the second resistor terminal to the ground rail, and the second capacitor terminal to the I/O pad.