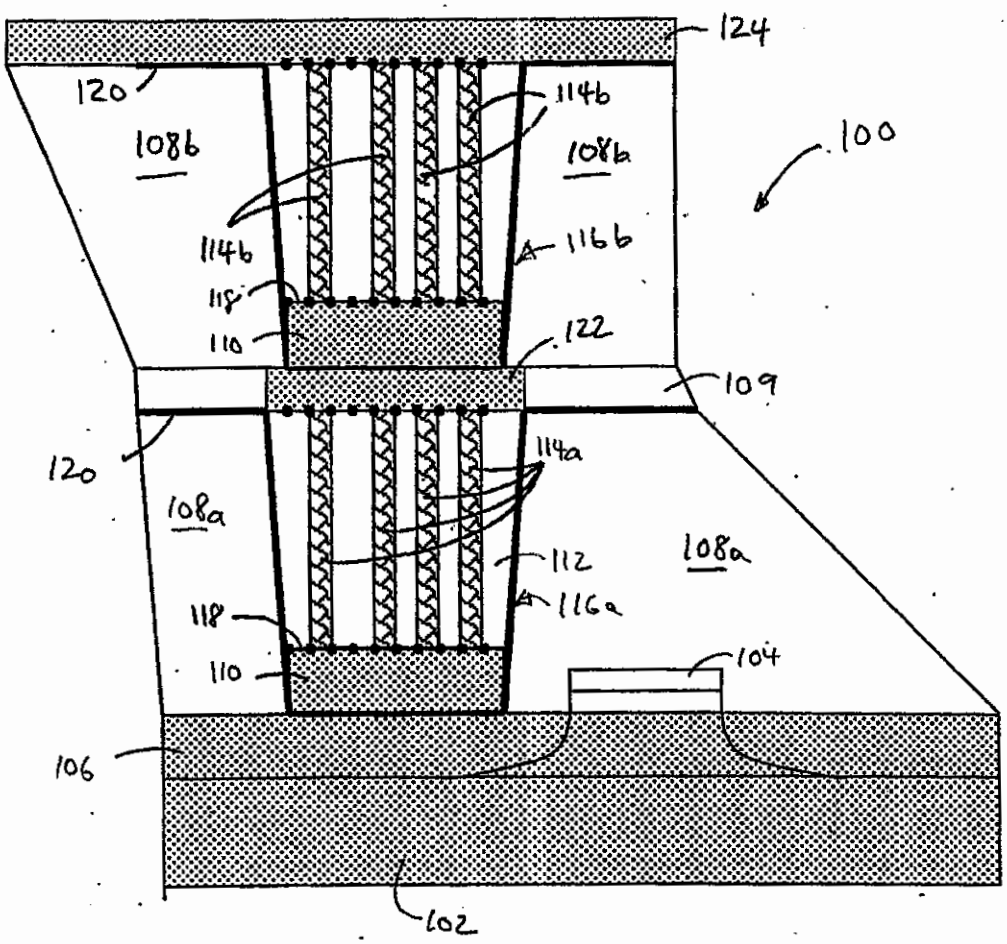

124
120
114b
108b
108b
100
114b
116b
118
110
122
109
120
114a
108a
112
108a
116a
118
110
104
106
102

Fig. 1

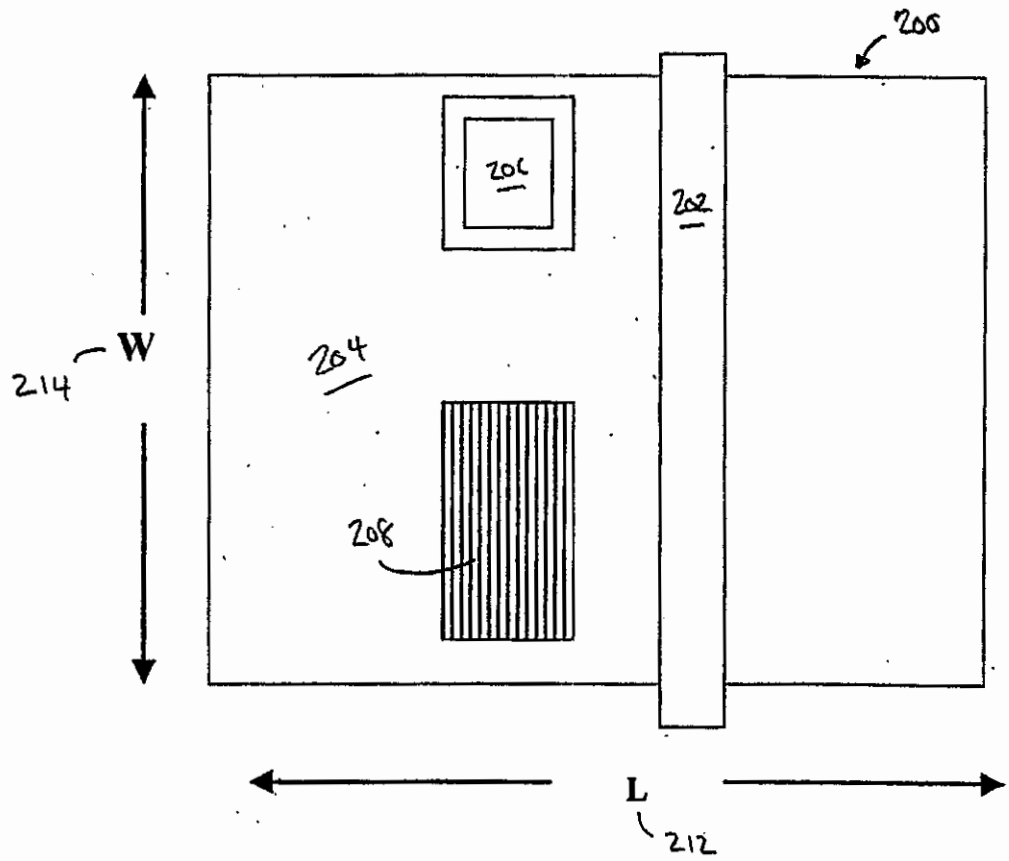


Fig. 2

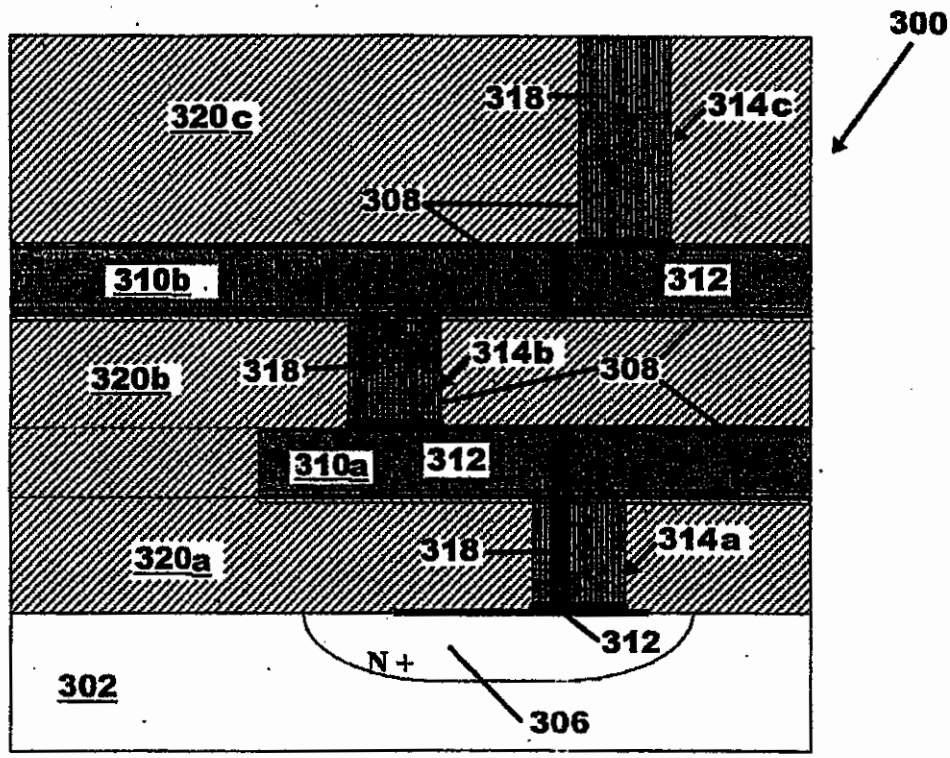

300
320c
318
314c
308
310b
312
320b
318
314b
308
310a
312
320a
318
314a
312
N+
302
306

Fig. 3

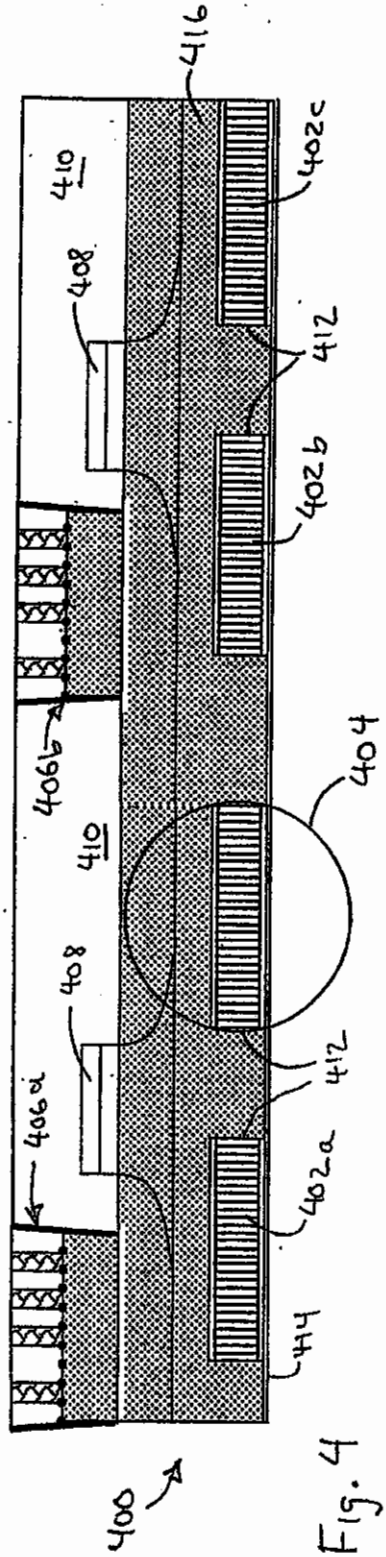

416
402c
410
408
412
402b
406b
404
410
408
412
406a
402a
414
400

Fig. 4

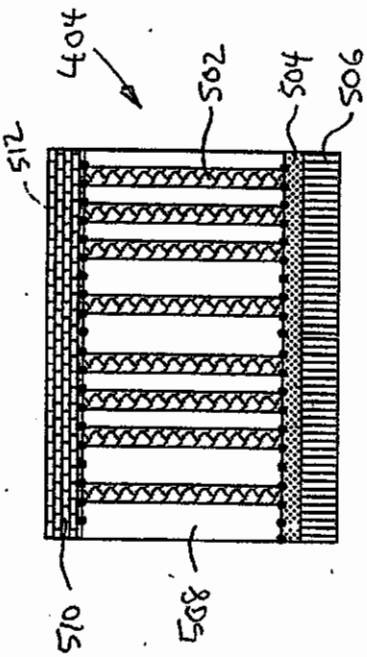

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502
504
506
512
510
508

Fig. 5

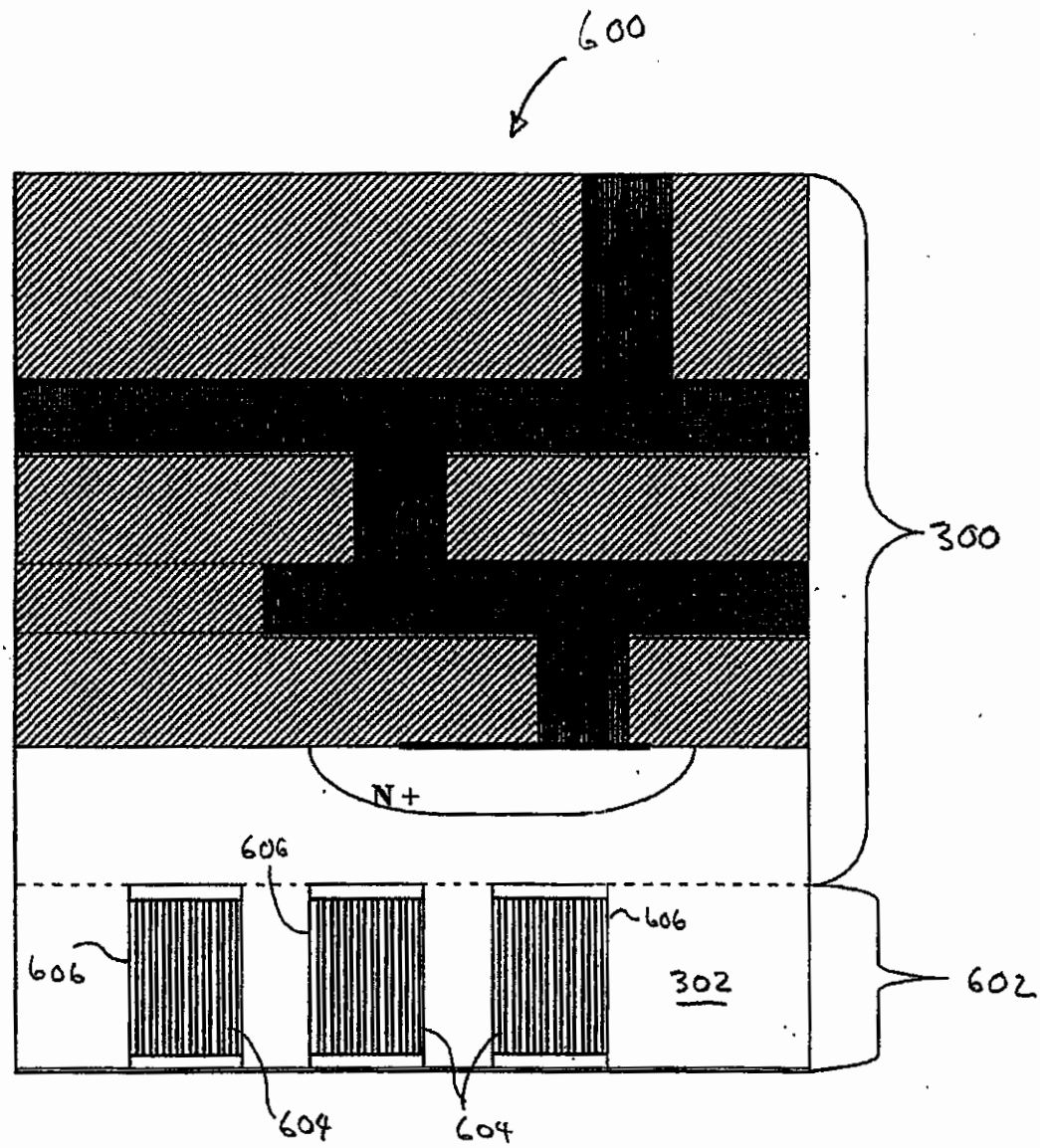


Fig. 6

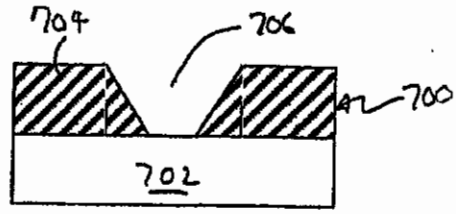


Fig. 7a PRIOR ART

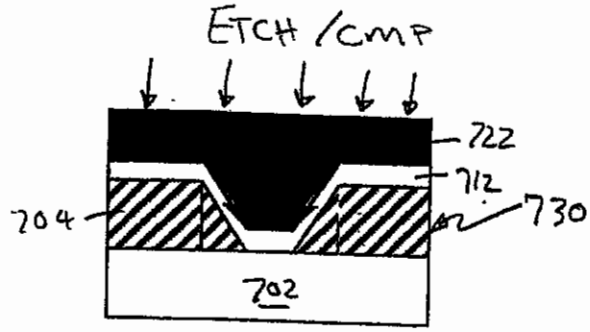


Fig. 7d PRIOR ART

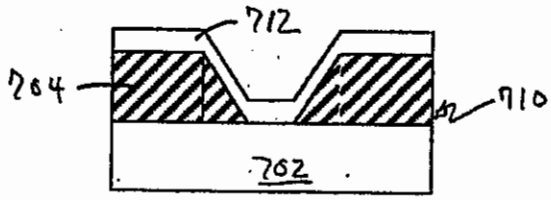


Fig 7b PRIOR ART

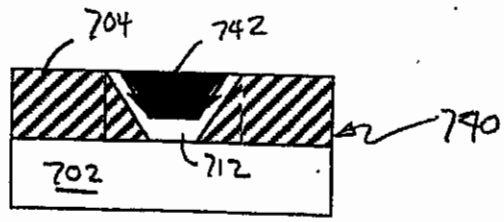


Fig. 7e PRIOR ART

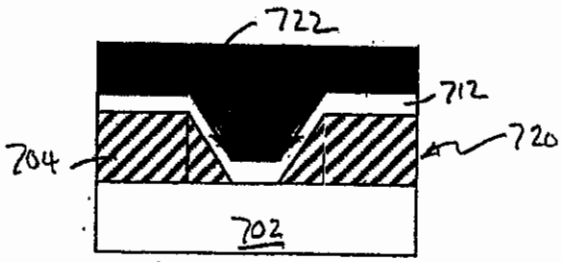


Fig. 7c PRIOR ART

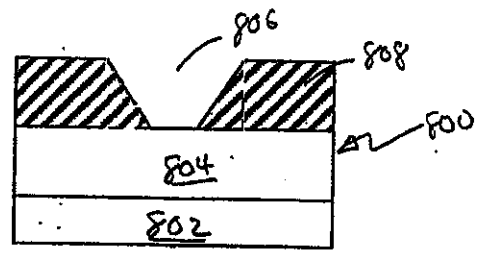


Fig. 8a

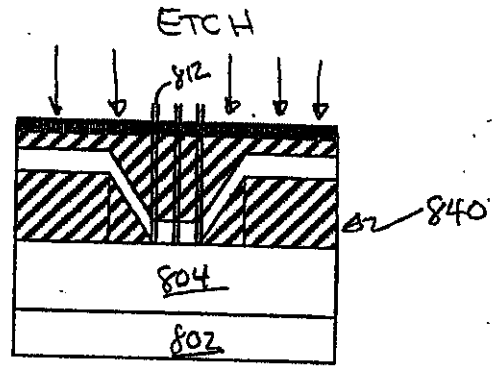


Fig. 8d

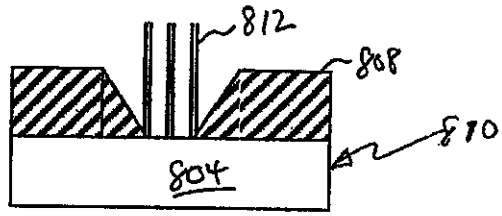


Fig. 8b

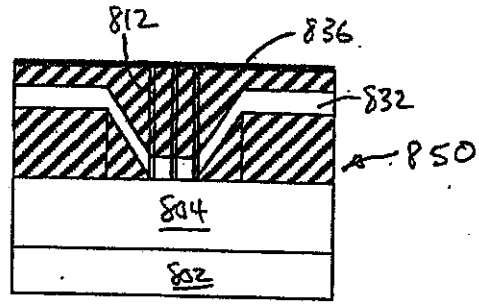


Fig 8e

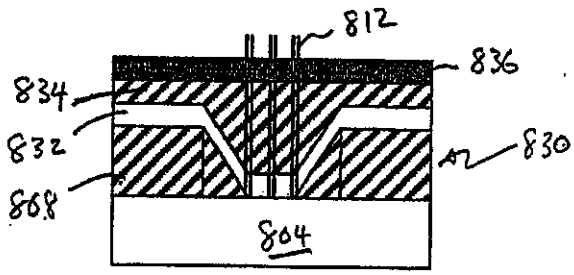


Fig 8c

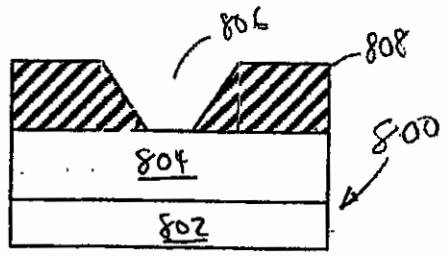


Fig. 8f

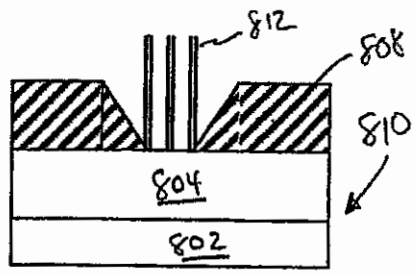


Fig. 8g

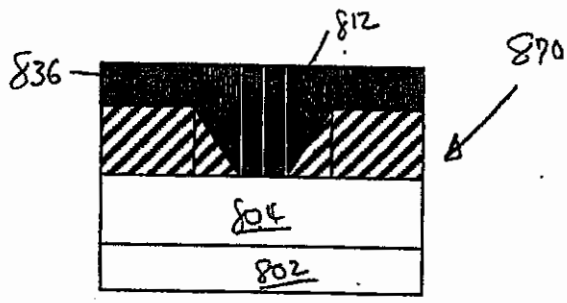


Fig. 8i

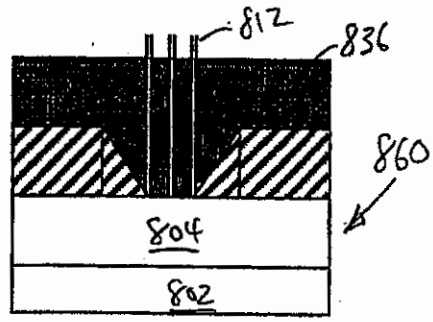


Fig. 8h

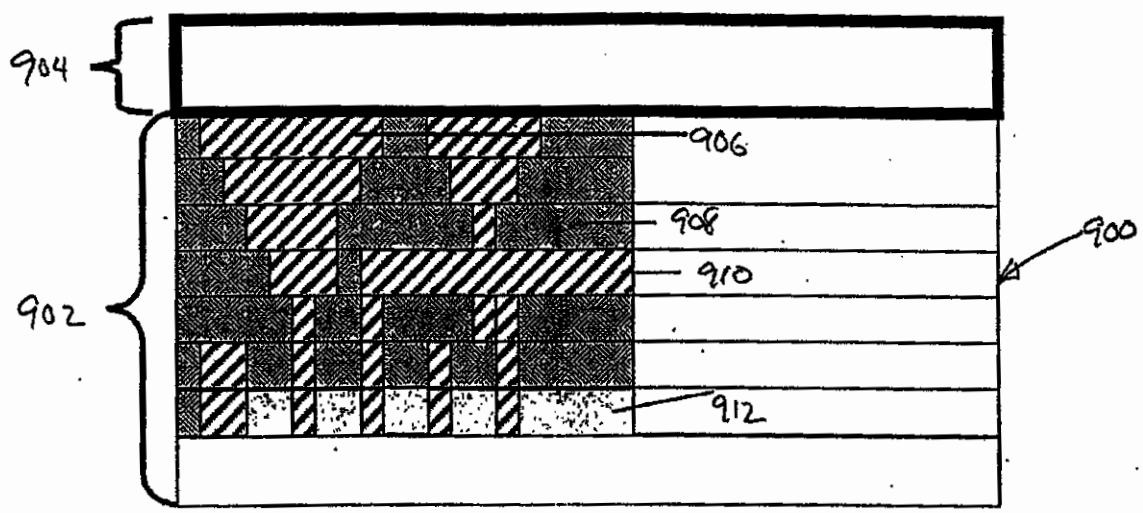
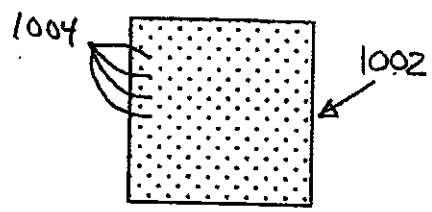


Fig. 9

Fig. 10B



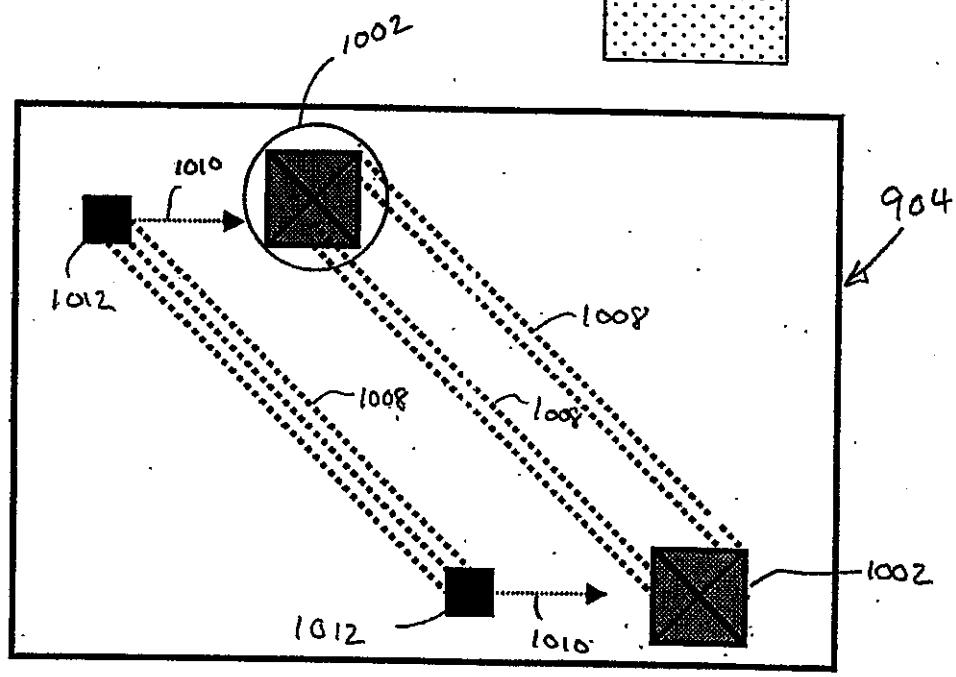


Fig 10A

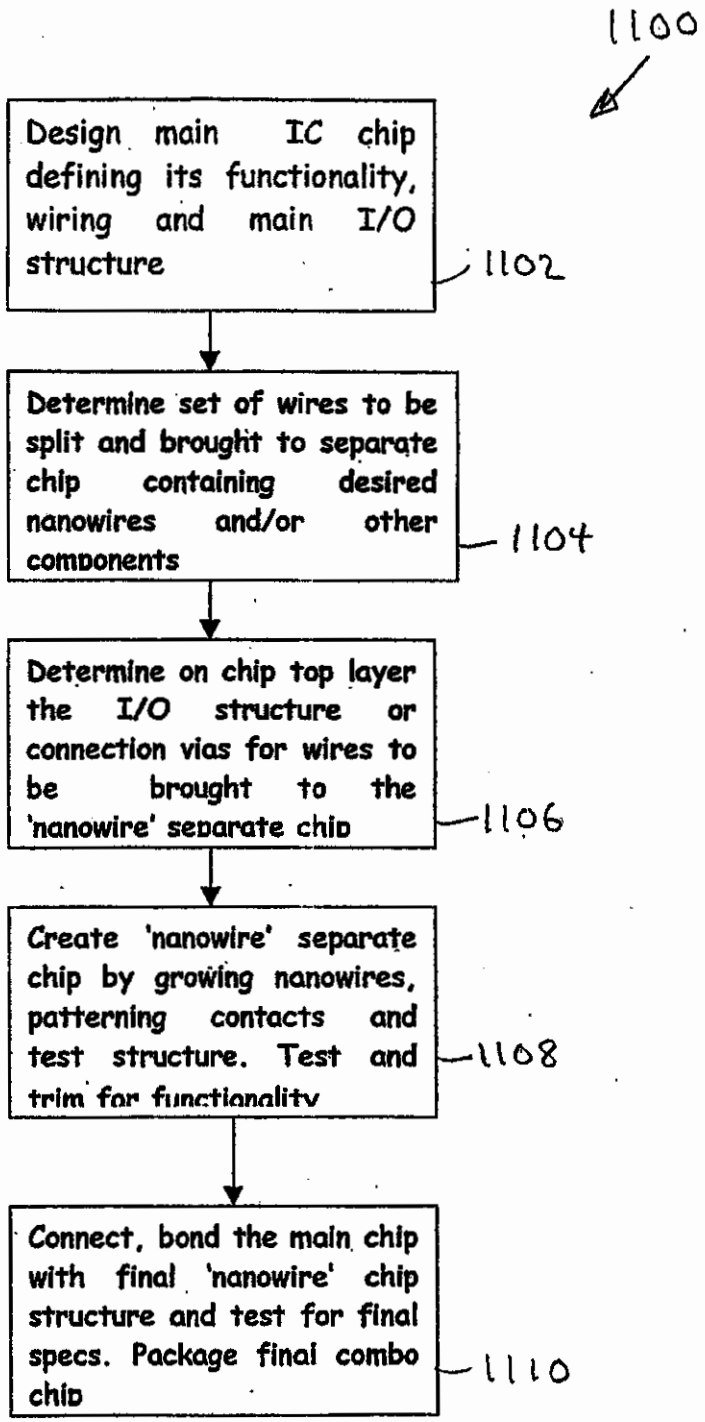

1100
Design main IC chip defining its functionality, wiring and main I/O structure
1102
Determine set of wires to be split and brought to separate chip containing desired nanowires and/or other components
1104
Determine on chip top layer the I/O structure or connection vias for wires to be brought to the 'nanowire' separate chip
1106
Create 'nanowire' separate chip by growing nanowires, patterning contacts and test structure. Test and trim for functionality
1108
Connect, bond the main chip with final 'nanowire' chip structure and test for final specs. Package final combo chip
1110

Fig. 11