WHAT IS CLAIMED IS:

1. An interposer substrate, comprising:

an array of interconnects in the interposer substrate, the array of connectors arranged in accordance with an array of interconnects for a processor on a circuit substrate;

at least one conductive trace in the interposer substrate in connection with at least one connector in the array of interconnects, the conductive trace arranged parallel to the interposer substrate such that no electrical connection exists between the connector in the interposer substrate and a corresponding one of the interconnects for the processor on the circuit substrate; and

at least one peripheral circuit residing on the interposer substrate in electrical connection with the conductive trace.

2. The interposer substrate of claim 1, wherein the interposer substrate comprises a flexible substrate.

3. The interposer substrate of claim 1, wherein the peripheral circuit comprises at least one memory chip.

4. The interposer substrate of claim 1, wherein the peripheral circuit further comprises at least one Peripheral Component Interconnect Express (PCIe) unit.

5. The interposer substrate of claim 1, wherein the peripheral circuit comprises a solid state disk drive.

6. The interposer substrate of claim 1, wherein the peripheral circuit is arranged on an edge of the interposer such that the interposer can fold when inserted between the processor and the circuit substrate.

7. The interposer substrate of claim 1, wherein the peripheral circuit attaches to the interposer by a connector.

8. The interposer substrate of claim 7, wherein the connector further comprises a memory micromodule connector.

9. The interposer substrate of claim 7, wherein the connector further comprises a coplanar connector.

10. The interposer substrate of claim 1, wherein the interposer substrate has multiple folds, each fold forming a plane of the interposer, each plane of the interposer holding at least one peripheral circuit.

11. The interposer substrate of claim 10, wherein the path length to each peripheral circuit is the same.

12. The interposer substrate of claim 1, wherein the array of interconnects on the interposer substrate comprise one of a land grid array, ball grid array, pin grid array or elastomer contacts.

13. The interposer substrate of claim 1, wherein the array of interconnects for the processor comprise one of a land grid array, ball grid array, pin grid array or a socket.

14. The interposer substrate of claim 1, wherein the conductive trace has a length of less than or equal to one quarter a wavelength of a highest frequency signal transmitted over the trace.

15. The interposer substrate of claim 1, wherein the interposer further comprises at least one connector of the array of interconnects in the interposer substrate that connects to one of the interconnects in the array of interconnects for the processor on the circuit substrate.

16. The interposer substrate of claim 15, wherein the one connector connects to memory circuits on the circuit substrate and the peripheral circuit on the interposer is configured as cache memory.

17. An apparatus comprising:

a processor having an array of interconnects arranged to connect the processor to conductive paths;

a circuit substrate having an array of interconnects arranged to provide connections between a processor and the circuit substrate, the circuit substrate having conductive paths connected to the array of interconnects;

an interposer substrate arranged between the processor and the circuit substrate, at least one conductive trace in the interposer substrate in connection with at least one connector in the array of interconnects on the processor, the conductive trace arranged parallel to the interposer substrate such that no electrical connection exists between the connector in the interposer substrate and a corresponding one of the interconnects on the processor on the circuit substrate; and

at least one peripheral circuit connected to the at least one conductive trace.

18. The apparatus of claim 17, the apparatus further comprising a heat sink thermally coupled to the processor and the peripheral circuit.

19. The apparatus of claim 18, wherein the heat sink thermally coupled to the processor comprises one of either the heat sink directly contacting the processor, or a thermal transfer sheet between the heat sink and the processor

20. The apparatus of claim 17, wherein the interposer further comprises at least one connector of the array of interconnects in the interposer substrate that connects to one of the interconnects in the array of interconnects for the processor on the circuit substrate.

21. The apparatus of claim 17, wherein the circuit substrate comprises one of a motherboard having an array of memory interconnects, or a motherboard without any memory interconnects.

WHAT IS CLAIMED IS:

1. An interposer substrate, comprising:

a first array of interposer interconnects in the interposer substrate, each interposer interconnect in the first array of interposer interconnects corresponding to interconnects in an array of processor interconnects;

a second array of interposer interconnects in the interposer substrate, each interposer interconnect in the second array of the interposer interconnects corresponding to an array of circuit interconnects on a circuit substrate; and

at least one conductive trace in the interposer substrate in connection with at least one interconnect in the first array of interposer interconnects, the conductive trace arranged to have a parallel portion parallel to the interposer substrate such that no electrical connection exists between the interconnect and a corresponding one of the interposer interconnects in the second array of interposer interconnects; and

at least one peripheral circuit residing on the interposer substrate in electrical connection with the conductive trace.

2. The interposer substrate of claim 1, wherein the interposer substrate comprises a flexible substrate.

3. The interposer substrate of claim 1, wherein the peripheral circuit comprises at least one memory chip.

4. The interposer substrate of claim 1, wherein the peripheral circuit further comprises at least one Peripheral Component Interconnect Express (PCIe) unit.

5. The interposer substrate of claim 1, wherein the peripheral circuit comprises a solid state disk drive.

6. The interposer substrate of claim 1, wherein the peripheral circuit is arranged on an edge of the interposer such that the interposer can fold when inserted between the processor and the circuit substrate.

7. The interposer substrate of claim 1, wherein the peripheral circuit attaches to the interposer by a connector.

8. The interposer substrate of claim 7, wherein the connector further comprises a memory micromodule connector.

9. The interposer substrate of claim 7, wherein the connector further comprises a coplanar connector.

10. The interposer substrate of claim 1, wherein the interposer substrate has multiple folds, each fold forming a plane of the interposer, each plane of the interposer holding at least one

peripheral circuit.

11. The interposer substrate of claim 10, wherein the path length to each peripheral circuit is the same.

12. The interposer substrate of claim 1, wherein the array of interconnects on the interposer substrate comprise one of a land grid array, ball grid array, pin grid array or elastomer contacts.

13. The interposer substrate of claim 1, wherein the array of interconnects for the processor comprise one of a land grid array, ball grid array, pin grid array or a socket.

14. The interposer substrate of claim 1, wherein the conductive trace has a length of less than or equal to one quarter a wavelength of a highest frequency signal transmitted over the trace.

15. The interposer substrate of claim 1, wherein the interposer further comprises at least one connector of the array of interconnects in the interposer substrate that connects to one of the interconnects in the array of interconnects for the processor on the circuit substrate.

16. The interposer substrate of claim 15, wherein the one connector connects to memory circuits on the circuit substrate and the peripheral circuit on the interposer is configured as cache memory.

17. An apparatus comprising:

a processor having an array of processor interconnects arranged to connect the processor to conductive paths;

a circuit substrate having an array of circuit interconnects arranged to provide connections between the processor and the circuit substrate, the circuit substrate having conductive paths connected to the array of circuit interconnects;

an interposer substrate arranged between the processor and the circuit substrate, at least one conductive trace in the interposer substrate in connection with at least one processor interconnect in the array of interconnects on the processor, the conductive trace arranged at least partially parallel to the interposer substrate such that no electrical connection exists between the conductive trace in the interposer substrate and a corresponding one of the circuit interconnects on the circuit substrate; and

at least one peripheral circuit connected to the at least one conductive trace.

18. The apparatus of claim 17, the apparatus further comprising a heat sink thermally coupled to the processor and the peripheral circuit.

19. The apparatus of claim 18, wherein the heat sink thermally coupled to the processor comprises one of either the heat sink directly contacting the processor, or a thermal transfer sheet between the heat sink and the processor.

20. The apparatus of claim 17, wherein the interposer further comprises at least one connector of the array of interconnects in the interposer substrate that connects to one of the interconnects in the array of interconnects for the processor on the circuit substrate.

21. The apparatus of claim 17, wherein the circuit substrate comprises one of a motherboard having an array of memory interconnects, or a motherboard without any memory interconnects.