

## ABSTRACT OF THE DISCLOSURE

A storage device may include a one time programmable (OTP) memory including a plurality of OTP cells and configured to store OTP key values in the plurality of OTP cells, and an erase instruction circuit that is detachably mounted on the storage device and connected to a first node of the OTP memory. When the erase instruction circuit is removed from the storage device, the OTP memory may be configured to receive the erase instruction signal having a first logic level at the first node and permanently erase all the OTP key values stored in the plurality of OTP cells by programming the plurality of OTP cells to an identical OTP key value in response to the erase instruction signal having the first logic level.

FIG. 4