METHODS FOR ENHANCING DIE SAW AND PACKAGING RELIABILITY

CROSS REFERENCE

[0001] The present application is a Continuation-In-Part application of U.S. Patent Application Serial No. 10/940,504 and claiming the benefits thereof.

BACKGROUND

[0002] The present invention relates generally to an integrated circuit (IC) design, and more particularly to a processing method for reducing die saw induced damage on the circuit during the cutting or breaking processes of the wafer while also improving packaging reliability.

[0003] In semiconductor technology, a large quantity of chips containing integrated circuits is created together within a wafer. Each wafer contains many dies, which are the specified areas required for the formation of a chip. As known by those skilled in the art, the dies on the wafer are separated with a space typically known as the scribe streets or the scribe lines. This space is designed to be large enough to allow separation of the die by cutting or breaking without damaging the chips within the die. During the cutting or breaking process of the wafer at the scribe lines, die saw induced damage can originate from crack propagation above and beneath the surface of the silicon (Si) substrate, thereby leading to serious chip damage or failure.

[0004] In order to reduce the die saw induced damage created at the scribe line, conventional methods such as crack-stop structure designs, interfacial adhesion enhancement, and material properties optimization are currently being practiced.

However, all conventional methods try to avoid crack propagation along the material interfaces above the Si substrate. By limiting the crack propagation above the Si substrate alone is not enough since the crack propagation can still frequently occur underneath the Si substrate which also leads to serious chip damage or failure.

[0005] For chips that were not damaged from the initial cutting or breaking process, it is still possible for crack propagation to occur during the packaging process of the chip, because it is during this time that additional stress is applied onto the chip.

[0006] Therefore, it is desirable to have a more reliable processing method for reducing or eliminating crack propagation damage to the chip during the cutting and packaging processes.

SUMMARY

[0007] In view of the foregoing, this invention provides a processing method and stress reduction mechanism on a wafer for reducing die saw induced damage done to the circuit during the cutting or breaking process of the wafer while also improving the packaging reliability. In one embodiment of the present invention, a seal ring is implemented to reduce the stress applied on a film stack of the circuit caused by the cutting or breaking process of the wafer. A shallow trench isolation is created beneath the surface of the silicon substrate to limit crack propagation caused by the cutting or breaking process from reaching the circuit area. A ditch is optionally implemented to reduce the stress applied on the film stack.

[0008] The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood

from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1A shows a cross-sectional view of a CMOS process with various design elements implemented to help reduce the chances of die saw induced damage during the cutting or breaking process of a wafer in accordance to one embodiment of the present invention.

[0010] FIG. 1B illustrates a diagram showing a top-view of the die area shown within FIG. 1A.

DESCRIPTION

[0011] The present disclosure provides a processing method for reducing die saw induced damage on scribe lines during the cutting or breaking process of the wafer.

[0012] FIG. 1A shows a cross-sectional view 100 of a CMOS process where various design elements are implemented for reducing the chances of die saw induced damage during the cutting or breaking process of a wafer in accordance to one embodiment of the present invention. The design elements are a seal ring 102 and a shallow trench isolation (STI) 106. The seal ring 102 is implemented above and/or around the metal layers that make up a film stack 104, which constitutes an active area for cell circuits. The seal ring 102 can have a width about or larger than 10 μm. The STI 106 is implemented within a silicon (Si) substrate 108 outside the area of the film stack 104. The STI 106 is filled by dielectrics such as SiO_2. The depth of the STI 106 can vary, but is preferred to be larger than 3000 Å. Also, there could be more than one STI 106 to be placed for the same protection purpose. The area

outside of the seal ring 102 is understood to be any area not surrounded by the seal ring 102. A ditch 110, which is another design element for further reducing die saw induced damage, is optionally etched down to the surface of the Si substrate 108 outside the area of the film stack 104.

[0013] The process includes the etching of the Si substrate 108 for the fabrication of the STI 106. The STI 106, typically used for creating isolation within the silicon area, is created by depositing oxide into the etched trench. The STI 106 in this example is designed to stop any die saw induced cracks propagation that may reach the circuit area through the Si substrate 108 during the cutting or breaking process of the wafer. For this reason, the STI 106 must be created outside the area of the cell circuits and the seal ring 102. The seal ring 102 is used for keeping contamination away from the film stack 104, which contains layers of conductive and non-conductive materials making up the circuitries of the chip. It is a continuous ring of narrow contact strip that surrounds the active area of the die (e.g., around the film stack 104).

[0014] A scribe line, not shown in this figure, surrounding the entire chip within the film stack 104 typically consists of bare silicon with no active circuitry. Contaminants can seep laterally into the exposed oxide layers abutting the scribe line. Therefore, the scribe ring 102 is placed around the film stack 104 to block any mobile ions. The seal ring 102 is created in the same manner as the film stack 104 where it contains layers of metal connected together through via contacts with oxide implemented between layers. For ease of fabrication, the seal ring 102 is designed to be at the same height as the film stack 104. The seal ring 102 can prevent contamination from entering laterally into the exposed oxide layers abutting the scribe line. It is crucial for the seal ring 102 to be a continuous ring uninterrupted by

any gaps in order to block all lateral movement of mobile ions. While the seal ring 102 serves no functional purposes other than to keep contamination from reaching the circuits within the film stack 104, it is still connected to the ground, which is a P-type diffusion in this example, via a substrate contact 112. It is understood by those skilled in the art that the seal ring 102 and the circuitry within the film stack 104 shares the same ground. During production, the metal layers of the chip within the stack film 104 and the metal layers within the seal ring 102 are formed at the same time. The seal ring 102 also contains a contamination barrier mechanism that is formed by flapping a protective overcoat, which is not shown in this figure, directly on top of the exposed silicon including the surface of the chip or the film stack 104, the surface of the seal ring 102, and the STI 106. This protective overcoat is designed to stretch from the surface of the film stack 104 all the way to the scribe line to serve as another barrier to any mobile ions created from a cutting or breaking process of the wafer by preventing mobile ions from reaching the oxide layers that are in contact with the chip within film stack 104. Note that a flap-down of the protective overcoat is used to cover the scribe line, which is much lower in height since it is designed for saw blade to cut. This flap-down of the protective overcoat is permitted since the scribe line does not contain any active circuitry. Any mobile ions created from a cutting or breaking process of the wafer attempting to penetrate the seal ring 102 must first surmount this protective overcoat and pass the continuous seal ring 102 before reaching the active region of the die. The seal ring 102 can also effectively prevent all crack propagation through the material interfaces above the Si substrate 108.

[0015] To further prevent crack propagation created from the cutting or breaking process of the wafer, the ditch 110 can be fabricated from the very top of the wafer level film stack 104 down to the surface of the Si substrate 108. The ditch 110 can

reduce the stress applied on the circuits within the film stack 104 during the cutting or breaking process. Like the STI 106, the ditch 110 must also be created outside the area of the cell circuits and the seal ring 102. As an optional final step, a block 114 is used to show the proper cutting or breaking area within the scribe line of the wafer. This block 114 may be seen as a die sawing guiding mechanism. The stress applied from the cutting or breaking process at the scribe line will not affect the film stack 104 due to the implementation of the seal ring 102 and the ditch 110 while the crack propagation beneath the surface of the Si substrate 108 is limited by the STI 106.

[0016] Note that with the implementation of this method, the chance of crack propagation within circuit during the packaging process is also reduced. It is also understood by those skilled in the art that this processing method can be achieved with existing tool and recipes and that no new or extra fabrication processes are necessary.

[0017] FIG. 1B illustrates a diagram 116 showing a top-view of the die area shown within FIG. 1A. A block 118 is used to represent the core circuitry of the chip, which is also shown as the film stack 104 within FIG. 1A. The core circuitry within the block 118 will be surrounded by the seal ring 102, now seen in a top-view. The seal ring 102, which is designed to be the same height as the film stack 104, helps to keep contamination from reaching the core circuitry within the block 118. The seal ring 102 can also prevent any contamination from entering laterally reaching the circuitry since it is created with the same metal layers, via contacts, and dielectric layers as the film stack 104. The width of the seal ring, which is not wide, is only a small percentage of the width of scribe lines 120. In order to protect the chip from die saw induced crack propagation through the Si substrate, the STI ring 106, now seen in a top-view, is implemented outside the seal ring beneath the surface of the Si

substrate. To reduce the stress applied on the film stack 104 during the die saw process, the ditch 110 may be optionally etched down to the surface of the Si substrate from the outer edge of the seal ring 102 to the outer edge of the scribe lines 120.

[0018] The above illustration provides many different embodiments or embodiments for implementing different features of the invention. Specific embodiments of components and processes are described to help clarify the invention. These are, of course, merely embodiments and are not intended to limit the invention from that described in the claims.

[0019] Although the invention is illustrated and described herein as embodied in one or more specific examples, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention, as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor wafer with die saw induced stress reduction mechanism having one or more circuits fabricated in at least one active area on a semiconductor substrate, and having a scribe line for cutting the active area there along, the wafer comprising:

at least one seal ring around the active area; and

at least one shallow trench isolation in the semiconductor substrate between the seal ring and the scribe line.

2. The wafer of claim 1, wherein the seal ring is a continuous ring surrounding the active area.

3. The wafer of claim 1, wherein the seal ring has a width more than about 10 μm.

4. The wafer of claim 1, wherein the active area is a film stack containing one or more layers of conducting materials connected together through via contacts with dielectric materials implemented between the one or more layers.

5. The wafer of claim 1, wherein the seal ring connects to ground via one or more contacts to the semiconductor substrate.

6. The wafer of claim 1, wherein the shallow trench isolation is a trench filled with at least one dielectric material.

7. The wafer of claim 1 wherein the shallow isolation trench has a depth of at least 3000 Å.

8. The wafer of claim 1, further comprising a ditch on the substrate between the seal ring and the scribe line.

9. The wafer of claim 8, wherein the ditch is fabricated on top of the shallow trench isolation.

10. A semiconductor wafer with die saw induced stress reduction mechanism having one or more circuits fabricated in at least one active area on a semiconductor substrate, and having a scribe line for cutting the active area there along, the wafer comprising:

at least one seal ring around the active area;

at least one shallow trench isolation in the semiconductor substrate between the seal ring and the scribe line; and

a ditch on the substrate between the seal ring and the scribe line and on top of the shallow trench isolation.

11. The wafer of claim 10, wherein the seal ring has a width more than about 10 μm.

12. The wafer of claim 10, wherein the seal ring connects to ground via one or more contacts to the semiconductor substrate.

13. The wafer of claim 10, wherein the shallow trench isolation is a trench filled with at least one dielectric material.

14. The wafer of claim 10, wherein the shallow isolation trench has a depth of at least 3000 Å.

15. A method for reducing die saw induced stress on a circuit fabricated in an active area on a semiconductor substrate when the active area is cut along a scribe line, the method comprising:

fabricating a seal ring around the active area; and

fabricating a shallow trench isolation between the seal ring and the scribe line by etching into a portion of the semiconductor substrate.

16. The method of claim 15 further comprising fabricating a ditch on the semiconductor substrate between the seal ring and the scribe line on top of the shallow trench isolation.

17. The method of claim 15, wherein the seal ring has a width more than about 10 μm.

18. The method of claim 15, wherein the seal ring connects to ground via one or more contacts to the semiconductor substrate.

19. The method of claim 15, wherein the shallow isolation trench has a depth of at least 3000 Å.