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Specification

Prior Art

The invention relates to a circuit arrangement for the suppression of noise signals during the transmission of digital signals.

It is known to amplify the signals received by a receiver for such signals, in a preamplifier. The amplified amplitudes are then stored by means of an RC network so that an analogue value corresponding to the amplitudes forms at this. The digital signals rising above this analogue value drive a following amplifier stage. Noise pulses which are below the stored value are suppressed in the course of this. If the spacing of the wanted pulses

varies, the time constant of the RC network must be designed so that the signals with the shorter spacing are still transmitted. The consequence of this, however, is that if the pulse spacing of the digital signal is relatively great, the stored analogue value has dropped to such an extent that noise pulses can get through more easily, for example digital signals with different spacing, that is to say pulse-code modulated signals, are used in the remote control of radio and television equipment. The signals transmitted by means of infrared light as a carrier consist of a plurality of short serial pulses, the information, that is to say which channel of the television service is to be influenced, lying in the different spacing between the individual pulses. In this manner, digital words are formed from a plurality of bits, a longer spacing forming an H-signal for example and a shorter spacing an L-signal.

In the circuit designs hitherto known with remote control of receiving sets, individual noise pulses were not very critical because test circuits do not accept an erroneously received instruction. It is different in the receiver art if these are equipped with microprocessors and the microprocessor carries out the most varied controls and monitoring in succession through its program, such as interrogation of the remote control, indication of the display, tuning and frequency control etc. for example.

The program of the microprocessor system is prepared in such a manner that this gives priority to the handling of remote-control instructions. In the course of the program, a repeated check is made as to whether a remote-control instruction is present, otherwise other subroutines run continuously. Now if powerful noise pulses are present, calling up is continuous so that the microprocessor system cannot perform other tasks.

In DE-OS 2 943 913, a circuit arrangement is described which serves for the reception of light signals in the form of pulses by means of optoelectronic transducer devices. The object of this said Application is therefore to eliminate interfering light components, particularly in the form of constant light, to produce a variable threshold depending on the proportion of constant light, so that only the wanted pulses are evaluated. For this purpose, various time-constant elements are provided at the input of the circuit, of which the one only produces a voltage in the event of low-frequency signal components, higher-frequency signals are short-circuited by a capacitor. The other time-constant element forms a short circuit for the low-frequency signal components. The ratio of the voltages divided by the time-constant elements is dependent on frequency and not dependent on the amplitude. In the circuit disclosed there, the threshold value is determined

largely by the low-frequency modulated signal component of the current flowing through the receiving diodes but not by the height of the signal amplitude.

A following comparator serves as an amplitude filter with an adjustable comparator threshold. Here the threshold is dependent on the interfering light component.

It is the object of the invention, in the circuit arrangement of the type defined in the preamble to Patent Claim 1, to suppress noise pulses while, depending on the input amplitude, noise pulses which make microprocessor-controlled tuning systems unusable in particular, are suppressed both with weak and with strong input signals.

This problem is solved by the features given in the characterising part of Patent Claim 1.

Description

In order to explain the invention, this will be described with the aid of the drawing with reference to one example.

Figure 1 shows the relationships in the former circuitry;

Figure 2 shows signal patterns at the marked points of the circuit;

Figures 3 and 4 show the corresponding conditions which are achieved by the invention.

In Figure 1, the prior art is first explained with reference to a pulse-code modulated remote-control signal. The remote-control signals pass, via the receiver diode D1,

to a first amplifier stage V1. The amplified pulses of the pulse-code modulated remote-control signal as shown in Figure 2A appear at the output A. These are rectified by means of the diode D2 and the peak value is stored in an RC network R1C1. The analogue value B shown in Figure 2B results from the time constant R1C1. The difference between the amplitudes of the wanted signal and the stored peak value reaches the next stage V2 via the coupling capacitor C3. The pulse crests shown in Figure 2C control the following stage V2. The remote-control signal shown in Figure 2D appears at the output D.

If noise pulses S are received as well as the wanted signal N, the former may be effective and harmful if they rise above the analogue voltage at the point B. This is particularly critical when, with wide pulse spacing of the wanted signal, the voltage at the point B has dropped to such an extent that the noise pulses S cause signals corresponding to the wanted pulses at the output D.

The circuit shown in Figure 3 serves to remedy this drawback. Here the components corresponding to those in Figure 1 are provided with the same reference symbols. In contrast to the circuit previously described, an additional RC network R2C2 is introduced and a voltage-limiting Zener diode is connected in parallel with the first RC network R1C1. Voltages as shown in Figure 4 A-D result at the

points A, B1, B2, C and D. The time constant of the RC network R2C2 is substantially higher than that of the first RC network R1C1. The voltage limitation at the latter is designed by the Zener diode Z so that a variation by this value is sufficient to drive the following stage V2 definitely. The time constant R1C1 is determined in known manner according to the shortest spacing of the wanted signals while the time constant R2C2 depends on the maximum spacing of the wanted signal pulses. In this case, it may also be a question of the long intervals between the individual pulse packets which form the individual digital control words.

What is important in the circuit arrangement described is that the voltages stored in the time constant networks R1, C1, R2, C2 relate to the peak voltage of the wanted signal. Here the stored voltage is determined only by the wanted signals. The ratio of the voltages divided in the time constant networks R1/C1 and R2/C2 is, with very low amplitudes, dependent on the divider ratios R1:R2 and C1:C2 respectively. With higher amplitudes, the limitation by the element Z becomes effective. The voltage at the time constant network R1/C1 cannot rise above the limited value determined by Z so that the remaining signal component decreases at the second time constant network R2/C2.

With the circuit just described, a reliable suppression of noise pulses is ensured so long as these are smaller

than the wanted signal minus the maximum possible voltage at the first RC network R1C1 caused by the voltage-limiting means Z.

The circuit works satisfactorily even when, as a result of using a capacitor with a very low value, the time constant R1C1 is extremely small, which is indicated by the broken curve in Figure 4 B2.

Patent Claims

1. A circuit arrangement for the suppression of noise pulses in the transmission of digital signals with different spacing in time and different amplitudes with a first time constant network and a second time constant network connected in series with this, the time constant networks being disposed in the wanted signal path, characterised in that the two time constant networks (R1, C1; R2, C2) have time constants which differ greatly from one another and that a voltage-limiting means (Z) is connected in parallel with the first time constant network (R1, C1) with the smaller time constant, the signal applied to the time constant networks (R1, C1; R2, C2) connected in series being divided at these in such a manner that the signal applied to the first time constant network (R1, C1) serves to drive a following switch stage (V2) and that the signal applied to the second time constant network (R2, C2) supplies a signal-to-noise ratio depending on the amplitude of the wanted signal (N), the voltage component of the wanted

signal (N) at the first time constant network (R1, C1) with the smaller time constant being restricted to the value preset by the voltage-limiting means (Z), and that the first time constant network (R1, C1) is dimensioned in such a manner that the voltage applied to this has dropped, before the arrival of the next wanted pulse (N), to such a value that the wanted pulse (N) definitely switches through the following amplifier stage (V2) working as a switch.

2. A circuit arrangement as claimed in Claim 1, characterised in that the time constant of the second time constant network (R2, C2) is dimensioned according to the maximum spacing in the pulse train of the wanted signal.

Claims

1. A circuit for suppressing interference signals during the transmission of digital signals having different spacing in time and different amplitudes, comprising a first component for establishing a time constant and a second component for establishing a time constant connected in series in relation to the first, the components for establishing time constants being disposed in the wanted-signal transmission path, characterised in that the two components for establishing time constants (R1, C1; R2, C2) have time constants differing greatly from one another, in that the first component for establishing a time constant

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signal (N) at the first time constant network (R1, C1) with the smaller time constant being restricted to the value preset by the voltage-limiting means (Z), and that the first time constant network (R1, C1) is dimensioned in such a manner that the voltage applied to this has dropped, before the arrival of the next wanted pulse (N), to such a value that the wanted pulse (N) definitely switches through the following amplifier stage (V2) working as a switch.

2. A circuit arrangement as claimed in Claim 1, characterised in that the time constant of the second time constant network (R2, C2) is dimensioned according to the maximum spacing in the pulse train of the wanted signal.

Claims

1. A circuit for suppressing interference signals during the transmission of digital signals having different spacing in time and different amplitudes, comprising a first component for establishing a time constant and a second component for establishing a time constant connected in series in relation to the first, the components for establishing time constants being disposed in the wanted-signal transmission path, characterised in that the two components for establishing time constants (R1, C1; R2, C2) have time constants differing greatly from one another, in that the first component for establishing a time constant

(R1, C1) having the smallest time constant is connected in parallel with a voltage limiting means (Z) in which case the signal (N) applied to the components for establishing time constants (R1, C1; R2, C2) connected in series is divided in these in such a manner that the signal applied to the first component for establishing a time constant (R1, C1) serves to control the following switching stage (V2), in that the signal applied to the second component for establishing a time constant (R2, C2) determines a spacing which depends on the amplitude of the wanted signal, the voltage fraction of the wanted signal (N) applied to the first component for establishing a time constant (R1, C1) having the smaller time constant being limited to the value predetermined by the voltage limiting means (Z), and in that the first component for establishing a time constant (R1, C1) is dimensioned in such a manner that the voltage which is applied to it is reduced, before the arrival of the following wanted pulse (N), to such a value that the wanted pulse (N) definitely controls the following amplifier stage (V2) working as a switch.

2. A circuit as claimed in Claim 1, characterised in that the time constant of the second component for establishing a time constant (R2, C2) is defined depending on the greatest spacing of the pulse sequence of the wanted signal.