

METHOD AND APPARATUS FOR GENERATING A PULSE WIDTH MODULATED SIGNAL

5 Field of the Invention

This invention relates generally to pulse width modulation, and more specifically to converting either a pulse density modulated data stream or a pulse code modulated data stream to a pulse width
10 modulated signal.

Background of the Invention

Pulse width modulation (PWM) is a suitable method to create a
15 power signal with high efficiency. In particular, many high efficiency digital audio switching power amplifiers are based on PWM signaling. Digital audio inputs to these amplifiers are typically pulse code modulated (PCM). Direct translation from PCM to PWM to generate a uniformly sampled PWM (UPWM) signal is a nonlinear operation that
20 results in a large amount of harmonic distortion. In contrast, naturally sampled PWM (NPWM) does not contain harmonic distortion. Naturally sampled PWM signals are easily generated in the analog domain by comparing an analog input signal to a sawtooth or triangular shaped ramp signal. The NPWM pulse edges are determined by the
25 natural crosspoints between the input analog signal and the ramp signal. However, calculating the natural crosspoints for NPWM in the digital domain based on PCM input data can be computationally expensive.

Super Audio Compact Disc (SACD) is a new digital audio data format. The audio is digitized and stored in Pulse Density Modulation (PDM) format. It consists of an oversampled ($64 \cdot F_s$, where F_s is the initial sampling rate) one-bit PDM data stream. It is desirable to convert the SACD bit stream (or any PDM bit stream) to a Pulse Width Modulated (PWM) signal that can be used to drive a highly efficient switching digital audio amplifier. The SACD PDM bit stream can be directly used as a switching signal; however this approach does not readily allow for the implementation of any desired signal processing (i.e. volume control, equalization, and the like).

Pulse density modulated signals (such as SACD) are typically noise shaped in order to push the quantization noise out of the frequency band of interest. This results in a frequency spectrum that contains a large amount of out-of-band noise.

A very high-end switching digital audio amplifier for SACD input has been commercially introduced. However, in order to accommodate volume control it cannot directly amplify the SACD PDM signal. Instead, it must treat the PDM input signal as an analog signal that can be attenuated as desired for volume control. This signal then feeds a seventh-order one-bit sigma delta ADC modulator that generates a new PDM signal for amplification in a switching amplifier. A big drawback of this system is that the signal does not stay in the digital domain. The digital input signal is converted to analog to allow signal processing in the analog domain, then converted to digital (PDM) to drive a switching amplifier. All the advantages of maintaining a digital signal line-up are lost. Additionally, the use of a PDM signal to drive a switching amplifier has some disadvantages compared to using a PWM signal. For example, PWM has a lower average switching frequency, which

results in greater efficiency compared to PDM. Furthermore, the non-return-to-zero (NRZ) nature of the PDM signal can result in increased distortion compared to the return-to-zero PWM signal. One might consider processing the high-speed one-bit PDM signal in the digital domain (volume control, equalization, etc.) followed by a digital sigma delta modulator. However, processing at such a high bit rate would be extremely costly.

Many common approaches of SACD demodulation and amplification consist of decimating the high sample rate PDM to a low sample rate PCM, performing signal processing, performing digital to analog conversion, and amplifying in the analog domain. A significant drawback to this approach is that all advantages of high efficiency digital switching amplification are lost.

Therefore, a computationally efficient method is desirable to convert both PDM and PCM encoded input signals to a PWM switching waveform entirely in the digital domain in order to advantageously drive a switching digital power amplifier. This method should be tolerant of out-of-band noise as typically found with PDM signals.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements.

FIG. 1 illustrates one embodiment of a digital to analog conversion system in accordance with the present invention.

FIG. 2 illustrates another embodiment of a digital to analog conversion system in accordance with the present invention.

FIG. 3 illustrates one embodiment of a PCM to PWM converter in accordance with the present invention.

FIG. 4 illustrates several signals used in natural sampling circuitry in accordance with the present invention.

5 FIG. 5 illustrates one embodiment of a timing diagram for two sided PWM signals.

FIG. 6 illustrates in flow chart form the functionality carried out by natural sampling circuitry in accordance with one embodiment of the present invention.

10 FIG. 7 is a block diagram illustrating a General Purpose Computer used to implement one embodiment of the present invention.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn
15 to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description

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FIG. 1 illustrates one embodiment of a digital to analog conversion system 10. In one embodiment of the present invention digital to analog conversion system 10 receives a pulse density modulated (PDM) signal 24 as an input to PDM to PWM converter 20.
25 PDM to PWM converter 20 then provides a pulse width modulation (PWM) signal 30 to low pass filter 18. Low pass filter 18 provides an analog signal as an output to a load 22 (not shown). In one embodiment load 22 may be an audio speaker. Other embodiments of the present

invention may use other types of loads. In one embodiment of the present invention PDM to PWM converter 20 includes a decimation filter 12, digital signal conditioning circuitry 14, and a PCM to PWM converter 16. In one embodiment decimation filter 12 receives PDM signal 24 as an input and provides pulse code modulated (PCM) signal 26 as an output. Note that PDM signal 24 has a one-bit resolution at a high sample rate. Decimation filter 12 decreases the sample rate and increases the bit resolution resulting in a pulse code modulation (PCM) signal 26. Digital signal conditioning circuitry 14 receives PCM signal 26 as an input and provides a conditioned PCM signal 28 as an output. PCM to PWM converter 16 receives the conditioned PCM signal 28 as an input and provides the PWM signal 30 as an output to low pass filter 18. Note that alternate embodiments of the present invention may optionally include an amplifier as part of digital to analog conversion system 10. For example, an amplifier (not shown) may optionally be included between converter 16 and low pass filter 18. Alternately an optional amplifier (not shown) may instead be included between low pass filter 18 and load 22. Note that alternate embodiments of the present invention may combine the functionality of decimation filter 12 and digital signal conditioning circuitry 14 in any way. What is important is that the functionality of circuits 12 and 14 receive a PDM signal 24 as an input and provide a conditioned PCM signal as an output. The digital signal conditioning that is performed by digital signal conditioning circuitry 14 may vary significantly. For example, some embodiments of the present invention may use digital signal conditioning circuitry 14 to provide volume control, graphic equalization, and any other desired digital effects or processing.

Alternatively, the digital signal conditioning may be performed before the decimation filter function.

FIG. 2 illustrates one embodiment of a digital to analog conversion system 110. In one embodiment of the present invention, digital to analog conversion system 110 receives a pulse code modulated (PCM) signal 124 as an input to PCM to PWM converter 120. PCM to PWM converter 120 then provides a pulse width modulation (PWM) signal 130 to low pass filter 118. Low pass filter 118 provides an analog signal as an output to a load 122 (not shown). In one embodiment load 122 may be an audio speaker. Other embodiments of the present invention may use other types of loads. In one embodiment of the present invention PCM to PWM converter 120 includes over sampling circuitry 112, digital signal conditioning circuitry 114, and a PCM to PWM converter 116. In one embodiment, over sampling circuitry 112 receives PCM signal 124 as an input and provides over sampled pulse code modulated (PCM) signal 126 as an output. Digital signal conditioning circuitry 114 receives over sampled pulse code modulated (PCM) signal 126 as an input and provides a conditioned PCM signal 128 as an output. PCM to PWM converter 116 receives the conditioned PCM signal 128 as an input and provides the PWM signal 130 as an output to low pass filter 118. Note that alternate embodiments of the present invention may optionally include an amplifier as part of digital to analog conversion system 110. For example, an amplifier (not shown) may optionally be included between converter 116 and low pass filter 118. Alternately an optional amplifier (not shown) may instead be included between low pass filter 118 and load 122. Note that alternate embodiments of the present invention may combine the functionality of over sampling circuitry 112 and digital signal conditioning circuitry 114

in any way. What is important is that the functionality of circuits 112 and 114 receive a PCM signal 124 as an input and provide a conditioned PCM signal as an output. The digital signal conditioning that is performed by digital signal conditioning circuitry 114 may vary significantly. For example, some embodiments of the present invention may use digital signal conditioning circuitry 114 to provide volume control, graphic equalization, and any other desired digital effects or processing. Alternatively, the digital signal conditioning may be performed before the over sampling circuitry function.

FIG. 3 illustrates one embodiment of a PCM to PWM converter 16 illustrated in FIG. 1 and a PCM to PWM converter 116 illustrated in FIG. 2. Note that although the PCM to PWM converter 16, 116 are both being illustrated by FIG. 3, alternate embodiments of digital to analog conversion system 10 illustrated in FIG. 1 and digital to analog conversion system 110 illustrated in FIG. 2 may use different embodiments of the PCM to PWM converter 16, 116. Note that for FIG. 3, optional circuitry and connections have been illustrated using dashed lines. In one embodiment PCM to PWM converter 16, 116 includes natural sampling circuitry 40 and PWM quantizer and noise shaper 42. In one embodiment, natural sampling circuitry 40 receives a conditioned PCM signal (U) 28, 128 as an input and provides natural sample point output (X) 57 as an output. PWM quantizer and noise shaper 42 receives natural sample point output (X) 57 as an input and provides PWM signal 30, 130 as an output. In one embodiment of the present invention natural sampling circuitry 40 includes duty ratio predictor 44, signal value interpolator 46, and correction of duty ratio circuitry 48. In one embodiment of the present invention, duty ratio predictor 44 receives conditioned PCM signal (U) 28, 128 as an input

signal and provides time point guess (G) 50 as an output. Signal value interpolator 46 receives time point guess (G) 50 as an input signal and provides interpolated signal value (V) 52 as an output. Correction of duty ratio circuitry 48 receives interpolated signal value (V) 52 as an input and provides natural sample point output (X) 57 as an output. In one embodiment of the present invention, the natural sample point output (X) 57 is provided as feedback to the duty ratio predictor 44 as a previous natural sample point output (X) 58. Also, in some embodiments of the present invention, the natural sample point output (X) 57 is fed back as updated time point guess (G) 56 input to signal value interpolator 46. Also, in some embodiments of the present invention, the interpolated signal value (V) 52 is fed back as updated time point guess (G) 59. Note that the feedback paths 56, 58 and 59 are optional and may or may not be included in various embodiments of the present invention. Note also that the duty ratio predictor 44 is optional. Some embodiments of the present invention may directly provide the conditioned PCM signal (U) 28, 128 to signal value interpolator 46. Note that the time point guess (G) 50 signal is also provided as an input to the correction of duty ratio circuitry 48. Note that the conditioned PCM signal (U) 28, 128 is also provided as an input to the signal value interpolator 46 and the correction of duty ratio circuitry 48. Note that if the duty ratio predictor 44 is not used, then the time point guess (G) signal 50 is merely the same as the conditioned PCM signal (U) 28, 128. The input to the PWM quantizer and noise shaper 42 is a natural sample point output (X) 57 which is a high resolution PWM signal. Thus, PWM quantizer and noise shaper 42 quantizes this high resolution PWM signal to produce a lower resolution quantized PWM signal 30,

130. In one embodiment, the noise shaping function of circuitry 42 shapes the quantization noise outside the pass band.

Still referring to FIG. 3, in one embodiment of the present invention, the addition of the correction of duty ratio circuitry 48 may greatly increase the accuracy of the natural sample point output (X) signal 57 which is generated by converter 16, 116. In fact, the addition of correction of duty ratio circuitry 48 to converter 16, 116 may allow the duty ratio predictor 44 to be eliminated entirely for some applications. However, alternate embodiments of the present invention may use a combination of correction of duty ratio circuitry 48 and duty ratio predictor circuitry 44. The addition of the correction of duty ratio circuitry 48 may reduce the number of calculations and the amount of memory required by converter 16, 116. The addition of correction of duty ratio circuitry 48 also greatly improves the distortion performance of the natural sample point output (X) signal 57, and thus also the distortion performance of PWM signal 30, 130. In addition, the correction of duty ratio circuitry 48 produces a natural sample point output (X) signal 57 which is less sensitive to out-of-band noise. This is especially important because PDM signal 24 (see FIG. 1) normally has a significant amount of out-of-band noise.

FIG. 4 illustrates a time domain representation of some of the signals used and/or generated in natural sampling circuitry 40 (see FIG. 3) in which a single sided PWM signal is generated by using a saw tooth shaped ramp signal 81. Alternate embodiments of the present invention may use a ramp other than a saw tooth shape. For example, FIG. 5 illustrates one embodiment of a timing diagram for a two-sided PWM signal with a symmetric triangular shaped ramp signal 90. The left half of the ramp signal 90 is when the ramp is rising and the right half of the

ramp signal 90 is when the ramp is falling. The individual samples of conditioned PCM signal (U) 28, 128 are chosen to line up with the centers of the ramp signal 81 or the ramp signal 90. Theoretical analog signal 80 and theoretical analog signal 91 represent the ideal analog
5 signal corresponding to the samples of conditioned PCM signal (U) 28, 128. A two sided example PWM signal 30, 130 is illustrated in FIG. 5. The conditioned PCM signal (U) 28, 128 is chosen to have even time indices during the left half while the odd indices line up with the right half of the PWM signal 30, 130.

10 Referring to FIG. 3 and FIG. 4, the time point guess (G) signal 50 is used to compute the value of the interpolated signal value (V) 52 using the conditioned PCM (U) signal 28, 128. Interpolated signal value (V) 52 is not equal to the time point guess (G) 50 unless all error is eliminated. The difference (V-G) is multiplied with the estimated signal
15 slope (S) of theoretical analog signal 80 to compute a correction (C) 82. The natural sample point output (X) signal 57 is the corrected signal. Note that for one embodiment of the present invention, the ramp signal 81 was chosen to rise linearly between 0 and 1.

FIG. 6 illustrates, in flow chart form, the functionality carried out
20 by one embodiment of natural sampling circuitry 40 of FIG. 3. In one embodiment, flow 199 begins as start oval 200 and proceeds to step 203 where a guess time (G) is provided. Step 203 provides a guess time (G) which is based on the conditioned PCM samples and/or the previously calculated natural sample point output (X). Flow 199 then proceeds to
25 step 204 where the interpolated signal value (V) at the time point guess (G) is digitally computed based on the conditioned PCM signal (U). Flow 199 then continues with decision diamond 202 where the determination is made as to whether it is necessary to repeat step 204

using the interpolated signal value (V) as a next time point guess (G). Note the decision diamond 202 may be used to repeat step 204 N times, where N is an integer greater than or equal to zero. Thus, if N equals 0, step 204 is executed only once and no recursive looping occurs. Note

5 that step 205 merely indicates that step 204 will use the interpolated signal value (V) as a next time point guess (G). After repeating step 204 N times, flow 199 continues at step 206 where a correction (C) based on the most recent interpolated signal value (V) and the most recent time point guess (G) and estimated signal slope (S) are created. From step

10 206 flow 199 continues at step 207 where the correction (C) is combined with the most recent interpolate signal value (V) to generate a natural sample point output (X). From step 207, flow 199 continues at step 208 where the entire flow of 199 is repeated for each sample of conditioned PCM signal (U). From step 208, flow 199 continues at oval 201 where

15 flow 199 ends. In alternate embodiments of the present invention, steps 206 and 207 may be moved to before decision diamond 202 so that steps 206 and 207 are repeated as part of the iterative recursion loop. Note that for some embodiments of the present invention, the number used for N in decision diamond 202 may be a function of one of the values used

20 in flow 199. For example, the value N in decision diamond 202 may be a function of the correction value (C). Note that alternate embodiments of the present invention may use any appropriate method to provide a time point guess (G) as required by step 203. One example of a method for providing a time point guess (G) is described in U.S. patent

25 application serial number 09/478,024, Pallab Midya et al., filed January 5, 2000.

It can be shown that for a given order of interpolation, the flow described in FIG. 6 which is performed by converter 16, 116 generates a

natural sample point output (X) which is nearly optimal compared to the ideal natural sample point for that order.

A mathematical description of one embodiment of the invention will be given using the following variables:

- 5 Sample index n
- Conditioned PCM signal $U(n)$ 28,128
- Time point guess $G(n)$ 50
- Interpolated signal value $V(n)$ 52
- Correction signal $C(n)$ 82
- 10 Natural sample point output $X(n)$ 57
- Time point guess for natural sampling at the first iteration: $G_1(n)$
- Interpolated signal value obtained by interpolation at the sample point at the first iteration: $V_1(n)$
- Correction to the signal value at the first iteration: $C_1(n)$
- 15 Natural sample point output at the first iteration: $X_1(n)$
- Time point guess for natural sampling at the second iteration: $G_2(n)$
- Interpolated signal value obtained by interpolation at the sample point at the second iteration: $V_2(n)$
- 20 Correction to the signal value at the second iteration: $C_2(n)$
- Natural sample point output at the second iteration: $X_2(n)$

The first step is to determine an initial time point guess (G) 50. In its most general form, it is derived from a combination of previous, present and future samples of conditioned PCM signal (U) 28, 128 as well as past-calculated samples of natural sample point output (X) 57. Example cases are as follows.

$$G(n) = U(n) + [2\{X(n-1) - U(n-1)\} - \{X(n-2) - U(n-2)\}] \quad [1]$$

or

$$G(n) = U(n) + \{X(n-1) - U(n-1)\} \quad [2]$$

or

$$5 \quad G(n) = U(n) \quad [3]$$

The interpolated signal value (V) 52 of the theoretical analog signal 80, 91 at the guess time point is computed based on an interpolation formula. It is observed that for some embodiments of the present invention, better accuracy may be achieved when the uniform samples of conditioned PCM signal (U) 28, 128 are lined up with the center of the ramps 81, 90. Using this approach for two sided PWM (see FIG. 5), the interpolated signal value (V) 52 for the left sided PWM case can be calculated as follows.

15

$$v(2n) = U(2n) + \left\{ G(2n) - \frac{1}{2} \right\} \left\{ \frac{U(2n+1) - U(2n-1)}{2} \right\} + \left\{ \frac{U(2n+1) + U(2n-1) - 2U(2n)}{2} \right\} \left\{ G(2n) - \frac{1}{2} \right\}^2 \quad [4]$$

For the right hand side a similar equation holds.

20

$$v(2n+1) = U(2n+1) + \left\{ \frac{1}{2} - G(2n+1) \right\} \left\{ \frac{U(2n+2) - U(2n)}{2} \right\} + \left\{ \frac{U(2n+2) + U(2n) - 2U(2n+1)}{2} \right\} \left\{ \frac{1}{2} - G(2n+1) \right\}^2 \quad [5]$$

Both of these equations are based on a three-point second order Lagrange interpolation formula. Other orders of Lagrange interpolation, as well as other types of interpolation formula, may be substituted based on accuracy and computational constraints.

5

The next step is the correction step. The correction step is based on the idea that if the time point guess (G) is close to the ideal natural sample time point, the value of the interpolated signal value (V) is very close to the ramp. Thus, the signal value (V) must be very close to the time point guess (G). Any difference implies that the time point guess (G) is not entirely accurate and can be corrected assuming that the signal is sufficiently slowly moving. A first order correction for both the left side PWM and the right side PWM, respectively, is given below.

$$C(2n) = \{V(2n) - G(2n)\} \left\{ \frac{U(2n+1) - U(2n-1)}{2} \right\} \quad [6]$$

$$C(2n+1) = \{V(2n+1) - G(2n+1)\} \left\{ \frac{U(2n+2) - U(2n)}{2} \right\} \quad [7]$$

In both cases the corrected natural sample point output is determined by simply summing the interpolated signal value and the correction signal value.

$$X(m) = V(m) + C(m) \quad [8]$$

The correction term improves accuracy. Recursion can be introduced to further improve accuracy. Typically, two iterations improve accuracy significantly. Recursion can be implemented by using the corrected natural sample point output as a new time point guess as
 5 given by the equations below.

$$V_1(2n) = U(2n) + \left\{ G_1(2n) - \frac{1}{2} \right\} \left\{ \frac{U(2n+1) - U(2n-1)}{2} \right\} + \left\{ \frac{U(2n+1) + U(2n-1) - 2U(2n)}{2} \right\} \left\{ G_1(2n) - \frac{1}{2} \right\}^2$$

[9]

$$10 \quad C_1(2n) = \{V_1(2n) - G_1(2n)\} \left\{ \frac{U(2n+1) - U(2n-1)}{2} \right\} \quad [10]$$

$$G_2(2n) = X_1(2n) = V_1(2n) + C_1(2n) \quad [11]$$

The steps in equations (9-11) can be repeated for improved
 15 accuracy. The amount of recursion needed to achieve a given accuracy is dependent on the oversampling ratio. If the signal is moving fast and changing significantly from sample to sample, corresponding to a low oversampling ratio, the need for recursion increases. This comes with added computational and memory requirements. The complexity of
 20 each of the time point estimation, interpolation to compute signal value, and correction of signal value steps are variable depending on the accuracy required. Depending on the accuracy requirement, as well as constraints on memory and computation, an optimal algorithm can be designed. As an example, for one embodiment of a digital audio
 25 amplifier system with an input signal constrained to 20 kHz bandwidth

and a 375 kHz PWM switching frequency, the following left hand side equations can be used to achieve extremely good results.

$$G(2n) = U(2n) \quad [12]$$

5

$$V(2n) = U(2n) + \left\{ U(2n) - \frac{1}{2} \right\} \left\{ \frac{U(2n+1) - U(2n-1)}{2} \right\} + \left\{ \frac{U(2n+1) + U(2n-1) - 2U(2n)}{2} \right\} \left\{ U(2n) - \frac{1}{2} \right\}^2 \quad [13]$$

$$X(2n) = V(2n) + \{V(2n) - G(2n)\} \left\{ \frac{U(2n+1) - U(2n-1)}{2} \right\} \quad [14]$$

10

The corresponding right hand side equations are as follows.

$$G(2n+1) = U(2n+1) \quad [15]$$

15

$$V(2n+1) = U(2n+1) + \left\{ \frac{1}{2} - U(2n+1) \right\} \left\{ \frac{U(2n+1) - U(2n-1)}{2} \right\} + \left\{ \frac{U(2n+2) + U(2n) - 2U(2n+1)}{2} \right\} \left\{ \frac{1}{2} - U(2n+1) \right\}^2 \quad [16]$$

$$X(2n+1) = V(2n+1) + \{V(2n+1) - G(2n+1)\} \left\{ \frac{U(2n+2) - U(2n)}{2} \right\} \quad [17]$$

20

Note that in this example the initial time point guess (G) 50 has been chosen to be the input conditioned PCM signal (U) 28, 128. Since

the conditioned PCM signal (U) 28, 128 is already available, there is no computation or memory storage associated with the guess. There are eleven multiply or add computations associated with the calculation of the interpolated signal value (V) 52. There are four memory storage
5 locations needed for this step. Calculation of the corrected natural sample point output requires an additional two add or multiply operations and uses one memory storage location. Thus, for this example, the total is thirteen operations and five memory storage locations needed per sample. For a 375 kHz switching frequency with
10 two samples per switching cycle, the total computation is 9.75 million operations per second. The low total memory requirement is particularly beneficial for reducing overall computation overhead.

Note that the direct translation from PCM to PWM is a non-linear operation which results in an unacceptable total harmonic distortion if a
15 converter such as PCM to PWM converter 16, 116 is not used. Note that the conversion process performed by PCM to PWM converter 16, 116 produces a highly linear output and thus does not add significant harmonic components to the PWM signal 30, 130. Also note that the conversion process performed by PCM to PWM converter 16, 116 is
20 highly tolerant to large amounts of shaped wide band noise often associated with pulse density modulated input signals such as SACD.

The addition of the correction of duty ratio circuitry 48 in FIG. 3 may result in a more efficient PCM to PWM converter 16, 116. This PCM to PWM converter 16, 116 can be used for both single and two
25 sided PWM signals. Referring to FIG. 6, the recursion which may be performed on one or more of steps 204, 206, and 207 allow the PCM to PWM converter 16, 116 to produce a more accurate PWM signal 30,

130 that has less harmonic distortion and approaches the theoretical limits of accuracy.

In one embodiment, the present invention is an all-digital architecture to take the new SACD audio format and convert it into a digital PWM signal for driving a highly efficient digital switching amplifier. Note that this architecture easily accommodates the handling of volume control, graphic equalization and other desired digital signal processing functions entirely in the digital domain. Thus, the architecture illustrated by the present invention maintains a complete digital path from the PDM input signal all the way to the amplified digital PWM output signal. However, although the present invention has been illustrated in the context of audio signal processing, it is important to note that the present invention is applicable to any type of digital signal processing application in which a pulse density modulated data stream or a pulse code modulated data stream is converted to a pulse width modulated signal. Audio signal processing is just one such application.

The PCM to PWM converter 16, 116 illustrated in FIG. 3 as well as the methodology described in FIG. 6 may be used for a wide variety of frequencies, including radio frequencies. For example, the disclosed circuitry and methodology may be used as part of a radio frequency amplifier.

FIG. 7 is a block diagram illustrating a General Purpose Computer 220 used to implement one embodiment of the present invention. General Purpose Computer 220 includes a Computer Processor 222 and Memory 224, connected by a Bus 226. Memory 224 is a relatively high speed machine-readable medium and includes Volatile Memories such as DRAM, and SRAM, and Non-Volatile

Memories such as, ROM, FLASH, EPROM, EEPROM, and bubble memory. Also connected to the Bus are Secondary Storage 230, External Storage 232, output devices such as monitor 234, input devices such as keyboard (with mouse) 236, printers 238, and one or more other computers 240 coupled by way of communication link 228. Secondary Storage 230 includes machine-readable media such as hard disk drives, magnetic drum, and bubble memory. External Storage 232 includes machine-readable media such as floppy disks, removable hard drives, magnetic tape, CD-ROM, and even other computers, possibly connected via a communications line. The distinction drawn here between Secondary Storage 230 and External Storage 232 is primarily for convenience in describing the invention. As such, it should be appreciated that there is substantial functional overlap between these elements. Computer software 233 including user programs can be stored in a Computer Software Storage Medium such as memory 224, Secondary Storage 230, and External Storage 232. Secondary Storage 230 and Non-Volatile Memory are loaded for execution directly into Volatile Memory, executed directly out of Non-Volatile Memory, or stored in Secondary Storage 230 prior to loading into Volatile Memory for execution.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary, as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims.

CLAIMS

1. A method for generating a pulse width modulated signal,
5 comprising:
receiving a modulated input signal (24) in a digital format,
the modulated input signal being in pulse density
modulation (PDM) form; and
converting (16) the modulated input signal to pulse width
10 modulated (PWM) form (30) to provide the pulse
width modulated signal (30), the converting being
performed entirely in a digital format.
2. The method of claim 1 wherein the converting further comprises:
15 decimating (12) the modulated input signal (24) to reduce a
sampling rate of the modulated input signal and to
increase resolution of the modulated input signal.
3. The method of claim 1 wherein the converting further comprises:
20 conditioning (14) the modulated input signal by modifying
at least one of amplitude and frequency response of
the modulated input signal.

4. The method of claim 1 wherein the converting further comprises for each of a plurality of predetermined samples:
- predicting (203) a natural sample time point for sampling the modulated input signal;
- 5 interpolating (204) the modulated input signal at the predicted natural sample time point to provide an interpolated signal value;
- providing a correction value (206) to correct error associated with the natural sample time point which
- 10 was predicted, the correction value provided by using the interpolated signal value, the natural sample time point which was predicted and an estimated signal slope value; and
- combining (207) the correction value and the interpolated
- 15 signal value to provide a corrected natural sample point output.
5. An apparatus (10) for generating a pulse width modulated signal, comprising:
- 20 an input terminal for receiving a modulated input signal (24) in a digital format, the modulated input signal being in pulse density modulation (PDM) form; and
- a converter (20) coupled to the input terminal, the converter converting the modulated input signal to pulse width
- 25 modulated form to provide the pulse width modulated signal (30), the converting being performed by the converter entirely in a digital format.

6. The apparatus of claim 5 wherein the converter (20) further comprises:

5 a decimation filter (12) coupled to the input terminal for decimating the modulated input signal to reduce a sampling rate of the modulated input signal and to increase resolution of the modulated input signal.

7. The apparatus of claim 5 wherein the converter further comprises:

10 digital signal conditioning circuitry (14) for conditioning the modulated input signal prior to converting the modulated input signal to pulse width modulated form.

15 8. The apparatus of claim 7 further comprising:

a filter (18) coupled to the digital signal conditioning circuitry for filtering the pulse width modulated signal to make the pulse width modulated signal suitable for driving a load by rejecting predetermined frequency components.

20

9. A method for generating a pulse width modulated signal, comprising:

25 receiving a modulated input signal, the modulated signal being in either pulse code modulated (PCM) form (124) or pulse density modulated (PDM) form (24); converting the modulated input signal to pulse width modulated form to provide the pulse width

- modulated signal (30, 130), the converting being performed entirely in a digital format, the converting further comprising for each of a plurality of predetermined samples:
- 5 predicting (203) a natural sample time point for sampling the modulated input signal;
- interpolating (204) the modulated input signal at the natural sample time point to provide an interpolated signal value;
- 10 providing a correction value (206) to correct error associated with the natural sample time point which was predicted, the correction value provided by using the interpolated signal value, the natural sample time point which was
- 15 predicted and an estimated signal slope value; and
- combining the correction value (207) and the interpolated signal value to provide a corrected natural sample point output.
- 20
10. An apparatus (10, 110) for generating a pulse width modulated signal, the apparatus comprising:
- an input terminal for receiving a modulated input signal, the modulated signal being in either pulse code modulated (PCM) (124) form or pulse density
- 25 modulated (PDM) form (24); and
- a converter (16, 116) for converting the modulated input signal to pulse width modulated form to provide the

pulse width modulated signal, the converting being performed entirely in a digital format, the converter further comprising:

5 a duty ratio predictor (44) for predicting a natural sample time point for sampling the modulated input signal;

10 a signal value interpolator (46) coupled to the duty ratio predictor, the signal value interpolator interpolating the modulated input signal at the natural sample time point to provide an interpolated signal value; and

15 a correction circuit (48) coupled to the signal value interpolator, the correction circuit providing a correction value to correct error associated with the natural sample time point which was predicted, the correction value provided by using the interpolated signal value, the natural sample time point which was predicted and an estimated signal slope value, the correction
20 circuit combining the correction value and the interpolated signal value to provide a corrected natural sample point output.