CLAIMS

1. A high voltage logic circuit for high voltage system application comprising:

a first device layer formed from a first semiconductor material and comprising a low voltage logic circuit; and

a second device layer formed from a second semiconductor material different from the first semiconductor material and comprising one or more components of an additional circuit for generating a high voltage logic output from a low voltage logic input from the low voltage logic circuit;

wherein the first and second device layers are integrally formed.

2. The high voltage logic circuit of claim 1, wherein the first device layer comprises at least one component of the additional circuit, wherein the at least one component may comprise a bias circuit or at least one first tail transistor made from the first semiconductor material.

3. The high voltage logic circuit of claim 2, wherein the additional circuit does not require an additional biasing circuit for biasing of at least one second tail transistor of the additional circuit, wherein the at least one second tail transistor is made from the second semiconductor material.

4. The high voltage logic circuit of any one of claims 1 to 3, wherein the additional circuit comprises a logic inverter circuit or a NOR logic circuit.

5. The high voltage logic circuit of any one of claims 1 to 4, wherein the first semiconductor material comprises a silicon based material, and may comprise a group III-V based material.

6. A logic circuit comprising:

a low voltage logic input;

a high supply voltage input;

a circuit ground voltage input;

a high voltage output;

at least one first tail device made from a first semiconductor material, the first tail device comprising a first gate, wherein a voltage applied to the first gate controls a current flow through the first tail device; and

at least one second tail device made from a second semiconductor material different from the first semiconductor material, the second tail device comprising a second gate, wherein a voltage applied to the second gate controls a current flow through the second tail device;

wherein the at least one first and second tail devices are coupled, in series, between the high voltage output and the circuit ground voltage input; and

wherein the first and second gates of the at least one first and second tail devices, respectively, are coupled, in parallel, to the low voltage logic input.

7. The logic circuit of claim 6, further comprising a top device coupled between the high supply voltage input and the high voltage output.

8. The logic circuit of claim 6, wherein the top device is made from the second semiconductor material and/or wherein the top device has a small size for reducing an on-state current consumption of an inverter circuit of the logic circuit.

9. The logic circuit of any one of claims 6 to 8, wherein the logic circuit comprises a logic inverter circuit or a NOR logic circuit.

10. The logic circuit of any one of claims 6 to 9, wherein the first semiconductor material comprises a silicon based material, and may comprise a group III-V based material.

11. A method of fabricating a high voltage logic circuit for high voltage system application comprising:

providing a first device layer formed from a first semiconductor material and comprising a low voltage logic circuit; and

providing a second device layer formed from a second semiconductor material different from the first semiconductor material and comprising one or more components of an additional circuit for generating a high voltage logic output from a low voltage logic input from the low voltage logic circuit;

wherein the first and second device layers are integrally formed.

12. The method circuit of claim 11, wherein the first device layer comprises at least one component of the additional circuit, wherein the at least one component may comprise a bias circuit or at least one first tail transistor made from the first semiconductor material.

13. The method of claim 12, wherein the additional circuit does not require an additional biasing circuit for biasing of at least one second tail transistor of the additional circuit, wherein the at least one second tail transistor is made from the second semiconductor material.

14. The method of any one of claims 11 to 13, wherein the additional circuit comprises a logic inverter circuit or a NOR logic circuit.

15. The method of any one of claims 11 to 14, wherein the first semiconductor material comprises a silicon based material, and may comprise a group III-V based material.

16. A method of fabricating a logic circuit comprising:

providing a low voltage logic input;

providing a high supply voltage input;

providing a circuit ground voltage input;

providing a high voltage output;

providing at least one first tail device made from a first semiconductor material, the first tail device comprising a first gate, wherein a voltage applied to the first gate controls a current flow through the first tail device; and

providing at least one second tail device made from a second semiconductor material different from the first semiconductor material, the second tail device comprising a second gate, wherein a voltage applied to the second gate controls a current flow through the second tail device;

wherein the at least one first and second tail devices are coupled, in series, between the high voltage output and the circuit ground voltage input; and

wherein the first and second gates of the at least one first and second tail devices, respectively, are coupled, in parallel, to the low voltage logic input.

17. The method of claim 16, further comprising providing a top device coupled between the high supply voltage input and the high voltage output.

18. The method of claim 17, wherein the top device is made from the second semiconductor material and/or wherein the top device has a small size for reducing an on-state current consumption of an inverter circuit of the logic circuit.

19. The method of any one of claims 16 to 18, wherein the logic circuit comprises a logic inverter circuit or a NOR logic circuit.

20. The method of any one of claims 15 to 18, wherein the first semiconductor material comprises a silicon based material, and may comprise a group III-V based material.