

Semiconductor wafer composed of monocrystalline silicon

The present invention relates to a semiconductor wafer made of single-crystal silicon having a front side and a back side,
5 wherein the semiconductor wafer comprises a denuded zone which extends from the front side in the direction of the back side to a certain depth and a region which is adjacent to the denuded zone and contains BMD seeds.

10 A denuded zone is a region of the semiconductor wafer which extends from the front side in the direction of the back side over a certain depth and in which oxygen precipitates known as BMDs (bulk micro defects) are not formed. The denuded zone is typically intended as a location for accommodating electronic
15 components.

Adjacent to the denuded zone is a region which extends further into the interior (bulk) of the semiconductor wafer and contains BMD seeds. BMD seeds are developed into BMDs by means
20 of a heat treatment. BMDs act as so-called internal getters which in particular can bond metallic impurities. The development of BMD seeds into BMDs is also possible in the course of a heat treatment that is used primarily for construction of electronic components in the denuded zone.

25 It is known that the presence of vacancies in the single crystal is advantageous when comparatively high densities of BMDs are sought. US 2002/0170631 A1 describes a process for producing a semiconductor wafer of single-crystal silicon with
30 a deep denuded zone. The process comprises a heat treatment (RTA treatment, rapid thermal anneal) of the semiconductor wafer which includes a short-duration rapid heating and cooling of the semiconductor wafer. The RTA treatment is to be performed in an atmosphere containing oxygen in a concentration
35 of not less than 100 ppma and not more than 10,000 ppma. The

described process is moreover conceived so as to form a concentration profile of vacancies in which the peak density of vacancies is achieved in the middle between the front side and the back side of the semiconductor wafer or near to the middle. Since the concentration profiles of the vacancies, of the BMDs seeds and of the BMDs correlate the peak density of BMDs is likewise found in the middle or near to the middle.

The production of modern integrated circuits with 3-D architecture necessitates the provision of a denuded zone which extends comparatively deep into the semiconductor wafer and an adjoining region comprising BMD seeds which may be developed into BMDs, wherein the distance between the BMDs and the denuded zone should be as small as possible. One known procedure comprises through silicon via (TSV) fabrication and grinding-back of the semiconductor wafer from the back side until far beyond the middle of the semiconductor wafer (M.Motoyoshi, Proceedings of the IEEE, Vol.97, No.1, January 2009). The proximity of the BMDs to the denuded zone is said to ensure that in the ground-back semiconductor wafer too there is a sufficient density of getter centers, in particular even during construction of structures of electronic components.

The present invention accordingly has for its object to provide a semiconductor wafer of single-crystal silicon which better fulfills the recited requirements.

The object is achieved by a semiconductor wafer of single-crystal silicon comprising a polished front side and a back side;

a denuded zone which extends from the polished front side toward the back side to a depth of not less than 30 μm ; and a region adjacent to the denuded zone and comprising BMD seeds which may be developed into BMDs, wherein a density of the BMDs

at a distance of 120 μm from the front side is not less than $2 \times 10^8 \text{ cm}^{-3}$.

The semiconductor wafer of single crystalline silicon is either
5 an uncoated semiconductor wafer or a semiconductor wafer coated
with at least one epitaxial layer. When the semiconductor wafer
of single-crystal silicon is coated with an epitaxial layer the
upper surface of the epitaxial layer forms the front side of
the semiconductor wafer. The at least one epitaxial layer
10 preferably has a thickness of not less than 1 μm and not more
than 5 μm .

In a first preferred embodiment of the invention the
semiconductor wafer of single-crystal silicon is an uncoated
15 substrate wafer of single-crystal silicon whose denuded zone
extends from the polished front side to a depth of not less
than 45 μm , wherein the semiconductor wafer in the region
adjacent to the denuded zone comprises BMD seeds after whose
development into BMDs, the density of the BMDs at a distance of
20 120 μm from the front side is not less than $3 \times 10^9 \text{ cm}^{-3}$.

In a second preferred embodiment of the invention the
semiconductor wafer of single-crystal silicon is a substrate
wafer of single-crystal which is coated with at least one
25 epitaxial layer of single-crystal silicon and whose denuded
zone extends from the polished front side of the coated
substrate wafer to a depth of not less than 45 μm , wherein the
semiconductor wafer in the region adjacent to the denuded zone
comprises BMD seeds after whose development into BMDs, the
30 density of the BMDs at a distance of 120 μm from the front side
is not less than $3 \times 10^9 \text{ cm}^{-3}$.

The at least one epitaxial layer has a thickness of preferably
not less than 1 μm and not more than 5 μm . The semiconductor
35 wafer of the second preferred embodiment of the invention is

preferably an epitaxially coated substrate wafer with n/n^- doping or p/p^- doping. The dopant of the n-type is preferably phosphorous and the dopant of the p-type is preferably boron.

5 In a third preferred embodiment of the invention the semiconductor wafer of single-crystal silicon is an uncoated substrate wafer of single-crystal silicon whose denuded zone extends from the polished front side to a depth of not less than 30 μm , wherein the semiconductor wafer in the region
10 adjacent to the denuded zone comprises BMD seeds after whose development into BMDs, the density of the BMDs at a distance of 120 μm from the front side is not less than $2 \times 10^8 \text{ cm}^{-3}$. Producing a semiconductor wafer of the third embodiment of the invention requires a comparatively small number of process
15 steps.

An inventive semiconductor wafer of single-crystal silicon comprises in a region below the denuded zone BMD seeds which may be developed into BMDs. It is preferable when the density
20 of developed BMDs decreases from a peak density in the direction of the central plane. The semiconductor wafer of single-crystal silicon may be ground back to a residual thickness from the back side while preferably retaining the region in which the peak density of BMDs may be developed.

25 In the denuded zone the lifetime of minority charge carriers is preferably greater than 1000 μs on average.

The back side of an inventive semiconductor wafer of single-crystal silicon is preferably burdened with not more than 100
30 defects.

The production of a semiconductor wafer of the first preferred embodiment of the invention comprises the following process
35 steps:

providing a substrate wafer of single-crystal silicon;
polishing the substrate wafer by DSP;
loading an RTA reactor with the substrate wafer;
a first RTA treatment of the substrate wafer at a temperature
5 in a temperature range of not less than 1275°C and not more
than 1295°C for a period of not less than 15 s and not more
than 30 s in an atmosphere consisting of argon and oxygen
having a proportion of oxygen of not less than 0.5 vol% and not
more than 2 vol%;
10 cooling the substrate wafer after the first RTA treatment to a
temperature of not more than 800°C, wherein a gas feed to the
semiconductor wafer is reset to 100 vol% argon;
a second RTA treatment of the substrate wafer at a temperature
in a temperature range of not less than 1280°C and not more
15 than 1300°C for a period of not less than 20 s and not more
than 35 s in an atmosphere consisting of argon;
removing an oxide layer from a front side of the semiconductor
wafer; and
polishing the front side of the substrate wafer by CMP.

20

DSP (double side polishing) is a polishing procedure in the
course of which the front side and the back side of a substrate
wafer are polished simultaneously.

25 CMP (chemical mechanical polishing) is a polishing procedure in
the course of which the front side or the back side of a
substrate wafer is polished.

The oxide layer present on the substrate wafer after the first
30 RTA treatment is removed from the front side of the substrate
wafer, preferably by treating the substrate wafer with aqueous
HF solution. The aqueous HF solution preferably contains not
less than 0.5% by weight of HF and not more than 2% by weight
of HF and the duration of the treatment is preferably not less
35 than 150 s and not more than 350 s.

The production of a semiconductor wafer of the second preferred embodiment of the invention comprises the following process steps:

- 5 providing a substrate wafer of single-crystal silicon;
polishing the substrate wafer by DSP;
polishing the front side of the substrate wafer by CMP;
depositing at least one epitaxial layer of single-crystal
silicon on the front side of the substrate wafer;
- 10 loading an RTA reactor with the coated substrate wafer;
a first RTA treatment of the coated substrate wafer at a
temperature in a temperature range of not less than 1275°C and
not more than 1295°C for a period of not less than 15 s and not
more than 30 s in an atmosphere consisting of argon and oxygen
15 having a proportion of oxygen of not less than 0.5 vol% and not
more than 2 vol%;
cooling of the coated substrate wafer after the first RTA
treatment to a temperature of not more than 800°C, wherein a
gas feed to the semiconductor wafer is reset to 100 vol% argon;
- 20 a second RTA treatment of the coated substrate wafer at a
temperature in a temperature range of not less than 1280°C and
not more than 1300°C for a period of not less than 20 s and not
more than 35 s in an atmosphere consisting of argon;
removing an oxide layer from a front side of the coated
25 substrate wafer; and
polishing the front side of the coated substrate wafer by CMP.

- The oxide layer present on the coated substrate wafer after the first RTA treatment is removed from the front side of the
- 30 coated substrate wafer, preferably by treating the coated
substrate wafer with aqueous HF solution. The aqueous HF
solution preferably contains not less than 0.5% by weight of HF
and not more than 2% by weight of HF and the duration of the
treatment is preferably not less than 150 s and not more than
35 350 s.

The deposition of the at least one epitaxial layer on the substrate wafer is preferably carried out by CVD (chemical vapor deposition) and preferably in a single wafer reactor, for example such as is described in US 2010/0213168 A1. A preferred deposition gas contains trichlorosilane as the silicon source. The deposition temperature is then preferably not less than 1110°C and not more than 1180°C, particularly preferably 1130°C. Furthermore, the deposition gas preferably contains a dopant of the n-type or of the p-type.

The production of a semiconductor wafer of the third preferred embodiment of the invention comprises the following process steps:

- providing a substrate wafer of single-crystal silicon;
- loading an RTA reactor with the substrate wafer;
- a first RTA treatment of the substrate wafer at a temperature in a temperature range of not less than 1250°C and not more than 1310°C for a period of not less than 5 s and not more than 40 s in an atmosphere consisting of nitrogen and oxygen having a proportion of oxygen of not less than 0.5 vol% and not more than 3.0 vol%;
- cooling the substrate wafer after the first RTA treatment to a temperature of not more than 800°C, wherein a gas feed to the substrate wafer is reset to 100 vol% argon;
- a second RTA treatment of the substrate wafer at a temperature in a temperature range of not less than 1280°C and not more than 1300°C for a period of not less than 20 s and not more than 35 s in an atmosphere consisting of argon;
- polishing the substrate wafer by DSP; and
- polishing the front side of the substrate wafer by CMP.

The oxide layer present on the substrate wafer after the first RTA treatment is removed from the front side of the substrate wafer by polishing the substrate wafer by DSP. The thus

achieved material removal from the front side and the back side of the substrate wafer is preferably not less than 8 μm in each case.

5 The step of providing a substrate wafer of a single crystalline silicon is a step recited at the beginning of the production processes described. The substrate wafer is preferably cut from a single crystal of single-crystal silicon pulled by the CZ method and subjected to further processing. In the CZ method
10 silicon is melted in a crucible made of quartz and the single-crystal grows at the end of a seed crystal which is immersed in the resulting melt and raised. The crucible material is partially dissolved by contact with the melt and in this way provides oxygen later required for developing BMDs.

15 The single crystal of single-crystal silicon preferably has a diameter of not less than 300 mm. The substrate wafer cut from the single crystal preferably originates from n region. N region describes single crystal silicon which contains neither
20 agglomerates of vacancies nor agglomerates of silicon interstitial atoms nor OSF defects (oxidation induced stacking faults). Such material is formed for example when the single-crystal is pulled according to the CZ method and the V/G ratio of pulling speed V and axial temperature gradient G at the
25 crystallization boundary is controlled such that it remains between critical limits.

The single-crystal from which the provided substrate wafer of single-crystal silicon is cut is preferably not intentionally
30 doped with nitrogen or carbon. Accordingly the provided substrate wafer of single-crystal silicon contains nitrogen in a concentration of preferably not more than 3×10^{12} atoms/cm³ and carbon in a concentration of preferably not more than 2.5×10^{15} atoms/cm³. The concentration of oxygen in the provided
35 substrate wafer is preferably not less than 4.5×10^{17} atoms/cm³

and not more than 5.5×10^{17} atoms/cm³, taking account of the calibration factor as per new ASTM.

The substrate wafer cut from the single-crystal may be
5 subjected to further processing using mechanical and chemical
processing steps such as grinding and etching. It is preferable
to provide a substrate wafer of single-crystal silicon which
has been subjected to at least one material-removing processing
operation, wherein the last material-removing treatment carried
10 out before providing the substrate wafer is preferably a
treatment by etching.

The provided and optionally epitaxially coated substrate layer
of single-crystal silicon is loaded into an RTA reactor and in
15 the course of the first RTA treatment preferably heated to the
target temperature at a rate of not less than 50°C/s.

Following the first RTA treatment the provided and optionally
epitaxially coated substrate layer remains in the RTA reactor
20 and is cooled, preferably to a temperature of not more than
800°C. The cooling rate is preferably not less than 30°C/s. The
gas feed into the RTA reactor is simultaneously switched to
100% argon.

25 The provided and optionally epitaxially coated substrate layer
of single-crystal silicon is in the course of the second RTA
treatment preferably heated to the target temperature at a rate
of not less than 50°C/s.

30 The period between the end of the first RTA treatment and the
beginning of the second RTA treatment is preferably not less
than 25 s and not more than 50 s.

Burdening of a semiconductor wafer according to the invention
35 (according to the first, second and third embodiment) with

defects is preferably curtailed by passing oxygen (100 vol%) through the RTA reactor prior to the first RTA treatment, preferably with a flowrate of not less than 8 slm and not more than 18 slm (standard liters per minute). The defect burden of the semiconductor wafer may be analysed using a high-resolution laser scattering system for example. Analysis results contained herein were obtained in part using an edge and back side inspection module (EBI) from Rudolph Technologies which allows for determination of defects such as particles, scratches, surface defects and haze on the back side and in part with a KLA Tencor Surfscan SP3 inspection system which detects LLS defects (localized light scatterers) on the front side.

The inventive semiconductor wafer of single-crystal silicon comprises a region having BMD seeds which is located below the denuded zone and is adjacent to the denuded zone. BMD seeds are centres comprising vacancies where BMDs may develop after a precipitation heat treatment. The precipitation heat treatment is not a constituent of a process for producing a semiconductor wafer according to the invention but is necessary to test whether BMDs can be developed in the required density or to develop BMDs that exhibit their activity as getter centres. The precipitation heat treatment is accordingly performed either as a test or preferably in the course of a further processing of the semiconductor wafer of single-crystal silicon into electronic components.

A typical precipitation heat treatment for test purposes consists of a two-stage precipitation heat treatment of the semiconductor wafer according to the invention under oxygen at a temperature of 780°C for a duration of 3 h (stage 1, stabilization step) and at a temperature of 1000°C for a duration of 16 h (stage 2, growth step).

The density of the developed BMDs may be determined along a broken edge of the semiconductor wafer for example by IR laser scattering tomography as the analytical method using an MO-441 detector from Raytex Corporation, Japan. Evaluation of the measured results is typically performed by plotting in a diagram the average density of BMDs (D_{BMD}) along the radius of the semiconductor wafer (averaged over a depth of 7-300 μm at each radial position of measurement, wherein the BMD defect density is measured every 5 μm in the depth axis) for example at at least 25 radial positions of measurement P which are equidistant from one another. Also determined at the radial positions of measurement P is the distance DZ1 from the first encountered BMD to the front side, this distance being plotted in a diagram along the radius of the semiconductor wafer. The arithmetic average of the distances DZ1 represents the depth to which the denuded zone extends from the polished front side into the interior of the semiconductor wafer. Also plottable in a diagram is the average size s_{av} of BMDs (measured over a depth of 7-300 μm at each radial position of measurement, the BMD defect size being measured in the depth axis every 5 μm) as a function of the radial position of measurement P and also the profile of the density of BMDs (D_{BMD}) in the depth direction, i.e. along the distance d to the front side of the semiconductor wafer, based on a particular radial position of measurement P.

The invention is further elucidated hereinbelow with the aid of examples and with reference to drawings.

30

Substrate wafers of single-crystal silicon having a diameter of 300 mm were provided. The substrate wafers consisted of n region and had surfaces in an etched state. A first portion of the substrate wafers was subjected to the process according to

the invention for producing semiconductor wafers according to the first preferred embodiment.

Prior to the first RTA treatment oxygen (100 vol%)
5 was passed through the RTA reactor at a flowrate of 10 slm. The first RTA treatment was then undertaken at a temperature of 1290°C in an atmosphere of argon and oxygen (oxygen proportion 1 vol%). The duration of the first RTA treatment at this temperature was 20 s. The substrate wafers were subsequently
10 cooled to a temperature of 600°C and held at this temperature over a period of 40 s while the gas feed to the semiconductor wafers was switched to 100% argon. This was followed by the second RTA treatment at a temperature of 1295°C and in an argon atmosphere over a period of 30 s.

15 The oxide layer formed was then removed from the substrate wafers and the front sides of the substrate wafers polished by CMP. The resulting semiconductor wafers according to the first embodiment of the invention were subjected to the two-stage
20 precipitation heat treatment provided for test purposes.

A second portion of the substrate wafers was subjected to the process according to the invention for producing semiconductor wafers according to the third preferred embodiment.

25 Prior to the first RTA treatment oxygen (100 vol%) was passed through the RTA reactor at a flowrate of 10 slm. The first RTA treatment was then undertaken at a temperature of 1290°C in an atmosphere composed of nitrogen and oxygen (oxygen
30 proportion 1 vol%). The duration of the first RTA treatment at this temperature was 20 s. The substrate wafers were subsequently cooled to a temperature of 600°C and held at this temperature over a period of 40 s while the gas feed to the semiconductor wafers was switched to 100% argon.

This was followed by the second RTA treatment at a temperature of 1295°C and in an argon atmosphere over a period of 30 s.

The substrate wafers were subsequently polished initially by DSP and then by CMP and the resulting semiconductor wafers according to the third embodiment of the invention were likewise subjected to the two-stage precipitation heat treatment provided for test purposes.

Fig.1 and Fig.2 respectively show the radial profile of the average density D_{BMD} of BMDs using the example of representatives of semiconductor wafers of the first embodiment (Fig.1) and of the third embodiment (Fig.2).

Fig.3 and Fig.4 respectively show the radial profile of the distance $DZ1$ using the example of representatives of semiconductor wafers of the first embodiment (Fig.3) and of the third embodiment (Fig.4) with a corresponding depth of the denuded zone of not less than 45 μm (Fig.3) and of not less than 30 μm (Fig.4).

Fig.5 and Fig.6 respectively show the average size s_{av} of the BMDs as a function of their radial position using the example of representatives of semiconductor wafers of the first embodiment (Fig.5) and of the third embodiment (Fig.6).

Fig.7 to Fig.12 respectively show a depth profile of the density D_{BMD} of BMDs using the example of representatives of semiconductor wafers of the first embodiment (Fig.7, Fig.8 and Fig.9) and of the third embodiment (Fig.10, Fig.11 and Fig.12), wherein the depth profile in the center ($P = 0 \text{ mm}$; Fig.7 and Fig.10), at half radius ($P = 75 \text{ mm}$; Fig.8 and Fig.11) and at the radial distance $P = 140 \text{ mm}$ (Fig.9 and Fig.12) was determined.

Fig.13 and Fig.14 show analysis results obtained after analysis of the back sides of representatives of the semiconductor wafers with the abovementioned edge and back side inspection module (EBI). Fig.13 shows a typical defect burden of the back side of an inventive semiconductor wafer of 8 defects greater than 0.2 μm and less than 100 defects, wherein during production of the semiconductor wafer care was taken to ensure that pure oxygen was passed through the RTA reactor at a flowrate of 10 slm prior to the first RTA treatment. If the passing of oxygen through the reactor is dispensed with the defect burden of the back side is markedly greater and annular defect regions having high defect densities are detectable (Fig.14) (all defects larger than 0.2 μm were in turn measured and depicted). On the other hand it is not advantageous to set the flowrate of the oxygen to values of for example 25 slm prior to the first RTA treatment. In this case the number of LLS defects having a latex sphere equivalent of $\geq 0.13 \mu\text{m}$ is unacceptably high. This is not the case when the flow rate of the oxygen is selected to fall within the range of not less than 8 slm and not more than 18 slm. Fig.15 shows this difference with reference to a box whisker plot, wherein the number N of LLS defects has been normalized. It is generally advantageous to recondition the oxidation state of the RTA reactor at regular intervals by running in the presence of wafer dummies. This is preferably carried out in an ambient of Ar/O₂ having an O₂ vol% proportion of 75-100% and a flow of 20-25 slm.

Claims

1. Semiconductor wafer of single-crystal silicon comprising a polished front side and a back side;
- 5 a denuded zone which extends from the polished front side toward the back side to a depth of not less than 30 μm ; and a region adjacent to the denuded zone and comprising BMD seeds which may be developed into BMDs, wherein a density of the BMDs at a distance of 120 μm from the front side is not less than 2
- 10 $\times 10^8 \text{ cm}^{-3}$.
2. Semiconductor wafer according to claim 1, wherein the denuded zone extends to a depth of not less than 45 μm and the region adjacent to the denuded zone comprises BMD seeds which
- 15 may be developed into BMDs, wherein the density of the BMDs at a distance of 120 μm to the front side is not less than $3 \times 10^9 \text{ cm}^{-3}$.
3. Semiconductor wafer according to claim 2 comprising an
- 20 epitaxial layer of single-crystal silicon, wherein an upper surface of the epitaxial layer forms the front side of the semiconductor wafer, thus increasing the depth to which the denuded zone extends by the magnitude of the thickness of the epitaxial layer.
- 25
4. Semiconductor wafer according to any of claims 1 to 3, wherein the back side of the semiconductor wafer is burdened with not more than 100 defects.