

SPECIFICATION

Title of Invention: INSPECTION SYSTEM AND TEMPERATURE CONTROL METHOD

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Technical Field

[0001]

The present disclosure relates to an inspection system and a temperature control method.

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Background

[0002]

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Patent Document 1 discloses a power conversion device capable of detecting an inter-terminal voltage between a source terminal and a drain terminal during an on-period of a power transistor and estimating a junction temperature of the power transistor with high accuracy.

Prior Art Documents

Patent Documents

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[0003]

Patent Document 1: Japanese Laid-open Patent Publication No. 2019-122107

Summary

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Problems to Be Resolved by the Invention

[0004]

In one aspect, the present disclosure provides an inspection system for inspecting a substrate while appropriately performing temperature control and a temperature control method.

5 **Means for Solving the Problems**

[0005]

To solve the problems, in one embodiment, an inspection system configured to inspect a substrate while performing temperature control using a temperature control mechanism is provided. The inspection system comprises a
10 substrate holder configured to hold the substrate, a detector configured to supply an inspection power to an electrode portion of the substrate, and a controller. The detector includes a temperature estimation part configured to estimate a junction temperature of a junction portion provided at the substrate. The controller includes
15 supplying the inspection power to the substrate, acquiring information on the junction temperature after the supply of the inspection power is stopped, determining an offset temperature of the substrate holder based on the information on the junction temperature, adjusting the temperature of the substrate holder based on a control temperature offset by the offset temperature, and supplying the inspection power to the substrate to inspect the substrate after the temperature of
20 the substrate holder is adjusted.

Effect of the Invention

[0006]

In one aspect, an inspection system for inspecting a substrate while
25 appropriately performing temperature control and a temperature control method can be provided.

Brief Description of the Drawings

[0007]

FIG. 1 is an example of a perspective view of an inspection system.

5 FIG. 2 is an example of a configuration diagram of an inspection system.

FIG. 3 is an example of a plan view schematically showing a configuration of a substrate.

FIG. 4 is an example of a flowchart explaining temperature control in an inspection system.

10 FIG. 5 is an example of a graph showing temporal transition of an inspection power and an offset temperature of an electronic device.

FIG. 6 is an example of a graph showing temporal transition of an inspection power and an offset temperature of an electronic device before and after the completion of the inspection of an electronic device.

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Detailed Description

[0008]

Hereinafter, various exemplary embodiments will be described in detail with reference to the accompanying drawings. Further, like reference numerals will be used for like or corresponding parts throughout the drawings.

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[0009]

An inspection system 1, which is an example of an inspection system according to the present embodiment, will be described with reference to FIG. 1. FIG. 1 is an example of a perspective view of the inspection system 1. FIG. 2 is an example of a configuration diagram of the inspection system 1. Further, FIG. 2 is a partial cross-sectional view schematically showing components in the

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inspection system 1.

[0010]

In a semiconductor manufacturing process, a plurality of electronic devices D (see FIG. 3 to be described later), each having a predetermined circuit pattern, are formed on a substrate W such as a semiconductor wafer or the like. Electrical characteristics of the electronic devices D formed on the substrate W are inspected and the electronic devices D are classified into non-defective products or defective products. The electronic devices D are inspected using the inspection system 1 before the substrate W is divided into the electronic devices D.

[0011]

The inspection system 1 inspects the electrical characteristics of the plurality of electronic devices D (see FIG. 3 to be described later) formed on the substrate W while controlling a temperature. In other words, in the inspection system 1, an inspection power is supplied to the electronic devices D when the temperature of the electronic devices D is higher than or equal to a predetermined inspection temperature, and the electrical characteristics of the electronic devices D at that time are inspected.

[0012]

The inspection system 1 includes an accommodating chamber 2, a loader 3, and a tester 4.

[0013]

The accommodating chamber 2 has a hollow housing 11. In the housing 11, the accommodating chamber 2 has a stage (also referred to as "chuck") 10 on which the substrate W is placed. The stage 10 has an attraction holding portion (not shown) that attracts and holds the substrate W to prevent displacement of the position of the substrate W with respect to the stage 10. In the housing 11, the

accommodating chamber 2 is provided with a moving mechanism (not shown) for moving the stage 10 in a horizontal direction and a vertical direction. The moving mechanism adjusts the relative positions of a probe card 12 to be described later and the substrate W, so that a desired electrode portion E (see FIG. 3 to be described later) on the surface of the substrate W can be brought into contact with probes 12a of the probe card 12.

[0014]

The probe card 12 is provided in the housing 11 of the accommodating chamber 2. The probe card 12 is located above the stage 10 to face the stage 10. The probe card 12 has the plurality of needle-shaped probes 12a arranged to correspond to electrode pads or solder bumps provided to correspond to the electrode portions E of the electronic devices D of the substrate W. The probe card 12 is connected to the tester 4 via an interface 13. During the electrical characteristic inspection, the probes 12a are brought into contact with the electrode portions E of the electronic devices D of the substrate W, supply a power from the tester 4 to the electronic devices D via the interface 13, and transmit signals from the electronic devices D to the tester 4 via the interface 13.

[0015]

A front opening unified pod (FOUP), which is a transfer container accommodating substrates W, is provided in the loader 3. The loader 3 has a transfer mechanism (not shown) for transferring the substrate W. The transfer mechanism takes out the substrate W accommodated in the FOUP and transfers it to the stage 10 of the accommodating chamber 2. Further, the transfer mechanism receives the substrate W for which the electrical characteristic inspection of the electronic devices D has been completed from the stage 10, and accommodates the substrate W in the FOUP.

[0016]

The tester 4 has a test board (not shown) for reproducing a part of the circuit configuration of the motherboard on which the electronic devices D are mounted. The test board of the tester 4 is connected to a tester computer 15 for determining whether the electronic devices D are defective or non-defective based on the signals from the electronic devices D. The tester 4 can reproduce the circuit configuration of multiple types of motherboards by replacing the test board. The probe card 12 has the plurality of probes 12a to be in contact with the plurality of electrode portions E of the electronic devices D. The tester 4 has a plurality of detection devices for detecting the electrical characteristics of the electronic devices D. As a result, the tester 4 detects the electrical characteristics of the electronic devices D.

[0017]

The inspection system 1 includes a user interface part 16 for displaying information to a user or for allowing a user to input instructions. The user interface part 16 includes an input part such as a touch panel or a keyboard, and a display part such as a liquid crystal display, for example.

[0018]

As described above, the inspection system 1 includes the stage 10 serving as a substrate holder for holding the substrate W. The inspection system 1 further includes the probe card 12 having the probes 12a, the interface 13, and the tester 4, as the detection part for detecting the electrical characteristics of the electronic devices D by supplying an inspection power to the electrode portions E of the electronic devices D on the substrate W.

[0019]

The loader 3 includes a temperature control unit 14. The temperature

control unit 14 has a power supply 25, a chiller 26, and a controller 90.

[0020]

The stage 10 is provided with a heater 20 for heating the stage 10. The power supply 25 supplies a power to the heater 20 in the stage 10. A coolant
5 channel 10a through which a heat transfer medium (antifreeze or the like) flows is formed in the stage 10. The chiller 26 circulates the heat transfer medium of which temperature has been adjusted through the coolant channel 10a. The inspection system 1 includes the heater 20, the power supply 25, the coolant channel 10a, and the chiller 26, as a temperature control mechanism for controlling
10 the temperature of the substrate holder. The configuration of the temperature control mechanism is not limited thereto.

[0021]

The temperature control mechanism includes a temperature detector 30 for detecting the temperature of the substrate holder. The temperature detector 30
15 is provided at the stage 10, and detects a temperature T_{stage} of the stage 10. The temperature T_{stage} of the stage 10 detected by the temperature detector 30 is inputted to the controller 90.

[0022]

The tester 4 includes a power detector 41 for detecting the inspection power
20 (current and voltage) supplied from the tester 4 to the electronic devices D via the interface 13 and the probe card 12. The inspection power detected by the power detector 41 is inputted to the controller 90.

[0023]

The tester 4 includes a temperature estimation part 42 for detecting a
25 junction temperature T_j that is the temperature of the junction portion of the electronic devices D from the correlation between the generated electromotive

force and the temperature by causing a current to flow through PN junction (junction portion, e.g., transistor) formed in the electronic devices D. The junction temperature T_j detected by the temperature estimation part 42 is inputted to the controller 90.

5 [0024]

The controller 90 has a holder temperature controller 91 and an offset temperature determining part 92. The controller 90 controls the temperature control mechanism such that the junction temperature T_j (temperature of the substrate W) of the electronic devices D becomes the inspection temperature.

10 [0025]

The holder temperature controller 91 controls the temperature control mechanism such that the temperature T_{stage} of the substrate holder detected by the temperature detector 30 becomes the control temperature or the offset control temperature. In other words, the holder temperature controller 91 controls the power supply 25 to control the heat generation amount of the heater 20, thereby controlling the temperature T_{stage} of the stage 10. The holder temperature controller 91 may control the chiller 26 to control the temperature of the heat transfer medium supplied by the chiller 26 to the coolant channel 10a, thereby controlling the temperature T_{stage} of the stage 10.

20 [0026]

The offset temperature determining part 92 determines the offset temperature of the control temperature according to the test pattern and/or the inspection power. As a result, during the inspection, the holder temperature controller 91 controls the temperature control mechanism such that the temperature T_{stage} of the substrate holder detected by the temperature detector 30 becomes the offset control temperature.

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[0027]

The offset temperature determining part 92 acquires the inspection power to be supplied to the electronic devices D. For example, the offset temperature determining part 92 acquires the inspection power to be supplied to the electronic devices D by inputting the inspection power detected by the power detector 41. The offset temperature determining part 92 may acquire the inspection power to be supplied to the electronic devices D by inputting the inspection power recorded in the test pattern of the electronic devices D from the tester computer 15.

[0028]

Next, the substrate W to be inspected in the above-described inspection system 1 will be described with reference to FIG. 3. FIG. 3 is a plan view schematically showing the configuration of the substrate W.

[0029]

By performing etching or wiring processing on a substantially circular silicon substrate, the plurality of electronic devices D are formed on the surface of the substrate W at predetermined intervals, as shown in FIG. 3. The electrode portions E are formed on the surfaces of the electronic devices D, i.e., the substrate W, and the electrode portions E are electrically connected to circuit elements in the electronic devices D. By applying a voltage to the electrode portions E, the current can flow through the circuit elements in the electronic devices D.

[0030]

Here, when the electronic devices D such as a logic IC and the like are inspected, the temperature estimation part 42 for detecting the junction temperature T_j may not be able to appropriately detect the junction temperature T_j due to the influence of noise or the like under the conditions where a clock is generated.

[0031]

Further, when the electronic devices D are inspected, the temperature difference occurs between the temperature T_{stage} of the stage 10 and the junction temperature T_j of the electronic devices D due to the thermal resistance between the stage 10 and the substrate W (electronic devices D). Therefore, when the electronic devices D are inspected by controlling the temperature such that the temperature T_{stage} of the stage 10 becomes the inspection temperature, the junction temperature T_j of the electronic devices D may be higher than the inspection temperature. In other words, the electronic devices D are inspected at a temperature higher than the inspection temperature, which may reduce the yield of the electronic devices D.

[0032]

Next, the temperature control in the inspection system 1 according to the present embodiment will be described with reference to Figs. 4 to 6. FIG. 4 is an example of a flowchart for explaining the temperature control in the inspection system 1.

[0033]

First, the offset temperature determining process will be described using steps S101 to S107. In the offset temperature determining process, the offset temperature of the control temperature of the substrate holder is determined.

[0034]

In step S101, the holder temperature controller 91 controls the temperature T_{stage} of the substrate holder to the initial control temperature. In other words, the holder temperature controller 91 controls the temperature control mechanism such that the temperature T_{stage} of the substrate holder detected by the temperature detector 30 reaches the control temperature. The initial control

temperature may be, for example, the inspection temperature.

[0035]

5 In step S102, the holder temperature controller 91 determines whether or not the temperature T_{stage} of the substrate holder detected by the temperature detector 30 is within a predetermined control temperature range including the initial control temperature. If the temperature T_{stage} is not within the control temperature range (NO in S102), the process of step S102 is repeated. If the temperature T_{stage} is within the control temperature range (YES in S102), the processing of the controller 90 proceeds to step S103. In the subsequent
10 processes (steps S103 to S104), the holder temperature controller 91 controls the temperature control mechanism such that the temperature T_{stage} is maintained within the predetermined control temperature range.

[0036]

15 In step S103, the tester 4 supplies an inspection power to the electrode portions E of the electronic devices D based on the test pattern, and performs the inspection of electrical characteristics of the electronic devices D.

[0037]

FIG. 5 is an example of a graph showing the temporal transition of the inspection power and the offset temperature $T_{joffset}$ of the electronic devices D. In FIG. 5, the upper graph shows an example of a test pattern of the inspection power supplied to the electronic devices D. The vertical axis represents the inspection power supplied to the electronic devices D. The horizontal axis represents time. The lower graph shows an example of the offset temperature $T_{joffset}$ of the electronic devices D. The vertical axis represents the offset
20 temperature $T_{joffset}$ of the electronic devices D. The horizontal axis represents time. Here, the offset temperature $T_{joffset}$ of the electronic devices D is the offset
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temperature of the junction temperature T_j of the electronic devices D with respect to the inspection temperature. In other words, the offset temperature $T_{j\text{offset}}$ of the electronic devices D is the temperature obtained by subtracting the inspection temperature from the junction temperature T_j of the electronic devices D.

5 [0038]

The test pattern includes multiple types of inspection with different inspection powers. In the example shown in FIG. 5, the test pattern includes first inspection performed with an inspection power P_1 , second inspection performed with an inspection power P_2 , third inspection performed with an inspection power P_3 , ..., i-th inspection (i being an arbitrary integer) performed with an inspection power P_i .

[0039]

By supplying the inspection power to the electronic devices D, the electronic devices D generates heat, and the temperature of the electronic devices D increases. In other words, the junction temperature T_j of the electronic devices D increases, and the offset temperature $T_{j\text{offset}}$ of the electronic devices D also increases. Further, by ending the inspection and stopping the supply of the inspection power, the temperature of the electronic devices D decreases. In other words, the junction temperature T_j of the electronic devices D decreases, and the offset temperature $T_{j\text{offset}}$ of the electronic devices D also decreases.

20 [0040]

Here, in the inspection of the electronic devices D, the temperature estimation part 42 cannot detect the junction temperature T_j of the electronic devices D. Therefore, in FIG. 5, the offset temperature $T_{j\text{offset}}$ of the electronic devices D in the section where the junction temperature T_j cannot be detected is indicated by a dashed line.

[0041]

In step S103, the tester 4 supplies the inspection power P1 to the electronic devices D based on the test pattern, and inspects the electrical characteristics of the electronic devices D. The offset temperature determining part 92 acquires the inspection power P1 supplied to the electronic devices D in the inspection of the electronic devices D shown in step S103. When the inspection of the electrical characteristics of the electronic devices D is completed, the tester 4 stops the supply of the inspection power P1.

[0042]

In step S104, the offset temperature determining part 92 acquires information on the junction temperature T_j after delay time t_{delay} . Specifically, the offset temperature determining part 92 detects (acquires) the transition of the junction temperature T_j from the temperature estimation part 42 after the delay time t_{delay} . As a result, the offset temperature determining part 92 detects (acquires) the transition of the offset temperature T_{joffset} of the electronic devices D after the delay time t_{delay} .

[0043]

FIG. 6 is an example of a graph showing the temporal transition of the inspection power and the offset temperature T_{joffset} of the electronic devices D before and after the inspection of the electronic devices D is completed. In FIG. 6, the vertical axis represents the offset temperature T_{joffset} of the electronic devices D and the inspection power supplied to the electronic devices D. The horizontal axis represents time. In FIG. 6, the offset temperature T_{joffset} of the electronic devices D in the detected range (after the delay time t_{delay}) is indicated by a solid line. In addition, the offset temperature T_{joffset} of the electronic devices D in the non-detected range (before the delay time t_{delay}) is indicated by a dashed

double-dotted line. The inspection power supplied to the electronic devices D is indicated by a dashed line.

[0044]

After the delay time t_{delay} has elapsed from the stop of the supply of the inspection power, the offset temperature determining part 92 detects the transition of the junction temperature T_j of the electronic devices D by the temperature estimation part 42. Then, the offset temperature determining part 92 detects the transition of the offset temperature T_{joffset} of the electronic devices D from the difference between the junction temperature T_j and the inspection temperature. As a result, as shown in FIG. 6, the transition in which the offset temperature T_{joffset} of the electronic devices D decreases is detected.

[0045]

In step S105, the offset temperature determining part 92 calculates a peak temperature $\text{TEMP}_{\text{peak}}$ during the inspection. Here, the peak temperature $\text{TEMP}_{\text{peak}}$ is the offset temperature T_{joffset} of the electronic devices D during the inspection. In other words, the peak temperature $\text{TEMP}_{\text{peak}}$ is the increase in the junction temperature T_j of the electronic devices D with respect to the inspection temperature during the inspection. In other words, the peak temperature $\text{TEMP}_{\text{peak}}$ is the temperature obtained by subtracting the inspection temperature from the junction temperature T_j of the electronic devices D during the inspection.

[0046]

Here, the offset temperature T_{joffset} at the time of stopping the supply of the inspection power is calculated as the peak temperature $\text{TEMP}_{\text{peak}}$. The system in which the offset temperature T_{joffset} of the electronic devices D decreases after the supply of the inspection power is stopped is represented as a

first-order lag system. The offset temperature determining part 92 calculates a time constant T by the least square method or the like from the transition of the offset temperature T_{offset} of the electronic devices D detected in step S104.

[0047]

5 Then, the offset temperature determining part 92 calculates the peak temperature $TEMP_{\text{peak}}$ by the following formula based on the delay time t_{delay} , the calculated time constant T , and the observed temperature $TEMP_{\text{ob}}$ at the delay time.

[0048]

10 $TEMP_{\text{peak}} = TEMP_{\text{ob}} \cdot \exp(t_{\text{delay}}/T)$

[0049]

In step S105, the peak temperature $TEMP_{\text{peak1}}$ (see FIG. 5) in the case of inspecting the electronic devices D with the inspection power $P1$ (see FIG. 5) is calculated.

15 [0050]

In step S106, the offset temperature determining part 92 stores the peak temperature $TEMP_{\text{peak}}$ in a memory part (not shown).

[0051]

20 In step S106, the offset temperature determining part 92 determines the peak temperature $TEMP_{\text{peak1}}$ as the offset temperature of the substrate holder in the case of inspecting the electronic devices D with the inspection power $P1$ (see FIG. 5), and stores the inspection power $P1$ and the peak temperature $TEMP_{\text{peak1}}$ (offset temperature of the substrate holder) in association with each other in the memory part.

25 [0052]

In step S107, the controller 90 determines whether or not all the test

patterns have been completed. If all the test patterns have not been completed (No in S107), the controller 90 returns to step S102 and repeats the processes from step S102 to step S106. As a result, in the second inspection and subsequent inspections performed with the inspection power P2, the inspection power and the peak temperature TEMP_{peak} (offset temperature of the substrate holder) are associated with each other and stored in the memory part.

[0053]

When all the test patterns have been completed (YES in S107), the controller 90 ends the offset temperature determining process (steps S101 to S107).

[0054]

The inspection power and the peak temperature TEMP_{peak} (offset temperature of the substrate holder) may be stored as a table in the memory part. The offset temperature determining part 92 may generate a function indicating the relationship between the inspection power and the peak temperature TEMP_{peak} (offset temperature of the substrate holder) from the information stored in the table, and the generated function may be stored in the memory part.

[0055]

Next, the inspection process will be described using steps S108 to S111. In the inspection process, the control temperature of the substrate holder is offset by the offset temperature determined in the offset temperature determining process to inspect the electronic devices D.

[0056]

In step S108, the holder temperature controller 91 controls the temperature T_{stage} of the substrate holder by the offset control temperature. In other words, the holder temperature controller 91 controls the temperature control mechanism

such that the temperature T_{stage} of the substrate holder detected by the temperature detection part 30 reaches the offset control temperature.

[0057]

For example, a configuration in which the tester sends an instruction to the controller 90 will be described. The tester 4 transmits, to the controller 90, the offset temperature of the substrate holder corresponding to the inspection power of the inspection to be performed next according to the test pattern (peak temperature $TEMP_{peak}$ stored in step S106). The controller 90 controls the temperature control mechanism to a temperature obtained by subtracting the offset temperature of the substrate holder from the initial control temperature.

[0058]

The tester 4 may be configured to transmit, to the controller 90, the inspection power of the inspection to be performed next according to the test pattern. In this case, the controller 90 determines the offset temperature of the substrate holder corresponding to the inspection power (peak temperature $TEMP_{peak}$ stored in step S106) and controls the temperature control mechanism to a temperature obtained by subtracting the offset temperature from the initial control temperature.

[0059]

Further, the inspection power detected by the power detector 41 may be transmitted to the controller 90. In this case, the controller 90 determines the offset temperature of the substrate holder corresponding to the inspection power (peak temperature $TEMP_{peak}$ stored in step S106) and controls the temperature control mechanism to a temperature obtained by subtracting the offset temperature from the initial control temperature.

[0060]

In step S109, the holder temperature controller 91 determines whether or not the temperature T_{stage} of the substrate holder detected by the temperature detector 30 is within a predetermined control temperature range including the offset control temperature. If the temperature T_{stage} is not within the control temperature range (NO in S109), the process of step S109 is repeated. If the temperature T_{stage} is within the control temperature range (YES in S109), the processing of the controller 90 proceeds to step S110. In the subsequent process (step S110), the holder temperature controller 91 controls the temperature control mechanism such that the temperature T_{stage} is maintained within the predetermined control temperature range. In the subsequent process (step S109), the holder temperature controller 91 controls the temperature control mechanism such that the temperature T_{stage} is maintained within the predetermined control temperature range.

[0061]

In step S110, the tester 4 supplies the inspection power to the electronic devices D based on the test pattern, and inspects the electrical characteristics of the electronic devices D.

[0062]

In the inspection shown in step S110, the temperature T_{stage} of the substrate holder is offset, so that the temperature of the electronic devices D during the inspection can become close to the inspection temperature.

[0063]

In step S111, the controller 90 determines whether or not all the test patterns have been completed. If all the test patterns have not been completed (NO in S111), the controller 90 returns to step S108 and repeats the processes from step S108 to step S110. If all the test patterns have been completed (S111,

YES), the controller 90 ends the inspection process (steps S108 to S111).

[0064]

As described above, the controller 90 can estimate the peak temperature TEMP_{peak} during the inspection based on the temperature change of the electronic devices D after the inspection. Accordingly, the junction temperature T_j during the inspection can be estimated.

[0065]

In addition, in the offset temperature determining process, the controller 90 estimates the peak temperature TEMP_{peak} during the inspection and stores it as the offset temperature of the substrate holder. Then, in the inspection process, the controller 90 controls the temperature of the substrate holder to the control temperature offset by the offset temperature. Accordingly, in the case of inspecting the electronic devices D, the electronic devices D can be set to the inspection temperature, and the inspection can be performed appropriately. In addition, a decrease in the yield of the electronic devices D can be prevented.

[0066]

In addition, the packaging cost of the electronic devices D can be reduced compared to the configuration in which the electrode portions E used only for detecting the junction temperature T_j are provided at the electronic devices. In addition, the number of probes 12a of the probe card 12 can be reduced.

[0067]

While the inspection apparatus 1 has been described, the present disclosure is not limited to the above-described embodiments, and various changes and modifications can be made without departing from the scope of the appended claims and the gist thereof.

[0068]

This application claims priority to Japanese Patent Application No. 2023-4559 filed on January 16, 2023, the entire contents of which are incorporated herein by reference.

5 **Description of Reference Numerals**

[0069]

W: substrate
D: electronic device
E: electrode portion
10 1: inspection system
 2: accommodating chamber
 3: loader
 4: tester
 10: stage
15 10a: coolant channel
 12: probe card
 12a: probe
 13: interface
 14: temperature control unit
20 20: heater
 25: power supply
 26: chiller
 30: temperature detector
 41: power detector
25 42: temperature estimation part
 50: temperature control mechanism

55: power supply

90: controller

91: holder temperature controller

92: offset temperature determining part

CLAIMS

[Claim 1]

5 An inspection system configured to inspect a substrate while performing temperature control using a temperature control mechanism, comprising:

- a substrate holder configured to hold the substrate;
- a detector configured to supply an inspection power to an electrode portion of the substrate; and
- a controller,

10 wherein the detector includes:

- a temperature estimation part configured to estimate a junction temperature of a junction portion provided at the substrate, and

the controller includes:

- supplying the inspection power to the substrate;
- 15 acquiring information on the junction temperature after the supply of the inspection power is stopped;
- determining an offset temperature of the substrate holder based on the information on the junction temperature;
- adjusting the temperature of the substrate holder based on a control
- 20 temperature offset by the offset temperature; and
- supplying the inspection power to the substrate to inspect the substrate after the temperature of the substrate holder is adjusted.

[Claim 2]

25 The inspection system of claim 1, wherein said acquiring information on the junction temperature includes:

acquiring transition of an offset temperature of the junction temperature, which is a difference between the junction temperature and the inspection temperature of the substrate.

5 [Claim 3]

The inspection system of claim 2, wherein said determining the offset temperature of the substrate holder includes:

estimating the offset temperature of the junction temperature at the time of stopping the supply of the inspection power based on the transition of the offset
10 temperature of the junction temperature; and

determining the offset temperature of the substrate holder based on the estimated offset temperature of the junction temperature at the time of stopping the supply of the inspection power.

15 [Claim 4]

The inspection system of claim 1, wherein the temperature control mechanism is configured to detect the temperature of the substrate holder and adjust the temperature of the substrate holder.

20 [Claim 5]

The inspection system of claim 1, wherein the detector has a detection device configured to detect a plurality of electrical characteristics.

[Claim 6]

25 The inspection system of claim 1, wherein the substrate includes:
the electrode portion; and

an electronic device connected to the electrode portion, and
wherein the detector is configured to detect electrical characteristics of the
electronic devices to which the inspection power is supplied.

5 [Claim 7]

A temperature control method for an inspection system for inspecting a
substrate while performing temperature control using a temperature control
mechanism,

wherein the inspection system includes:

10 a substrate holder configured to hold the substrate;

a detector that has a temperature estimation part configured to
estimate a junction temperature of a junction portion provided at the
substrate and is configured to supply an inspection power to an electrode
portion of the substrate,

15 the method comprising:

supplying the inspection power to the substrate;

acquiring information on the junction temperature after the supply
of the inspection power is stopped;

20 determining an offset temperature of the substrate holder based on
the information on the junction temperature;

adjusting the temperature of the substrate holder based on a control
temperature offset by the offset temperature; and

supplying the inspection power to the substrate and inspecting the
substrate after the temperature of the substrate holder is adjusted.

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[Claim 8]

The temperature control method of claim 7, wherein said acquiring information on the junction temperature includes:

acquiring transition of an offset temperature of the junction temperature, which is a difference between the junction temperature and the inspection
5 temperature of the substrate.

[Claim 9]

The temperature control method of claim 8, wherein said determining the offset temperature of the substrate holder includes:

10 estimating the offset temperature of the junction temperature at the time of stopping the supply of the inspection power based on transition of the offset temperature of the junction temperature; and

determining the offset temperature of the substrate holder based on the estimated offset temperature of the junction temperature at the time of stopping the
15 supply of the inspection power.