CLAIMS

Claim 1: A display apparatus, comprising:

a display module, comprising a plurality of pixels arranged in an array;

a plurality of light-emitting driving circuits, wherein each of the light-emitting driving circuits comprises:

a timing control circuit for receiving a plurality of clock signals and a previous light-emitting timing signal to provide a light-emitting timing signal and an internal voltage; and

a driving circuit for receiving a first phase signal among a plurality of phase signals and the internal voltage, and providing a light-emitting driving signal to the display module based on the first phase signal and the internal voltage to enable the plurality of pixels emitting light multiple times during one frame period,

wherein the phase signals all present a disabled level during a vertical blank period.

Claim 2: The display apparatus according to claim 1, wherein the timing control circuit comprises:

a first transistor having a first end for receiving the previous light-emitting timing signal, a control end for receiving a first direction scanning signal, and a second end;

a second transistor having a first end coupled to the second end of the first transistor, a control end for receiving a second direction scanning signal, and a second end for receiving a subsequent light-emitting timing signal;

a third transistor having a first end coupled to the second end of the first transistor, a control end for receiving a first clock signal of the clock signals, and a second end coupled

to the internal voltage;

a fourth transistor having a first end receiving a first gate voltage, a control end for receiving the internal voltage, and a second end for providing the light-emitting timing signal;

a first capacitor coupled between a second clock signal of the clock signals and the control end of the fourth transistor;

a fifth transistor having a first end, a control end coupled to the second end of the first transistor, and a second end for receiving a second gate voltage;

a second capacitor coupled between the first clock signal and the first end of the fifth transistor;

a sixth transistor having a first end for receiving the first gate voltage, a control end coupled to the first end of the fifth transistor, and a second end;

a seventh transistor having a first end coupled to the second end of the sixth transistor, a control end for receiving the internal voltage, and a second end for receiving the second gate voltage;

an eighth transistor having a first end for receiving the internal voltage, a control end coupled to the second end of the sixth transistor, and a second end for receiving the second gate voltage;

a ninth transistor having a first end coupled to the second end of the fourth transistor, a control end coupled to the second end of the sixth transistor, and a second end for receiving the second gate voltage; and

a tenth transistor having a first end for receiving the first gate voltage, a control end for receiving a reset signal, and a second end coupled to the second end of the sixth transistor.

Claim 3: The display apparatus according to claim 2, wherein the timing control circuit further comprises:

an eleventh transistor having a first end for receiving the second clock signal, a control end for receiving the internal voltage, and a second end, wherein the first capacitor is coupled between the second end of the eleventh transistor and the control end of the fourth transistor.

Claim 4: The display apparatus according to claim 3, wherein the timing control circuit further comprises:

a twelfth transistor having a first end for receiving the internal voltage, a control end for receiving the first gate voltage, and a second end coupled to the control end of the fourth transistor.

Claim 5: The display apparatus according to claim 4, wherein the timing control circuit further comprises:

a thirteenth transistor having a first end for receiving the internal voltage, a control end for receiving the first gate voltage, and a second end coupled to the control end of the eleventh transistor.

Claim 6: The display apparatus according to claim 2, wherein the timing control circuit further comprises:

a fourteenth transistor having a first end coupled to the control end of the eighth transistor, a control end coupled to the second end of the first transistor, and a second end coupled to the control end of the fourth transistor.

Claim 7: The display apparatus according to claim 2, wherein the driving circuit comprises:

a fifteenth transistor having a first end for receiving the first gate voltage, a control end for receiving the internal voltage, and a second end;

a sixteenth transistor having a first end coupled to the second end of the fifteenth transistor, a control end for receiving the first gate voltage, and a second end;

a seventeenth transistor having a first end for receiving the first phase signal, a control end coupled to the second end of the sixteenth transistor, and a second end for providing the light-emitting driving signal;

a third capacitor coupled between the control end of the seventeenth transistor and the second end of the seventeenth transistor;

an eighteenth transistor having a first end coupled to the second end of the fifteenth transistor, a control end coupled to the second end of the sixth transistor, and a second end receiving the second gate voltage;

a fourth capacitor coupled between the second end of the fifteenth transistor and the second gate voltage; and

a nineteenth transistor having a first end coupled to the second end of the seventeenth transistor, a control end coupled to the second end of the sixth transistor, and a second end for receiving the second gate voltage.

Claim 8: The display apparatus according to claim 1, wherein the display module comprises a plurality of display panels arranged in an array, and scanning directions of the display panels in odd-numbered rows are different from scanning directions of the display

panels in even-numbered rows.

Claim 9: The display apparatus according to claim 1, wherein each of the pixels comprises:

a light-emitting diode having an anode and a cathode for receiving a system low voltage;

a pixel driving circuit coupled between a system high voltage and the anode;

a first test transistor having a first end coupled to the anode, a control end for receiving a global test signal, and a second end for receiving a data voltage.

Claim 10: The display apparatus according to claim 9, wherein each of the pixels further comprises:

a second test transistor having a first end coupled to the second end of the first test transistor, a control end for receiving a corresponding light-emitting driving signal, and a second end for receiving the data voltage.

Claim 11: The display apparatus according to claim 10, wherein each of the pixels further comprises:

a third test transistor having a first end coupled to the anode, a control end for receiving a reset signal, and a second end for receiving a reference voltage.

Claim 12: The display apparatus according to claim 1, wherein each of the pixels comprises:

a light-emitting diode having an anode and a cathode for receiving a system low

voltage;

a pixel driving circuit coupled between a system high voltage and the anode; and

a fourth test transistor having a first end coupled to the anode, a control end for receiving a corresponding light-emitting driving signal, and a second end for receiving a data voltage.

Claim 13: A display apparatus, comprising:

a display module, comprising a plurality of pixels arranged in an array;

a plurality of light-emitting driving circuits coupled to the display module, wherein each of the light-emitting driving circuits comprises:

a first transistor having a first end for receiving a previous light-emitting timing signal, a control end for receiving a first direction scanning signal, and a second end;

a second transistor having a first end coupled to the second end of the first transistor, a control end for receiving a second direction scanning signal, and a second end for receiving a subsequent light-emitting timing signal;

a third transistor having a first end coupled to the second end of the first transistor, a control end for receiving a first clock signal, and a second end coupled to an internal voltage;

a fourth transistor having a first end for receiving a first gate voltage, a control end for receiving the internal voltage, and a second end for providing a light-emitting timing signal;

a first capacitor coupled between a second clock signal and the control end of the fourth transistor;

a fifth transistor having a first end, a control end coupled to the second end of

the first transistor, and a second end for receiving a second gate voltage;

a second capacitor coupled between the first clock signal and the first end of the fifth transistor;

a sixth transistor having a first end for receiving the first gate voltage, a control end coupled to the first end of the fifth transistor, and a second end;

a seventh transistor having a first end coupled to the second end of the sixth transistor, a control end for receiving the internal voltage, and a second end for receiving the second gate voltage;

an eighth transistor having a first end for receiving the internal voltage, a control end coupled to the second end of the sixth transistor, and a second end for receiving the second gate voltage;

a ninth transistor having a first end coupled to the second end of the fourth transistor, a control end coupled to the second end of the sixth transistor, and a second end for receiving the second gate voltage; and

a driving circuit for providing a light-emitting driving signal to the display module based on a first phase signal and the internal voltage to enable the plurality of pixels emitting light multiple times during one frame period,

wherein the first phase signal presents a disabled level during a vertical blank period.

Claim 14: The display apparatus according to claim 13, wherein each of the light-emitting driving circuits further comprises:

a tenth transistor having a first end for receiving the first gate voltage, a control end for receiving a reset signal, and a second end coupled to the second end of the sixth transistor.

Claim 15: The display apparatus according to claim 13, wherein each of the light-emitting driving circuits further comprises:

an eleventh transistor having a first end for receiving the second clock signal, a control end for receiving the internal voltage, and a second end, wherein the first capacitor is coupled between the second end of the eleventh transistor and the control end of the fourth transistor.

Claim 16: The display apparatus according to claim 15, wherein each of the light-emitting driving circuits further comprises:

a twelfth transistor having a first end for receiving the internal voltage, a control end for receiving the first gate voltage, and a second end coupled to the control end of the fourth transistor.

Claim 17: The display apparatus according to claim 16, wherein each of the light-emitting driving circuits further comprises:

a thirteenth transistor having a first end for receiving the internal voltage, a control end for receiving the first gate voltage, and a second end coupled to the control end of the eleventh transistor.

Claim 18: The display apparatus according to claim 13, wherein each of the light-emitting driving circuits further comprises:

a fourteenth transistor having a first end coupled to the control end of the eighth transistor, a control end coupled to the second end of the first transistor, and a second end coupled to the control end of the fourth transistor.