

PATENT SPECIFICATION

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DRAWINGS ATTACHED



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(54) IMPROVEMENTS IN OR RELATING TO MULTIPLE LAYER METAL STRUCTURE AND PROCESSING

(71) We, FAIRCHILD CAMERA & INSTRUMENT CORPORATION, of P.O. Box 880, Mountain View, California, United States of America, a Corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to multiple layer metallization of semiconductor substrates and also to a method of producing the individual layers of the multiple layer.

Multiple layers of conductive patterns, each layer being insulated from adjacent layers by an intervening dielectric, are commonly used to interconnect the active and/or passive regions of a semiconductor substrate, and to connect the electrical circuit or circuits in or on the substrate to external circuits. Such multiple layer structures have always been troublesome. Yields have been low due to breaking of the conductors or due to inadvertent shorting of one conductive layer to another conductive layer due to pinholes or cracks in the intermediate dielectric. Cracks in the conductors have occurred at the holes through the dielectric used for contacting adjacent metal layers, or at the transitions over underlying metal layers. Furthermore, intermetallic contacts between adjacent conductive layers have often been of poor quality. Consequently the yields of multiple layer semiconductor devices, that is the percentages of useful devices obtained from production runs have been notoriously low.

This invention substantially overcomes the short and open circuit problems of the prior art multiple layer metallization structures thereby to increase the yield associated with these structures.

According to one aspect of the invention, a semiconductor device comprising a semiconductor substrate containing a plurality of

layers of conductive leads, each layer of conductive leads being separated from adjacent layers of leads by intervening dielectric layers, and the bottom layer of conductive leads being separated from the underlying substrate by a first dielectric layer, said conductive layers selectively contacting adjacent conductive layers through holes in the intervening dielectric layers, and said bottom layer of conductive leads selectively contacting regions of active or passive circuit elements in the underlying substrate through windows in said intervening dielectric layer, said device being characterized in that each lead in each conductive layer possesses sloped sides and rounded edges thereby to ensure that leads which pass over underlying leads make gradual transitions over said lower leads. The term "edge" is used to mean the intersection of a side of a conductor with the top of the conductor. Consequently, overlying layers of dielectric and metal no longer change elevation abruptly when passing over underlying conductors but rather change elevation gradually and gently to pass over underlying conductors. The result is the almost complete elimination of breaks in the conductors at the cross-over points. Consequently, multiple layer interconnective patterns overlying semiconductor substrates are now possible with the result that a wide variety of design alternatives are available to the circuit designer. One immediate result of this invention is that the use of a plurality of overlying metal layers on a semiconductor die is now economically feasible because of the high yields associated with the invented process for producing the disclosed structure. Structures with as many as three layers of metal have been produced using the techniques of this invention with yields significantly improved over those of prior art processes.

According to another aspect of the invention, a method of producing a layer of conductor leads adherent to and overlying

an underlying dielectric layer in a wafer which includes a semiconductor substrate comprises depositing a layer of metal over said underlying dielectric layer, said layer of metal adhering to said dielectric layer, masking said layer of metal to define the conductive pattern to be formed from said layer of metal, leaving unmasked those portions of said layer of metal which are to be removed, submerging said wafer in a selected etch which not only removes the unmasked portions of said layer of metal but also removes the mask defining the conductive pattern to be produced from said metal layer, so as not only to etch away the unmasked regions of said metal layer but also to etch the metal exposed by lifting said conductive-pattern-defining mask from said metal layer to provide each lead in said layer of conductive leads with sloping sides and rounded edges and removing said wafer containing said etched metal layer from said etch after the unmasked metal has been completely removed.

In the prior art, the etching is carried out so as to avoid the lifting of the photoresist material defining the conductive pattern. As a result, the metal conductors underlying the photoresist material had steep sides and sharply defined edges. Upon completion of the etching, the photoresist material was removed from the remaining metal conductors. Then a dielectric layer was deposited over the metal conductors and a second metal layer was evaporated over this intervening dielectric. Usually contact holes were provided in this intervening dielectric to provide electrical contact between the first and second metal layers. The dielectric, however, possessed sharp edges overlying the edges of the underlying metal conductors. These sharp edges introduced discontinuities in the newly evaporated second metal layer. Upon etching away of the undesired portions of the second metal layer, the remaining metal conductors often cracked and broke at the sharp discontinuities in the underlying dielectric.

Thus, the etchant used to etch away the undesired portions of each metal layer is an etchant which lifts the masking material while it etches. Consequently, the etchant, a mixture of concentrated nitric, phosphoric and acetic acids when the conductors are of aluminum or an aluminum-silicon alloy, not only etches away the exposed metal, but also etches away substantial amounts of the metal on the tops and edges of the conductors exposed by the lifting of the masking material. This substantially slopes the sides and rounds the edges of the conductors remaining upon the completion of the etching. Consequently, the overlying dielectric layer deposited after the etching has been completed and the wafer cleaned, rides over

each underlying conductor by gently rising and climbing over this conductor rather than by abruptly changing its elevation. The second metal layer deposited over this dielectric consequently sees only gradual changes in elevation as it crosses over underlying conductors, rather than abrupt changes. Consequently the structural integrity of this second layer is maintained over these transition areas thereby eliminating the open-circuits and micro-cracks commonly prevalent in the prior art multiple layer structures.

Description of the Drawings

Figs. 1a and 1b illustrate in cross-section a typical prior art structure together with a typical open-circuit in a conductor due to an abrupt transition in an underlying conductive pattern.

Figs. 2a through 2e illustrate the etching process of the prior art for producing the metal conductors in one conductive layer.

Figs. 3a through 3e illustrate the etching process for producing the sloped and rounded conductors.

Figs. 4a and 4b illustrate the rounded transitions over underlying conductors.

Detailed Description

Figs. 1a and 1b illustrate a typical multi-layer structure of the prior art. A semiconductor substrate 11, of one type conductivity, has diffused into it a region 6 of opposite type conductivity. Substrate 11 is typically silicon, although any other semiconductor material such as germanium or gallium arsenide can be used if desired. Overlying and adherent to the top surface of substrate 11 is dielectric layer 12. Typically, if substrate 11 is silicon, dielectric 12 is silicon dioxide. A window 25 is cut in silicon dioxide layer 12 to define the region of substrate 11 into which region 6 is diffused. The use of oxide layer 12 as a mask for the diffusion of region 6 is well known in the arts and is described in U.S. Patent No. 3,025,589, issued March 20, 1962 and assigned to Fairchild Camera and Instrument Corporation, the assignee of this invention.

A second layer 12a of oxide is next reformed over that portion of substrate 11 exposed by window 25. A new window 25a is cut in this oxide. Electrical contact to the underlying diffused region 6 will be made through this window.

Conductive layer 13, which typically is aluminum but which can also be any other conductive metal such as a molybdenum-manganese-gold combination, is next deposited over dielectric layers 12 and 12a and window 25a through layer 12a. Metal 13 makes ohmic contact with a portion of the top surface of region 6 diffused in substrate 11. It should be noted that hereafter sub-

strate 11 together with any overlying layers of dielectric materials or conductors, will be referred to as wafer 10.

As shown in Fig. 1a, conductor 13 terminates just to the right of window 25a in dielectric layer 12a. The end of conductor 13, denoted by number 24a, has a sharp edge. Consequently, overlying dielectric layer 14 likewise has a sharp edge 24b adjacent edge 24a. Next, a second layer of metallization, layer 15, is evaporated over the top surface of dielectric layer 14. Metal 15 likewise has a sharp edge 24c caused by the sharp edge 24a of metal conductor 13. As shown by Fig. 1b, edge 24c of metal layer 15 often crazes or cracks with the result that conductor 15 open circuits. This often destroys a device.

Fig. 1a illustrates a third dielectric layer, layer 16, overlying metal layer 15. Placed on top of layer 16 is a third layer metal conductor, conductor 17. As shown in Fig. 1a, conductor 17 is intended to be perpendicular to conductor 15 but in a plane parallel to the plane occupied by conductor 15. Conductor 17 likewise has sharp edges, which cause corresponding sharp edges in overlying insulation layer 18. These edges, labeled 22a and 22b in Fig. 1, will cause cracks in any fourth layer conductor which must pass over conductor 17.

Figs. 2a through 2e illustrate the prior art process by which not only conductor 17, but also conductors 13 and 15, are produced from an evaporated layer of metal. Figs. 2a through 2e show just a small section of the wafer 10 shown in Fig. 1a and 1b. This section includes a portion of dielectric layer 16, and metal layer 17. Shown in Figs. 2a through 2e on top of metal layer 17 is a layer 23 of masking material, typically KMER (Registered Trade Mark) photoresist. Those portions of photoresist layer 23 overlying portions of evaporated metal layer 17 to be etched away are removed using well-known photolithographic techniques. Consequently, photoresist 23 remains only over those portions of metal 17 which are to form the third layer conductors on the wafer 10 shown in Figs. 1a and 1b.

Next, an etchant is brought into contact with the exposed surface of metal layer 17. The etchant is carefully selected not to undercut and lift masking material 23. Consequently, the etchant eats away exposed portions of metal layer 17 but leaves substantially untouched those portions of metal layer 17 lying under masking material 23. Of course, there is some lateral etching by the etchant of those portions of metal layer 17 underlying masking material 23. But because the width of the conductor is an order of magnitude or so greater than the thickness of the conductor, this lateral etching has sub-

stantially no effect on the ultimate size of the conductor. More importantly, etchant is unable to penetrate the interface between masking material 23 and the underlying metal 17. Consequently, the sides of conductor 17 remain substantially vertical and edges 17a and 17b of conductor 17 shown, for example, in Fig. 2e, remain sharp and in contact with overlying layer of masking material 23. The result is that when dielectric layer 18 Fig. 1a is deposited over conductor 17, edges 22a and 22b of dielectric layer 18 are likewise sharp. Any metal layer deposited over these edges will most likely exhibit cracks and breaks at these edges.

The process of this invention in the formation of a single layer is illustrated by Figs. 3a through 3e. Fig. 3a illustrates the identical structure shown in Fig. 2b with mask 23 again defining the conductive pattern to be formed from metal layer 17. The structure shown in Fig. 3a is brought into contact with an etchant. The etchant is carefully selected not only to remove the exposed portions of metal layer 17, but also to undercut and penetrate the interface between overlying layer of masking material 23 and the underlying metal conductor 17. Consequently, as shown in Fig. 3b, masking material 23 lifts at edges 23a and 23b. The etchant thus attacks the underlying metal 17 not only in a direction perpendicular to the plane of metal layer 17, but also in a direction parallel to this plane. The exposing of the top surface of metal layer 17 underlying masking material 23 results in the sides, the top surface, and in particular, the edges 17a and 17b (Fig. 2e) of metal 17 being etched away. As the process continues, etchant continues to destroy the bond between masking material 23 and underlying metal layer 17 until finally, at the completion of the etching, the sharp edges normally present in the remaining portions of conductive metal 17 have been completely removed. This process is illustrated in Figs. 3b through 3d. The resulting conductor has a cross-section substantially rounded as represented by conductor 17 in Fig. 3e.

When the metal conductors are aluminum, or an aluminum-silicon alloy containing no more than two (2) per cent silicon, the etchant used to produce the structure shown in Fig. 3e comprises, in one embodiment, 20% concentrated acetic acid, 20% concentrated nitric acid, and 60% concentrated phosphoric acid, all acid percentages being by volume. The etchant is heated to a given temperature, typically around 85°C plus or minus 15°C. The etching process continues for a selected time period, typically around one (1) to two (2) minutes until the exposed portions of metal layer 17 (Fig. 3a) have been completely removed.

Completion of etching is determined by

visual observation. The wafer is taken out of the etching solution, and observed. A darkening of the surface means that the unmasked metal has been removed and that the oxide underlying this metal is visible. Upon complete removal of the unmasked metal, the exposed surface appears dark. No perceptible etching of the oxide occurs.

A typical process for depositing two layers of metallization is as follows. The numbers in this description refer to Fig. 4b. The first layer 13 of aluminum is evaporated over oxide layer 12 on substrate 11. This aluminum, being in contact with silicon from oxide layer 12 and substrate 11, will contain a small percentage of silicon. The substrate may or may not be heated although heating generally insures a more uniform, better quality aluminum layer. Aluminum layer 13 is masked with KMER. The unmasked portions of aluminum 13 are removed by the special etch solution which also lifts the conductive-pattern-defining masking material thereby rounding all edges and sloping all sides of the remaining conductors. This etch is at 85°C and consists of 20% by volume concentrated acetic acid, 20% by volume concentrated nitric acid, and 60% by volume concentrated phosphoric acid. Upon completion of the etching, any remaining mask is removed. Then an oxide layer 14, containing a selected amount of phosphorus, is grown over the first layer aluminum 13 and the exposed oxide layer 12. Typically, this second dielectric layer 14 is about 0.5 microns thick. Next, dielectric layer 14 is masked and contact holes are etched through this dielectric to selected ones of underlying aluminum conductors 13. Then a selected thickness of a second aluminum layer, such as layer 15 (Fig. 4b) is deposited onto dielectric layer 14. For this deposition, the substrate is heated to about 350°C. Layer 15 is about 1 micron thick. Masking of this second aluminum layer to define the conductive pattern to be formed by this layer is followed by an etch using either the same solution as was used to etch the first aluminum layer if further layers are to be applied or a standard etch solution if no further layers are to be applied when there is no

need to slope the sides and round the edges of these conductors. Upon completion of the etching, the wafer 10 is rinsed in deionized water and sintered at 420°C for 10 minutes. Sintering ensures good electrical contact between the two aluminum layers and is also used to place a thin gold layer on the backside of the wafer for use in attaching each die to a support.

No satisfactory theory explaining the operation of the special etch used has as yet been developed. It is believed, however, that a competing reaction exists between nitric and phosphoric acid in the etch solution. Nitric acid is an oxidizing agent. It is believed that the nitric acid actually travels by capillary action along the interface between the aluminum layer and the overlying conductive-pattern-defining resist. The nitric acid breaks whatever bond exists between the overlying resist and the underlying aluminum. The acetic acid inhibits the nitric acid reaction but does not inhibit the phosphoric acid reaction. Consequently, the nitric acid lifts the resist, and then the phosphoric acid etches the exposed aluminum thereby sloping the sides and rounding off the edges of the conductor being etched. The acetic acid slows the rate of lifting of the photoresist.

Tables I, II, III, and IV give the effects of various mixtures of phosphoric, nitric and acetic acid, all concentrated, as a function of temperature, on the angles of the sides of an aluminum conductor with the horizontal plane as well as describe the appearance of the edges of the intersections of these sides with the top of the aluminum conductor. The sides of the conductors are essentially those sides of conductor 17 shown in Fig. 2e which rise from insulating layer 16 to contact photoresist layer 23 in this figure. Analysis of the tables shows that, in general, as the percentage of nitric acid in the etch solution goes down, the temperature at which sloping of the sides and rounding of the edges occurs, goes up. But as the temperature goes up, the speed of the etching reaction goes up. Consequently, experience has shown that an operator usually cannot accurately time the process when the temperature of the etchant is above 100°C.

TABLE I

	Temperature	Concentration (Percent Volume)	Remarks	
			Angle of sides with horizontal	Edge at intersection of side and top
5	60°C	60% Phosphoric 20% Nitric 20% Acetic	About 45°	Sharp
10	65°C	Same	About 30°	Sharp
	70°C	Same	About 30°	Rounding begins
	80°C	Same	About 30° or less	Well-rounded
	90°C	Same	Less than 30°	Completely rounded
15	100°C	Same	Increases toward 30°	Discernable but still rounded
	105°C	Same	Increases toward 30°	Discernable but still rounded
	110°C	Same	About 30°	Sharp

TABLE II

	Temperature	Concentration	Remarks	
			Angle of sides with horizontal	Edge at intersection of side and top
25	50°C	70% Phosphoric 15% Nitric 15% Acetic	About 70°	Sharp
30	60°C	Same	About 70°	Sharp
	70°C	Same	About 30°	Begins to round
	80°C	Same	About 30°	Rounding increases
	90°C	Same	Slightly steeper than 30°	Very well rounded
35	100°C	Same	Slightly steeper than 30°	Top of edge still rounded but sharpness appears near bottom of edge
	110°C	Same	Between 30° and 45°	Sharp

TABLE III

	Temperature	Concentration	Remarks
5	70°C, 80°C and 90°C	80% Phosphoric 10% Nitric 10% Acetic	At 70°C and 80°C sides made an angle of about 60° with horizontal. At 90°C side angle was lower than at lower temperatures. At all three temperatures, edges at intersections of sides with top were sharp.
10	70°C, 80°C and 90°C	90% Phosphoric 5% Nitric 5% Acetic	At these three temperatures sides were all almost vertical (making angle of about 85° with horizontal) and edges at intersections of sides with tops were sharp.

TABLE IV

	Temperature	Concentration	Remarks
15	All temperatures	60% Phosphoric 30% Nitric 10% Acetic	Get sloped sides with well rounded edges.
20	All temperatures	60% Phosphoric 10% Nitric 30% Acetic	Get severe and non uniform lifting of masking material at all temperatures.
	All temperatures	40% Phosphoric 40% Nitric 20% Acetic	Results unusable.

- 25 Figs. 4a and 4b show structure substantially similar to that of Fig. 1a, with the exception that the metal conductors 13, 15, 17 and the additional conductor 19, shown in both Figs. 4a and 4b, have all been etched, the edges of insulating layers 16 and 18 and metal conductor 19 showing a break line indicating that only a section of the structure is shown. The edge 24a of conductor 13 is rounded by the process of this invention with the result that the edge 24c of conductor 15 overlying the terminal portion of conductor 13 is also rounded. As a result, this edge does not exhibit the cracks commonly observed at this point in a multiple layer metal pattern. Likewise, the cross-section of conductive layer 17 is rounded with the result that overlying metal layer 19 rises gradually over and across layer 17.
- 30 While this invention has been described in connection with a semiconductor device containing two, three or four metal layers, this invention can, of course, be used to produce semiconductor devices containing any desired number of metal layers.
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- WHAT WE CLAIM IS:—
1. A semiconductor device comprising a semiconductor substrate carrying a plurality of layers of conductive leads, each layer of conductive leads being separated from adjacent layers of leads by intervening dielectric layers, and the bottom layer of conductive leads being separated from the underlying substrate by a first dielectric layer, said conductive layers selectively contacting adjacent conductive layers through holes in the intervening dielectric layers, and said bottom layer of conductive leads selectively contacting regions of active or passive circuit elements in the underlying substrate through windows in said intervening dielectric layer, said device characterized in that: each lead in each conductive layer possesses sloped sides and rounded edges thereby to ensure that leads which pass over underlying leads make gradual transitions over said lower leads.
 2. A device as claimed in claim 1 in which said semiconductor device includes two layers of conductive leads.
 3. A device as claimed in claim 1 in which said semiconductor device includes three layers of conductive leads.
 4. A device as claimed in claim 1 in which said semiconductor is silicon and said first dielectric layer is a compound of silicon.
 5. A device as claimed in claim 4 in

TABLE III

	Temperature	Concentration	Remarks
5	70°C, 80°C and 90°C	80% Phosphoric 10% Nitric 10% Acetic	At 70°C and 80°C sides made an angle of about 60° with horizontal. At 90°C side angle was lower than at lower temperatures. At all three temperatures, edges at intersections of sides with top were sharp.
10	70°C, 80°C and 90°C	90% Phosphoric 5% Nitric 5% Acetic	At these three temperatures sides were all almost vertical (making angle of about 85° with horizontal) and edges at intersections of sides with tops were sharp.

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	All temperatures	40% Phosphoric 40% Nitric 20% Acetic	Results unusable.

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- 30 While this invention has been described in connection with a semiconductor device containing two, three or four metal layers, this invention can, of course, be used to produce semiconductor devices containing any desired number of metal layers.
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- WHAT WE CLAIM IS:—
1. A semiconductor device comprising a semiconductor substrate carrying a plurality of layers of conductive leads, each layer of conductive leads being separated from adjacent layers of leads by intervening dielectric layers, and the bottom layer of conductive leads being separated from the underlying substrate by a first dielectric layer, said conductive layers selectively contacting adjacent conductive layers through holes in the intervening dielectric layers, and said bottom layer of conductive leads selectively contacting regions of active or passive circuit elements in the underlying substrate through windows in said intervening dielectric layer, said device characterized in that: each lead in each conductive layer possesses sloped sides and rounded edges thereby to ensure that leads which pass over underlying leads make gradual transitions over said lower leads.
 2. A device as claimed in claim 1 in which said semiconductor device includes two layers of conductive leads.
 3. A device as claimed in claim 1 in which said semiconductor device includes three layers of conductive leads.
 4. A device as claimed in claim 1 in which said semiconductor is silicon and said first dielectric layer is a compound of silicon.
 5. A device as claimed in claim 4 in



which said plurality of layers of conductive leads comprise a plurality of layers of aluminium leads, and one intervening dielectric layer comprises a layer of a compound of silicon containing an amount of phosphorus.

6. A method of producing a layer of conductor leads adherent to and overlying an underlying dielectric layer in a wafer which includes a semiconductor substrate comprising depositing a layer of metal over said underlying dielectric layer, said layer of metal adhering to said dielectric layer, masking said layer of metal to define the conductive pattern to be formed from said layer of metal, leaving unmasked those portions of said layer of metal which are to be removed, submerging said wafer in a selected etch which not only removes the unmasked portions of said layer of metal but also removes the mask defining the conductive pattern to be produced from said metal layer, so as not only to etch away the unmasked regions of said metal layer but also to etch the metal exposed by lifting said conductive-pattern-defining mask from said metal layer to provide each lead in said layer of conductive leads with sloping sides and rounded edges and removing said wafer containing said etched metal layer from said etch after the unmasked metal has been completely removed.

7. The method as claimed in claim 6 wherein said metal layer is aluminum.

8. The method as claimed in claim 7 wherein said etchant is a heated mixture of phosphoric, nitric and acetic acids.

9. The method as claimed in claim 8 wherein said mixture of acids is heated to between 60 and 110 degrees C.

10. The method as claimed in claim 8 wherein said mixture of acids is heated to a temperature between 70 and 100 degrees C.

11. The method as claimed in claim 10 wherein said mixture of acids comprises between 60 and 80 percent by volume concentrated phosphoric acid, with the remaining percentage by volume being approximately equally divided between nitric and acetic acid, both concentrated.

12. The method of claim 10 wherein,

said phosphoric acid comprises between 60 and 80 percent by volume of said etchant, said nitric acid comprises between 10 and 30 percent by volume of said etchant, and said acetic acid comprises the remainder of said etchant, all said acids being concentrated.

13. The method as in claim 10 wherein said phosphoric acid comprises about 60 percent by volume of said etchant, said nitric acid comprises between 10 and 30 percent by volume of said etchant, and said acetic acid comprises the remainder of said etchant.

14. A semiconductor device comprising a semiconductor substrate carrying a plurality of layers of conductive leads, each layer of conductive leads being separated from adjacent layers of leads by intervening dielectric layers, and the bottom layer of conductive leads being separated from the underlying substrate by a first dielectric layer, said conductive layers selectively contacting adjacent conductive layers through holes in the intervening dielectric layers, and said bottom layer of conductive leads selectively contacting regions of active or passive circuit elements in the underlying substrate through windows in said intervening dielectric layer, said device characterized in that: each lead in each conductive layer, except for the top conductive layer, possesses sloped sides and rounded edges thereby to ensure that leads which pass over underlying leads make gradual transitions over said lower leads.

15. The method of producing a layer of conductive leads adherent to and overlying an underlying dielectric layer substantially as described with reference to Figs. 3a to 3e of the accompanying drawings.

16. A semiconductor device substantially as described with reference to Fig. 4b of the accompanying drawings.

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