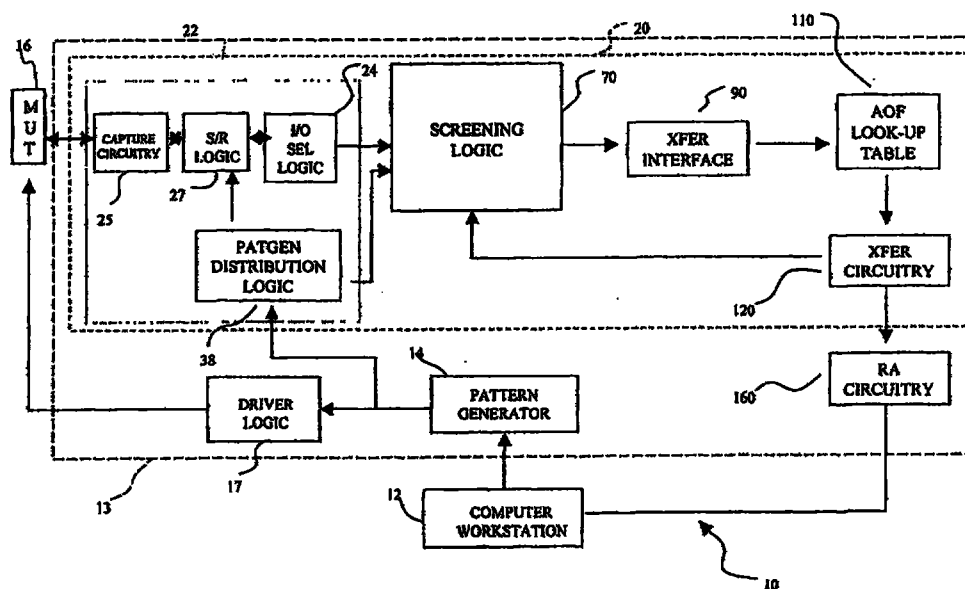




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(54) Title: FAILURE CAPTURE APPARATUS AND METHOD FOR AUTOMATIC TEST EQUIPMENT



(57) Abstract

A failure capture circuit for identifying failure location information from a memory-under-test (MUT) having a predetermined storage capacity is disclosed. The failure capture circuit includes failure detection circuitry adapted for coupling to the MUT and operative to apply test signals to the MUT and process output signals therefrom into failure information. The failure information is indicative of failed memory cell locations. A look-up table couples to the failure detection circuitry for storing the location information, thereby minimizing the size of the look-up table and the time to transfer failure data to a redundancy analyzer.