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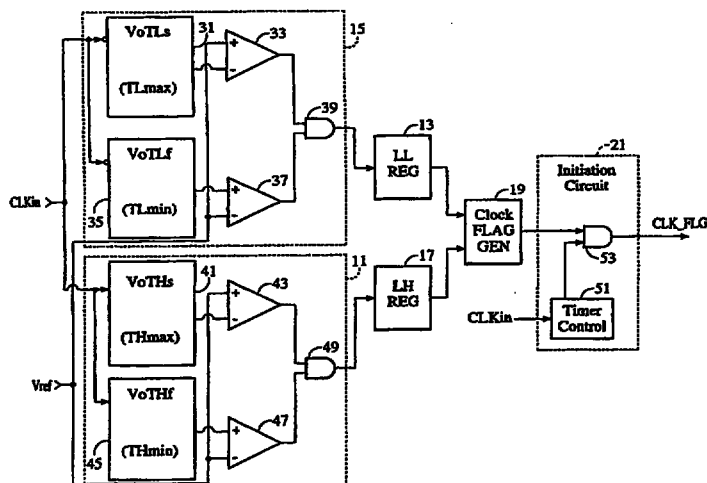
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(54) Title: DIGITAL FREQUENCY MONITORING



(57) Abstract: A pulse monitoring circuit monitors the pulse length of both the logic high pulse (11) and logic low pulse (15) of a received digital sequence. The pulse lengths are compared with a preferred transition window, and if the pulses transition are within the preferred transition window then they are categorized as good pulses. The pulse monitoring circuit issues an enable signal only when at least two consecutive good pulses are received. The pulse length is determined by means of a reference voltage (Vref), a first faster linear voltage ramp (35, 45), and a second slower linear voltage ramp (31, 41). The two linear voltage ramps are initiated in response to a logic change of the received digital sequence and continue to raise their outputs until the received digital sequence changes state once again. The values of the two linear voltage ramps at the time of the second state change are compared with the reference voltage. If the faster linear voltage ramp is above the reference voltage and the slower linear voltage ramp is below the reference voltage, then the observed pulse of the digital sequence is determined to have transitioned within its preferred transition window.