

ABSTRACT

The present disclosure provides an MBIST control circuit and method, a memory, and a device. The circuit includes: a memory control circuit, configured to receive an external precharge command of a target word line, generate a counter update command in response to the external precharge command, and output the counter update command; and a per row hammer tracking (PRHT) control circuit, configured to receive the counter update command, receive a PRHT control command, and stop providing the counter update command to a second output terminal of the PRHT control circuit when the PRHT control command is in a first level state, so that a row counter unit of the target word line connected to the second output terminal stops updating when no counter update command is received. The first level state of the PRHT control command is used to indicate a state of being in the MBIST test mode.

[Fig. 6]