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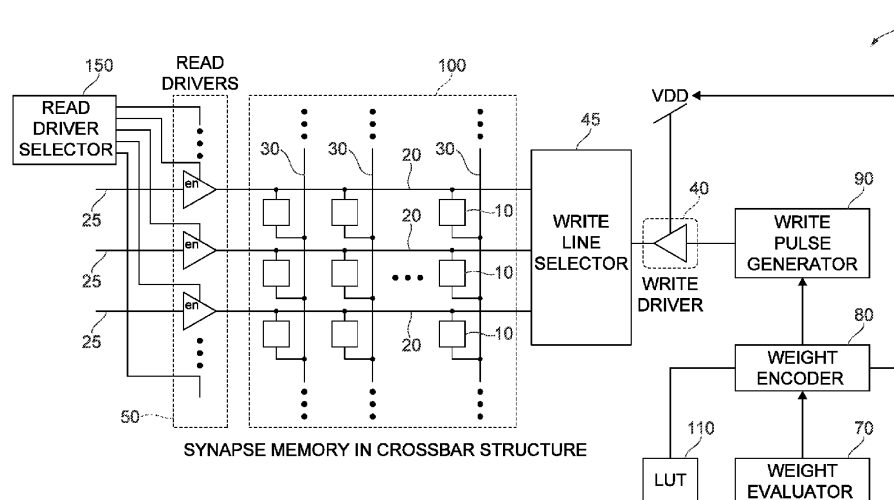
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**(54) Title:** PERFORMANCE AND AREA EFFICIENT SYNAPSE MEMORY CELL STRUCTURE

FIG.2



(57) **Abstract:** A synapse memory system includes: synapse memory cells provided at cross points of axon lines and dendrite lines, each synapse memory cell including plural analog memory devices, each synapse memory cell being configured to store a weight value according to an output level of a write signal, the plural analog memory devices being combined to constitute each synapse memory cell; a write portion configured to write the weight value to each synapse memory cell and including a write driver and an output controller, the write driver being configured to output the write signal to each synapse memory cell, the output controller being configured to control the output level of the write signal of the write driver; and read drivers configured to read the weight value stored in the synapse memory cells.

[Continued on next page]

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