CLAIMS

1. A semiconductor memory device comprising:

a first bit line;

a first capacitor; and

a first select transistor and a first memory cell transistor ~~and a second memory cell transistor~~ that are coupled in series between the first bit line and the first capacitor;

a second capacitor;

a second select transistor and a second memory cell transistor that are coupled in series between the first bit line and the second capacitor;

a first select gate line coupled to a gate of the first select transistor;

a second select gate line coupled to a gate of the second select transistor; and

a first word line coupled to a gate of the first memory transistor and a gate of the second memory transistor.

2. The semiconductor memory device according to claim 1, further comprising a ~~select~~ third memory transistor ~~electrically coupled to the first bit line~~, wherein

the first memory cell transistor and the ~~second~~ third

memory cell transistor being coupled in series between the first select transistor and the first capacitor.

3. The semiconductor memory device according to claim 1, wherein the first capacitor includes a first end configured to be electrically coupled to the first bit line, and a second end in a floating state.

4. The semiconductor memory device according to claim 1, wherein the first capacitor includes a first end configured to be electrically coupled to the first bit line, and a second end that is grounded.

5. The semiconductor memory device according to claim 1, comprising a first memory string and a second memory string, wherein~~each including the capacitor, the first memory cell transistor, and the second memory cell transistor,~~

the first memory string includes the first capacitor, the first select transistor, and the first memory transistor,

the second memory string includes the second capacitor, the second select transistor, and the second memory transistor, and

the first memory string and the second memory string ~~being~~ are electrically coupled to the first bit line.

6. The semiconductor memory device according to claim 1, comprising:

a second bit line different from the first bit line;

a first memory string being electrically coupled to the first bit line; and

a second memory string being electrically coupled to the second bit line, wherein

the first memory string includes the first capacitor, the first select transistor, and the first memory transistor,

the second memory string includes a third capacitor, a third select transistor, and a fourth memory transistor,

the third select transistor and the fourth memory transistor are coupled in series between the second bit line and the third capacitor~~, each including the capacitor, the first memory cell transistor, and the second memory cell transistor,~~

~~the first memory string being electrically coupled to the first bit line, and~~

~~the second memory string being electrically coupled to a second bit line different from the first bit line~~.

~~7. A semiconductor memory device comprising:~~

~~a plurality of first conductive layers stacked in a~~

~~first direction above a semiconductor layer;~~

~~a semiconductor film extending in the first direction through the semiconductor layer and the first conductive layers; and~~

~~a charge storage film interposed between the semiconductor layer and the semiconductor film and between the semiconductor film and the first conductive layers.~~

~~8. The semiconductor memory device according to claim 7, wherein the semiconductor layer includes:~~

~~a first portion located below a bottom end of the charge storage film; and~~

~~a second portion and a third portion that are in contact with the first portion above the bottom end of the charge storage film, and that are separated from each other.~~

~~9. The semiconductor memory device according to claim 8, wherein the charge storage film includes:~~

~~a first portion located between the first portion of the semiconductor layer and the semiconductor film;~~

~~a second portion located between the second portion of the semiconductor layer and the semiconductor film; and~~

~~a third portion located between the third portion of the semiconductor layer and the semiconductor film.~~

~~10. The semiconductor memory device according to claim 7, wherein the semiconductor layer is a substrate.~~

~~11. The semiconductor memory device according to claim 7, wherein the charge storage film is a continuous film formed between the semiconductor layer and the semiconductor film, and between the semiconductor film and the first conductive layers.~~

~~12. The semiconductor memory device according to claim 7, wherein the semiconductor film is a continuous film formed in the semiconductor layer and in the first conductive layers.~~

~~13. The semiconductor memory device according to claim 7, comprising an oxide film interposed between the semiconductor layer and the charge storage film.~~

~~14. The semiconductor memory device according to claim 7, wherein a part of the semiconductor layer that is in contact with the charge storage film includes an n-type impurity.~~

~~15. The semiconductor memory device according to claim 7, comprising~~

~~a first structure and a second structure, each~~

including the semiconductor film and the charge storage film;

a first contact provided on an upper surface of the first structure and extending in the first direction;

a second conductive layer provided on an upper surface of the first contact and extending in a second direction;

a second contact provided on an upper surface of the second structure and extending in the first direction; and

a third conductive layer provided on an upper surface of the second contact and extending in the second direction,

wherein the second conductive layer and the third conductive layer are arranged at different positions along the first direction.

16. A method of manufacturing a semiconductor memory device, comprising:

forming a first hole in a semiconductor substrate, and forming a first semiconductor film at a position inside the first hole and separated from a side surface of the first hole;

sequentially forming an insulating film and a first sacrificial member in the first hole in which the first semiconductor film is formed;

forming a plurality of second sacrificial members stacked in a first direction above the semiconductor substrate and the first sacrificial member;

~~forming a second hole which penetrates through the second sacrificial members to reach the first sacrificial member, and removing the first sacrificial member;~~

~~sequentially forming a charge storage film and a second semiconductor film in the second hole from which the first sacrificial member has been removed; and~~

~~replacing the second sacrificial members respectively with conductive layers.~~

~~17. The method of manufacturing a semiconductor memory device according to claim 16, wherein the forming the insulating film includes oxidizing the semiconductor substrate.~~

~~18. The method of manufacturing a semiconductor memory device according to claim 16, further comprising~~

~~forming a diffusion region in the first hole, after forming the first semiconductor film and before forming the insulating film.~~