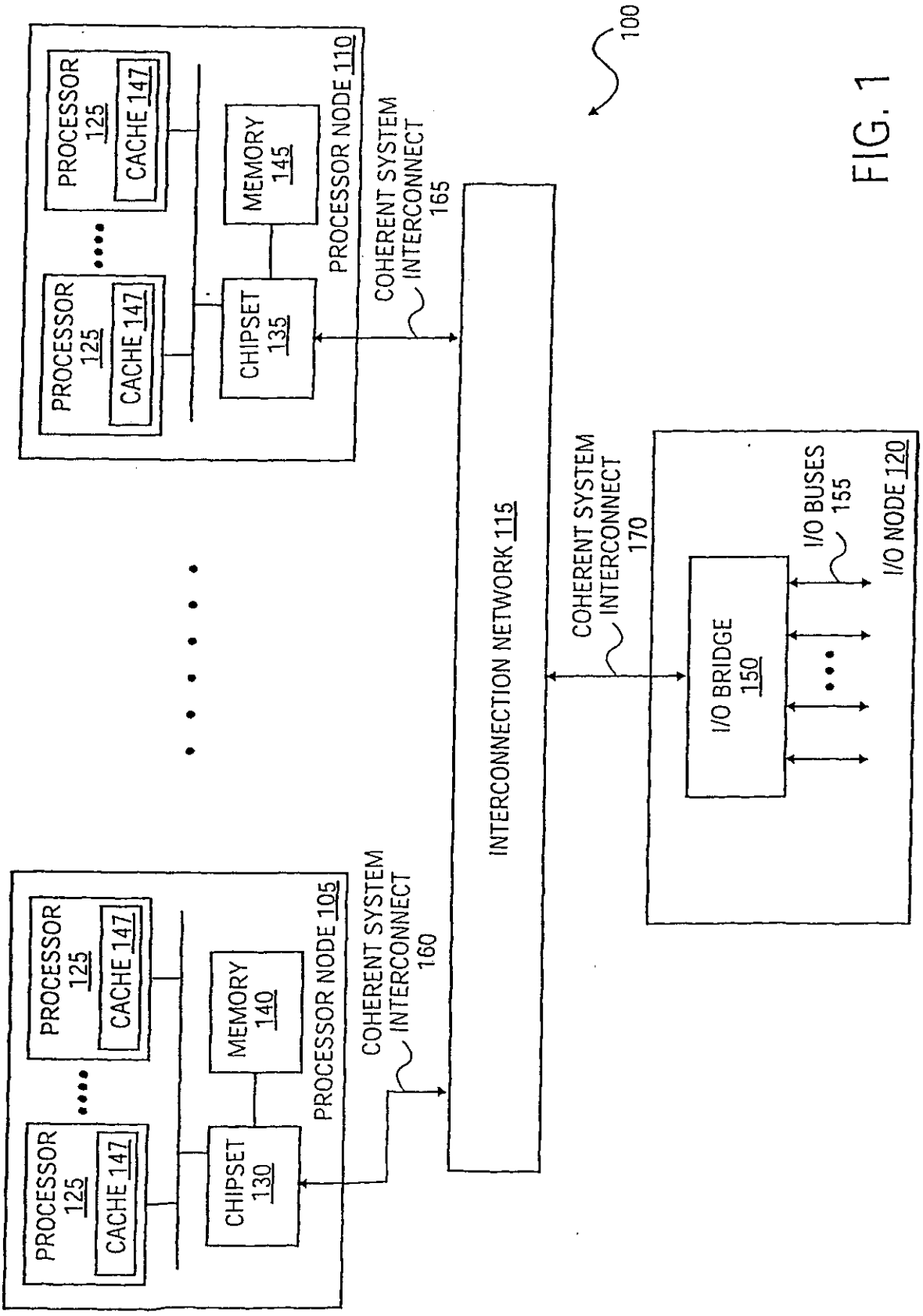

100
PROCESSOR NODE 110
PROCESSOR 125
CACHE 147
MEMORY 145
CHIPSET 135
COHERENT SYSTEM INTERCONNECT 165
INTERCONNECTION NETWORK 115
COHERENT SYSTEM INTERCONNECT 170
I/O BRIDGE 150
I/O BUSES 155
I/O NODE 120
PROCESSOR NODE 105
MEMORY 140
CHIPSET 130
COHERENT SYSTEM INTERCONNECT 160

FIG. 1

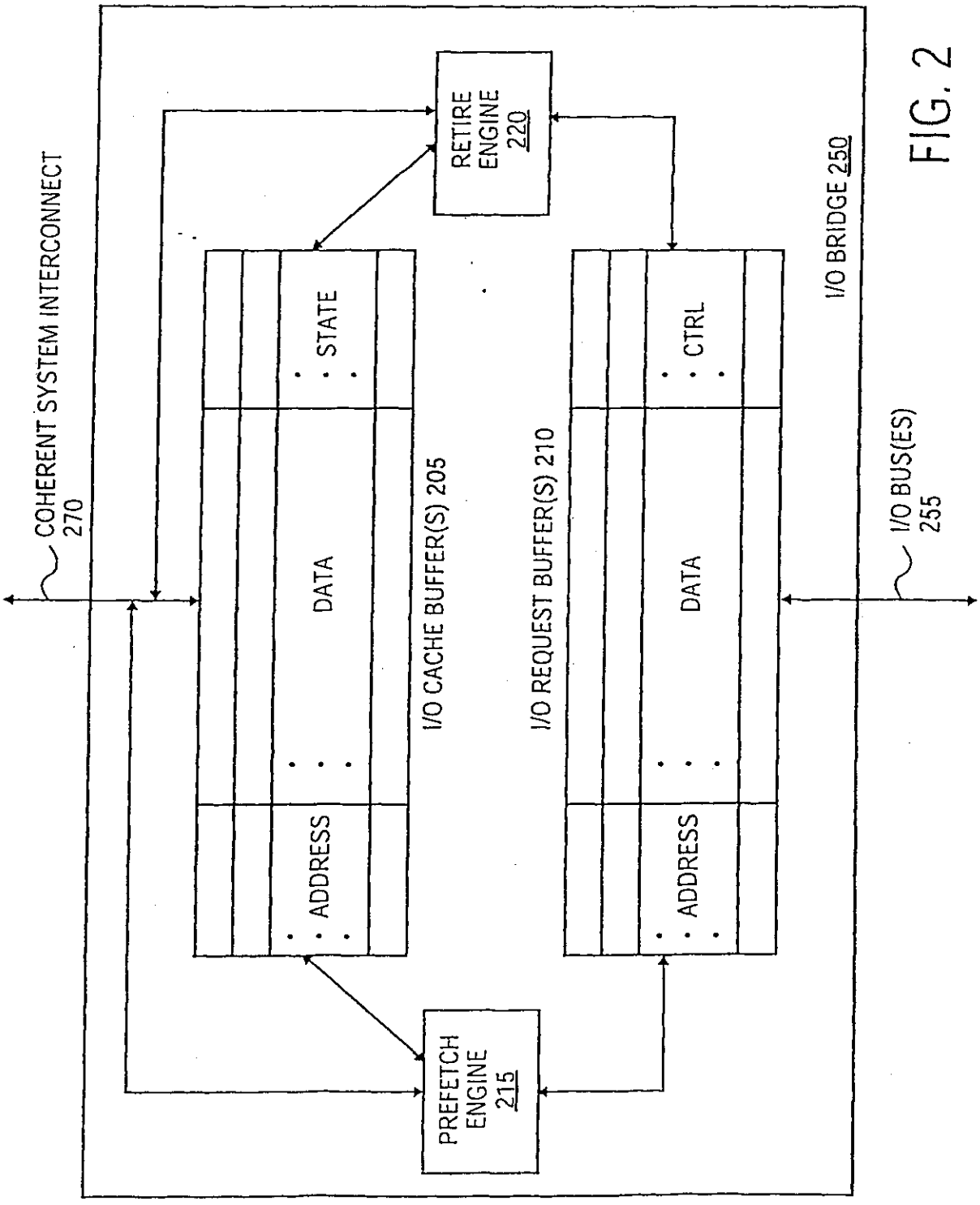

COHERENT SYSTEM INTERCONNECT 270
RETIRE ENGINE 220
I/O BRIDGE 250
STATE
DATA
ADDRESS
I/O CACHE BUFFER(S) 205
CTRL
DATA
ADDRESS
I/O REQUEST BUFFER(S) 210
I/O BUS(ES) 255
PREFETCH ENGINE 215

FIG. 2

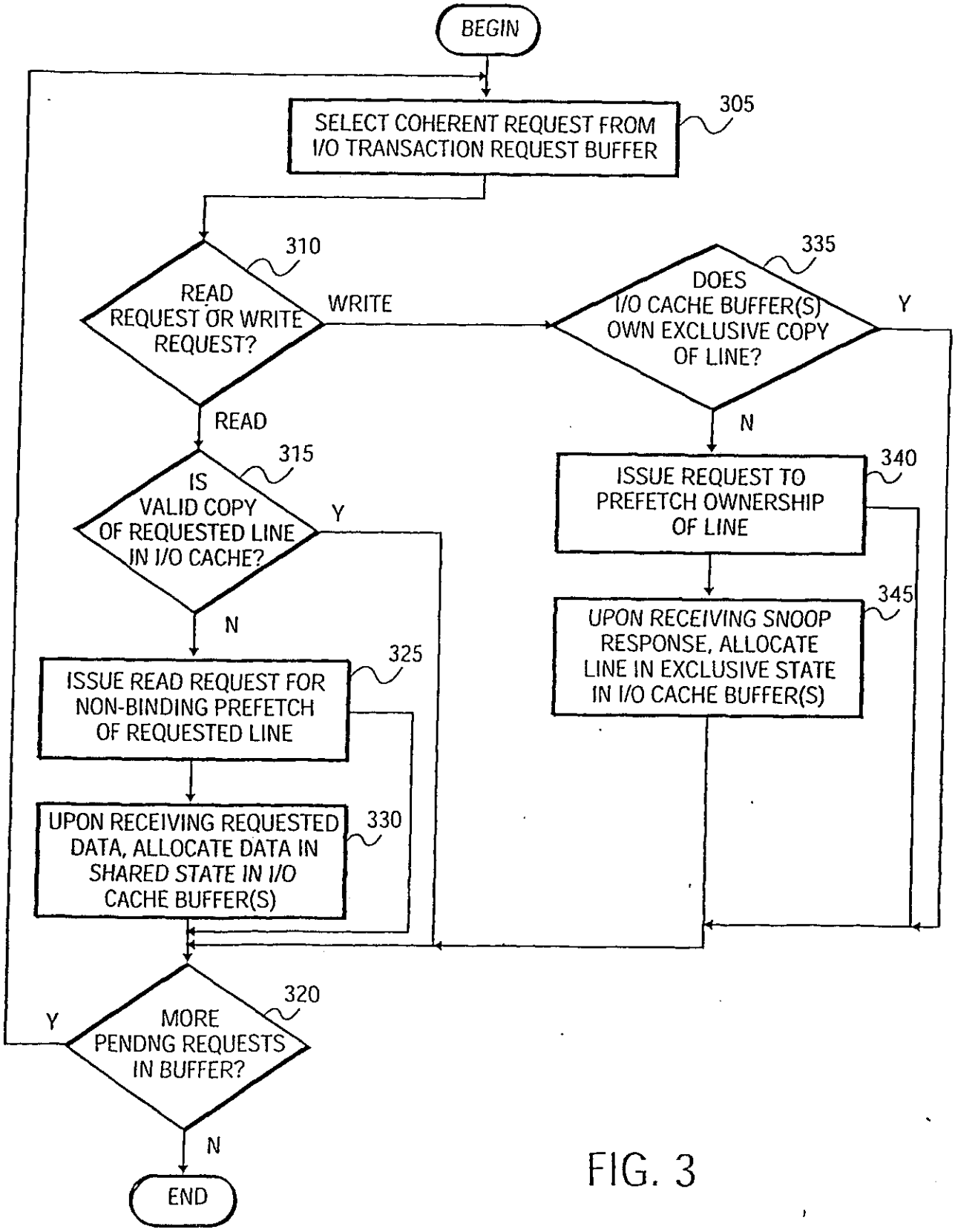

BEGIN
SELECT COHERENT REQUEST FROM I/O TRANSACTION REQUEST BUFFER
305
310
READ REQUEST OR WRITE REQUEST?
WRITE
READ
335
DOES I/O CACHE BUFFER(S) OWN EXCLUSIVE COPY OF LINE?
Y
N
315
IS VALID COPY OF REQUESTED LINE IN I/O CACHE?
Y
N
340
ISSUE REQUEST TO PREFETCH OWNERSHIP OF LINE
345
UPON RECEIVING SNOOP RESPONSE, ALLOCATE LINE IN EXCLUSIVE STATE IN I/O CACHE BUFFER(S)
325
ISSUE READ REQUEST FOR NON-BINDING PREFETCH OF REQUESTED LINE
330
UPON RECEIVING REQUESTED DATA, ALLOCATE DATA IN SHARED STATE IN I/O CACHE BUFFER(S)
320
MORE PENDNG REQUESTS IN BUFFER?
Y
N
END

FIG. 3

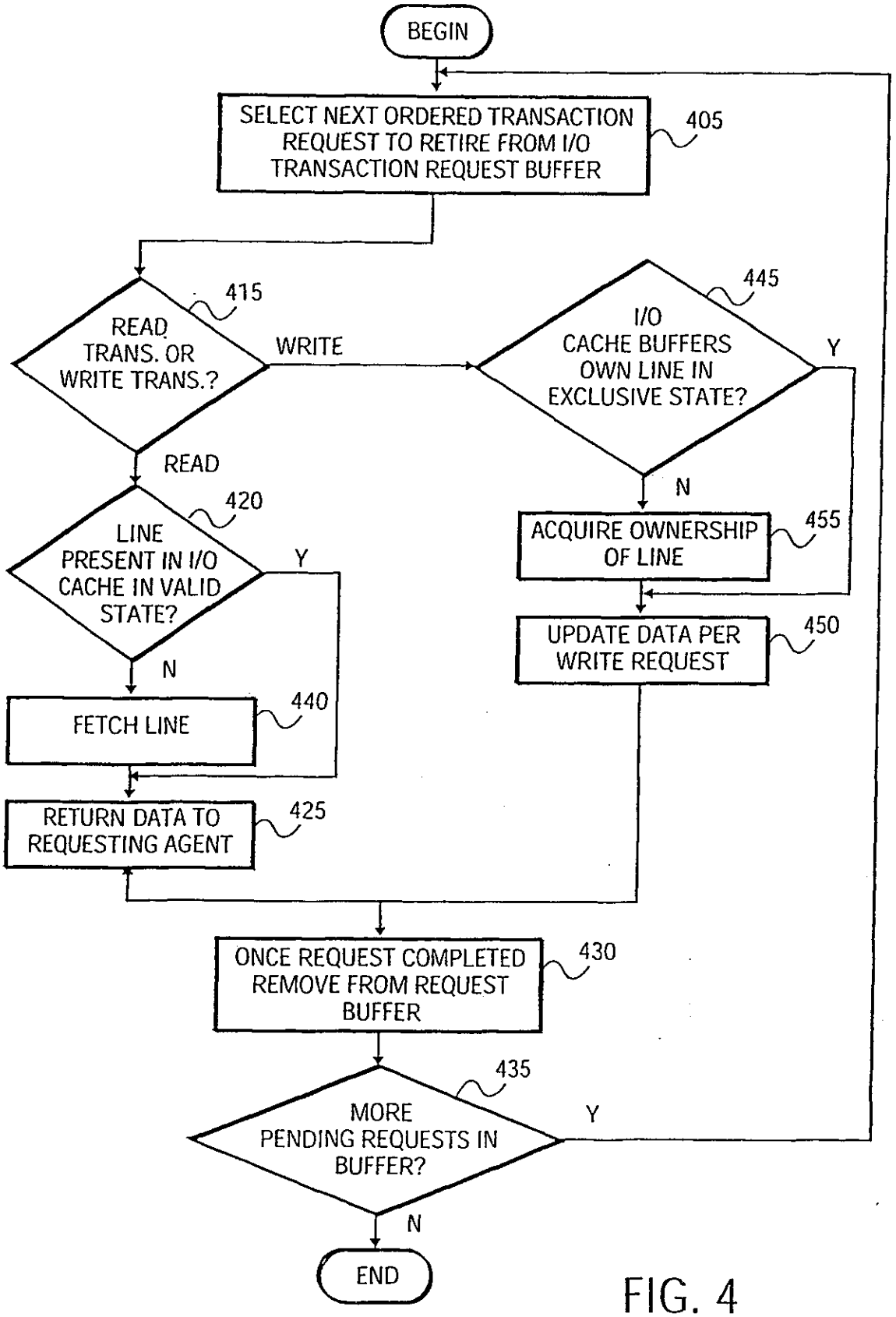

BEGIN
SELECT NEXT ORDERED TRANSACTION REQUEST TO RETIRE FROM I/O TRANSACTION REQUEST BUFFER
405
READ TRANS. OR WRITE TRANS.?
415
WRITE
READ
I/O CACHE BUFFERS OWN LINE IN EXCLUSIVE STATE?
445
Y
N
LINE PRESENT IN I/O CACHE IN VALID STATE?
420
Y
N
ACQUIRE OWNERSHIP OF LINE
455
UPDATE DATA PER WRITE REQUEST
450
FETCH LINE
440
RETURN DATA TO REQUESTING AGENT
425
ONCE REQUEST COMPLETED REMOVE FROM REQUEST BUFFER
430
MORE PENDING REQUESTS IN BUFFER?
435
Y
N
END

FIG. 4

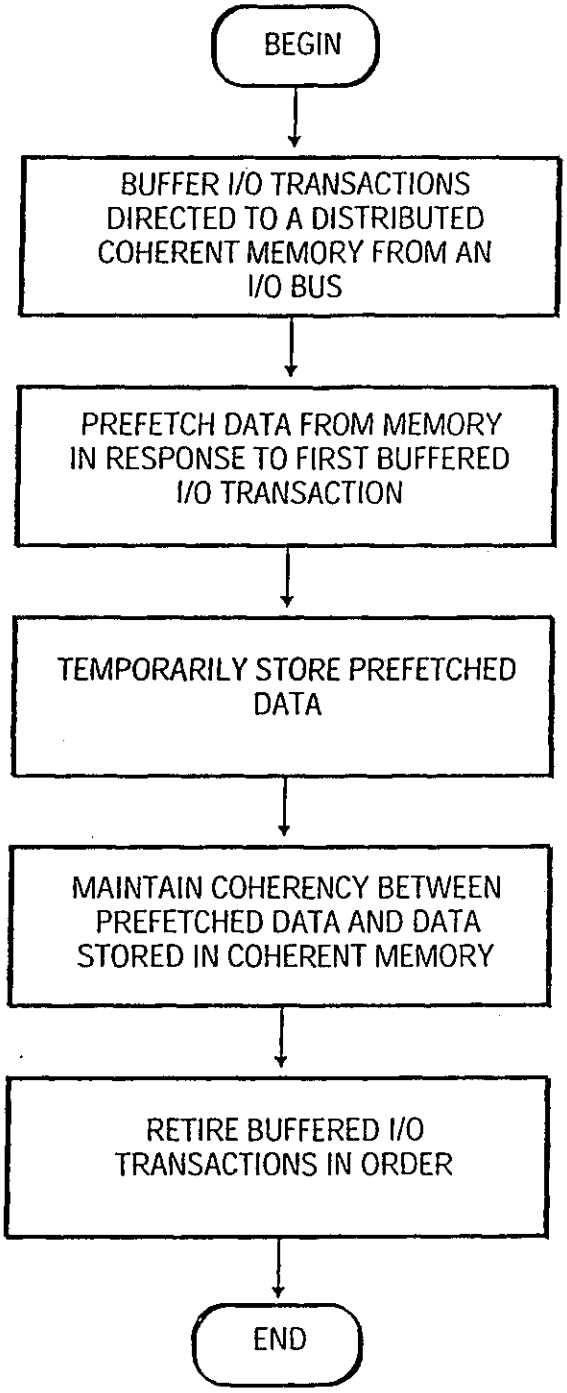

BEGIN
BUFFER I/O TRANSACTIONS DIRECTED TO A DISTRIBUTED COHERENT MEMORY FROM AN I/O BUS
PREFETCH DATA FROM MEMORY IN RESPONSE TO FIRST BUFFERED I/O TRANSACTION
TEMPORARILY STORE PREFETCHED DATA
MAINTAIN COHERENCY BETWEEN PREFETCHED DATA AND DATA STORED IN COHERENT MEMORY
RETIRE BUFFERED I/O TRANSACTIONS IN ORDER
END

FIG. 5