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INTEGRATED CIRCUIT INDUCTOR

TECHNICAL FIELD OF THE INVENTION

5 This invention relates to a method of forming an inductor in an integrated circuit, and to an integrated circuit including an inductor.

BACKGROUND OF THE INVENTION

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Integrated circuits are widely used in electronic devices of many types. It is very often necessary in such integrated circuits to be able to integrate an inductor, that is, a circuit component whose inductance is the most important part of its impedance.

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In particular, it is useful in the manufacture of radio frequency devices, for example integrated radio frequency transceivers, to integrate inductors. Moreover, as radio frequency devices are required to operate at higher frequencies, with higher performance requirements in terms of their efficiency, it becomes useful to be able to integrate inductors having larger inductance values.

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An inductor is formed by providing a conductive, usually metal, element on the semiconductor substrate, on which the other circuit components are formed.

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The performance of an inductor can be measured in terms of its quality factor, or Q value, which is a measure of the amount of energy, supplied to the inductor, which is lost. This depends on the electrical resistance of the conductive element, and on the amount of energy which is lost to the semiconductor substrate. It is therefore advantageous to be able to reduce the resistance and the energy lost in this way.

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In general, efforts at enhancing the Q value have involved modest reductions in the series resistance of the component, or elimination of substrate loss effects. These methods include the use of, for
5 example: additional relatively thick gold or copper metallization, multiple metal layers in parallel, bulk micromachining techniques to remove resistive material underneath the inductor, insulating or high resistivity substrates, or spun-on thick dielectrics above the
10 substrate to physically separate the inductor from the lossy silicon substrate.

Prior art US Patent No. 5,539,241, to Abidi, et al, discloses a method of forming an inductor on an insulating oxide layer above a semiconductor substrate,
15 and subsequently removing the semiconductor substrate by means of a wet etching process, leaving the inductor suspended. The loss of energy to the substrate is therefore reduced.

However, this method cannot be implemented using
20 standard CMOS process steps.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method of forming an inductor on a semiconductor device, and a semiconductor device having such an
25 inductor.

It is a further object of the invention to allow an inductor to be formed using standard CMOS process steps.

The method according to the invention includes the
30 steps of etching a pit to a first depth into the isolating layer and the semiconductor substrate; filling the pit with low dielectric constant material; and forming an inductor element to a second depth within or above the pit, the second depth being less
35 than the first depth, and the inductor element being

formed by a damascene process.

According to further aspects of the invention, there is provided a process for forming an inductor on a silicon substrate, with a pit filled with a low dielectric constant material to reduce the loss of energy to the substrate, and using a dual damascene structure to reduce the resistance by providing relatively thick metal for the inductor. A deep inductor trench is obtained simultaneously during the via etching. The depth of the inductor can thus be adjusted by via over-etch percentage since there is no metal stopping layer underneath it. The pit is obtained after completion of the pre-metal deposition, or the first inter-metal dielectric chemical mechanical polishing by masking the inductor area and etching down to a prescribed depth into the silicon substrate.

There is thus provided a fully CMOS compatible process to insert a pit underneath the inductor and to eliminate an additional thick metal layer to form the inductor.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, and to show how it may be put into effect, reference will now be made to the accompanying drawings, in which:-

Figure 1 is a partial cross-sectional view showing an initial state of a device in a process according to the invention.

Figure 2 is a partial cross-sectional view showing the device of Figure 1 at a later stage in a process according to the invention.

Figure 3 is a partial cross-sectional view showing the device of Figure 1 at a later stage in a process according to the invention.

Figure 4 is a partial cross-sectional view showing the device of Figure 1 at a later stage in a process

according to the invention.

Figure 5 is a partial cross-sectional view showing the device of Figure 1 at a later stage in a process according to the invention.

5 Figure 6 is a partial cross-sectional view showing the device of Figure 1 after completion of a process according to the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

10 Figure 1 shows a semiconductor device 10 during a CMOS manufacturing process. It will be appreciated that Figure 1 shows just a small part of what may be a large integrated circuit device. The device has a semiconductor substrate 12, for example of silicon. A layer of insulating oxide 14 is above the substrate, and a dielectric layer 16 is formed on that. Figure 1
15 schematically shows a plurality of active component isolation regions 18 formed on the silicon 12.

Figure 2 shows the device 10 after the next processing step. The desired location of the inductor is uncovered by a mask, and the area is etched, in a
20 dry etch process, through the dielectric 16, oxide 14 and substrate 12. This etching forms a pit 20. The depth of the pit can be selected to give the required properties of the final product, but may for example be
25 in the range of 5-10 μm .

Figure 3 shows the device 10 after the next processing step. The pit 20 is filled with a low dielectric constant material 22, which also surrounds the pit. The material 22 is preferably an oxide, such
30 as silicon dioxide, but any suitable material can be used, with a dielectric constant which gives the required properties of the final device.

Figure 4 shows the device 10 after the next processing step. This step involves planarizing the
35 upper surface of the device using a known technique

such as etchback or chemical-mechanical polishing (CMP), with a nitride stop layer.

Figure 5 shows the device 10 after the next processing step. This involves the formation of a conventional first metal layer, preferably using tungsten for contact plug 24 and aluminum for connection 26, and the deposition of dielectric stack 28 for dual damascene structure 30 with via 30a and trench 30b. The dielectric stack 28 can be formed of oxide, with or without nitride as trench etching stop-layer.

More particularly, it involves the simultaneous formation of the via and of a deep trench 32 for the inductor (which may be a spiral inductor, or may have any other desired shape in plan view) within the pit 20 filled with oxide 22, using a dual damascene via first etching approach. The depth difference between inductor trench and via can be adjusted by controlling the etching aspect ratio dependent effect and via over etching percentage.

Figure 6 shows the device 10 after the next processing step. This involves the formation of an inductor 42 and of the necessary connections 40 and 50 therefor in dual damascene process, using copper for example as the metal, using nitride for example as capping layer 34 and with additional oxide insulation 36. As is conventional, the dual damascene process involves two cycles of lithography and dry etching, a copper deposition step, removal of excess metal by chemical mechanical polishing, and capping of the exposed copper surface. There is therefore formed an inductor as shown in Figure 6, in which the conductive element 42 of the inductor, filling the trench, is electrically isolated by the low dielectric constant material 22 from the semiconductor substrate 12,

thereby reducing loss of energy to the substrate, to any large degree. The degree of electrical isolation of the inductor element 42 from the substrate 12 can be made as large as is required in the circumstances, by
5 controlling the depth of the pit 20, in the dry etching step described with reference to Figure 2, and by selecting a material 22 to fill the pit with a suitably high resistivity. Moreover, this is achieved without requiring an additional metal layer.

10 In this illustrated example, the inductor is formed above and partially within the pit. However, in accordance with the invention, the inductor may be formed entirely above the pit. For example, in the case of a 0.18 μ m system-on-a-chip process, implemented
15 with more than three (for example, six) metal layers, the inductor can be formed with the top metal layer, entirely above the pit. In such a case, the pit is still isolated by the pit.

The invention thus provides, using standard sub-
20 micron CMOS processes, an inductor having desirable characteristics.

CLAIMS

1. A process of forming an inductor in an integrated circuit, the integrated circuit having a semiconductor substrate and an isolating layer thereon, the process comprising:

etching a pit into the isolating layer and the semiconductor substrate;

filling the pit with low dielectric constant material;

forming an inductor element within or above the pit, by a damascene process.

2. A process according to claim 1, wherein the pit is formed by a dry etching process.

3. A process according to claim 1, wherein the pit has a depth selected to give desired performance characteristics.

4. A process according to claim 1, wherein the pit is filled with a material having a dielectric constant selected to give desired performance characteristics.

5. A process according to claim 1, wherein the inductor element is formed within or above the pit by a dual damascene process.

6. A process according to claim 1, wherein the inductor element is formed partially within the pit.

7. A process according to claim 1, wherein connections for the inductor element are formed above the pit by a dual damascene process.

8. A semiconductor device, comprising;
a semiconductor substrate and an isolating layer
thereon:

5 a pit, etched into the isolating layer and the
semiconductor substrate, and filled with a low
dielectric constant material; and

an inductor element within or above the pit, the
inductor element being formed by a damascene process.