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HYBRID DIELECTRIC STRUCTURE FOR IMPROVING THE STIFFNESS OF BACK END OF THE LINE STRUCTURES

ABSTRACT

A multi-level, coplanar copper damascene interconnect structure (12) on an integrated circuit chip (10) includes a first planar interconnect layer (14) on an integrated circuit substrate (16) and having a plural line conductors separated by a dielectric material (24) having a relatively low dielectric constant and a relatively low elastic modulus. A second planar interconnect layer (18) on the first planar interconnect layer comprises a dielectric film (26) having an elastic modulus higher than in the first planar interconnect layer (14) and conductive vias (28) therethrough. The vias (28) are selectively in contact with the line conductors. A third planar interconnect layer (20) on the second planar interconnect layer (18) has plural line conductors (22) separated by the dielectric material (24) and selectively in contact with the vias (28).

Figure 1.



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