PROCESS FOR CLEAVING LAYERS OF A WAFER OF MATERIAL

The present invention relates in general to the processing of materials, and more particularly substrates used in electronics, optics and optoelectronics.

More specifically, herein disclosed is a process for cleaving two layers of a wafer along an embrittled surface defined between the two layers, the process comprising a thermal anneal for the purpose of cleaving the wafer comprising said layers.

Processes of the aforementioned type are already known.

In particular, it is known to apply such known processes in order to produce the cleavage of two layers of material from the same substrate, between which an embrittled surface has been previously defined by the implantation of species within the substrate.

The implanted species may be ions or atoms. Thus it is known to implant a substrate of a semiconductor material such as silicon with a species such as hydrogen or helium.

The embrittled surface is determined with respect to the nature of the material, the nature of the species

implanted and the energy of implantation (said embrittled surface typically consisting of a plane parallel to the surface of implantation of the substrate).

It is likewise possible to produce the embrittled surface by any other means known in the art, for example by constructing an intermediate region of porous material between two regions of dense material, by forming an oxide layer embedded into a substrate (for example a SOI-type substrate), or else by bonding together two layers, the bonding area then corresponding to the embrittled surface.

This type of cleaving of two layers detached by an embrittled surface can be used to produce thin layers (the thickness of which may range between a fraction of a micron and several microns), as described, for example, in the document FR 2 681 472.

This document indeed describes a process known by the generic name of SMARTCUT®, the objective of which is to manufacture SOI-type structures (Silicon On Insulator, according to the widely used English terminology). The major steps of this process are as follows:

- Oxidation of a so-called upper silicon plate in order to create an oxide layer (which corresponds to the embedded oxide layer of the SOI structure),
- Implantation of hydrogen ions in said upper plate for the purpose of creating the embrittled surface, and to delimit, on the one hand, by means of this surface, the SOI structure (situated on the side of the embedded oxide) and, on the other hand, a silicon residue,
- Bonding of the upper plate onto a supporting plate (which may be made of silicon, but also of another material),

- Cleaving and detachment anneal, for the purpose of:
  - cleaving on one hand a SOI structure comprising the supporting plate, the embedded oxide layer and the silicon layer situated between the embedded oxide and the embrittled surface and, on the other hand, the silicon residue situated on the other side of the embrittled surface. In addition, upon completion of the cleaving process, cohesive forces may still exist between the two layers, which thereby remain integral with one another.
  - Detaching the two layers, i.e., physically disconnecting them, in addition to cleaving,
- Additional treatment intended to reduce the surface roughness of the SOI resulting from the cleaving and detachment processes.

Hereinafter within this text, the structures to be detached, and the layers constituting them that are detached will be designated by the generic term "wafer," which corresponds to the French term "tranche".

The surface condition of the wafers is an extremely important factor, very stringent specifications being imposed with respect to the subsequent use of the wafers following the detachment process, for example, in order to form electronic, optical or optoelectronic components.

This surface condition is characterized, in particular, by the surface roughness of the wafers following detachment.

It is therefore common to find specifications for roughness which must not exceed 5 Angströms expressed as a RMS value (corresponding to the English acronym for "root mean square").

The measurements of roughness are generally made with an atomic force microscope (AFM according to the acronym corresponding to the English name of Atomic Force Microscope).

With this type of device, the roughness of surfaces scanned by the tip of the AFM microscope is measured, ranging from 1x1 μm^2 to 10x10 μm^2 and more rarely 50x50 μm^2, or even 100x100 μm^2.

It is also made clear that it is possible to measure the surface roughness using other methods, in particular by means of a "haze" measurement, according to the widely used English terminology. In particular, this method has the advantage of making it possible to quickly characterize the uniformity of the roughness over an entire surface area.

This haze, measured in ppm, is the result of a method which utilizes the optical reflection properties of the surface being characterized, and corresponds to an optical "background noise" diffused by the surface, by reason of its microroughness.

An example of the relationship between haze and roughness, in the case of the surface of a SOI, is illustrated in figure 1.

It is indicated that the haze measurements that will be provided in this text are taken according to the same protocol and by means of the same device, in this case an instrument of the KLA Tencor Surfscan SPI type (registered trademark).

It is likewise indicated that the SMARTCUT®-type process can also be used to form structures other than SOI structures, for example SOA structures (Silicon On Anything according to the widely used English

terminology), or even AOA structures (Anything on Anything according to the widely used English terminology).

Cleaving and detachment anneals are conventionally carried out in annealing furnaces the configuration of which is illustrated in figure 2. Furnaces such as this are capable of simultaneously processing a plurality of wafers.

Figure 2 thus shows a plurality of wafers 10 arranged on a receptacle 11 such as a quartz boat, the wafers being aligned in parallel.

The boat 11 is itself place on a loader 12 fastened to a door 13 for sealing the mouth of the furnace.

The assembly 100 formed by the door 13, the loader 12 and the boat and the wafers supported by the loader is capable of moving in relation to an furnace structure 20 which comprises a quartz processing tube 21 around which a heating element 22 is wound.

A pyrometer tube 23 equipped with thermocouples is likewise provided.

The furnace of figure 2 is shown in open position.

In closed position, the assembly 100 is inserted into the furnace structure 20, the door 13 blocking the mouth of the furnace.

Inside of each wafer to be detached, the two layers forming the wafer face each other so that the useful surfaces, for which it is desired to control the surface condition in an extremely precise manner, are placed face-to-face.

Therefore, it is particularly important to take measures to ensure the best possible surface condition (specifically roughness) for these useful surfaces.

Returning to the prior art illustrated in figure 2, the wafers to be detached are therefore arranged vertically.

In this way, the two layers of each wafer being detached are prevented from moving and do not move in relation to one another (specifically following the detachment process, when the detached layers are removed from the furnace).

A relative movement of the two layers such as this might actually run the risk of producing scratches on the surfaces of the detached layers.

And it is likewise very important that the surface condition (and in particular the roughness) of these layers be as even as possible, on the surface of the layer.

Figure 3 illustrates the surface roughness of a SOI wafer after detachment, following a cleaving anneal that has been carried out in a conventional manner in an annealing furnace, as shown in figure 2.

The roughness is represented by means of a haze measurement.

This figure illustrates a dissymmetry in the roughness of the SOI structure, which corresponds to a lower haze on the part of the SOI structure located at the bottom part of the furnace (the so-called "notch" of the SOI structure, which is placed on the bottom during annealing, being situated to the left, at 9-o'clock in figure 3).

Thus, it appears that if known detachment anneals actually make it possible to prevent movements capable of leading to the formation of scratches, they promote

irregularities in the surface roughness of the layers resulting from the detachment process.

This constitutes a disadvantage to which the invention intends to respond.

According to a first aspect of the invention, there is provided a process for cleaving of two layers of a wafer along an embrittled surface defined between the two layers, the process comprising a thermal anneal for the purpose of cleaving the wafer comprising said layers, characterized in that said wafer is arranged in a substantially horizontal position during the annealing process.

Some preferred but nonlimiting features of this process are as follows:

- the structure is placed inside of a chamber between two heating electrodes,
- means are provided for handling the layers of material in a horizontal position,
- said handling is carried out individually for each wafer,
- said handling is carried out individually for each layer,
- a plurality of wafers are annealed simultaneously, each wafer being placed between two heating electrodes.

An embodiment of the invention provides for cleaving two layers of material delimited by an embrittled surface, said embrittled surface having been produced by means of a SMARTCUT®-type process.

Preferred but nonlimiting features of such an application are as follows:

- the two layers of material comprise a silicon layer,

- the two layers of material are two silicon layers, one of the two layers corresponding to the surface layer of a SOI structure, the other layer corresponding to a silicon residue.

According to a second aspect of the invention, there is provided an annealing device for cleaving a wafer, comprising a furnace capable of accommodating at least one wafer, characterized in that each wafer is held inside of a chamber in horizontal position, with the result being that the cleaving anneal is carried out while the wafer is in horizontal position.

In one variant, the device also comprises means for handling the wafers and/or the layers which constitute said wafers, in horizontal position.

Other features, objectives and advantages of the invention will become more apparent upon reading the following description of one embodiment of the invention, made with reference to the appended drawings in which, other than figures 1 to 3 which have already been commented on with reference to the prior art:

- figure 4 is a schematic representation of a facility for carrying out cleaving anneals, enabling implementation of the invention,

- figures 5a and 5b represent, respectively, spatial distributions of haze on the surface of two SOI structures, the SOI structure of figure 5a having undergone a cleaving anneal in a furnace customarily used for this purpose, according to prior art, the SOI of figure 5b having itself undergone a cleaving anneal while being disposed horizontally inside its annealing furnace, according to the invention.

With reference now to figure 4, a furnace 30 has been shown which is used according to the invention for carrying out the cleaving anneal of a plurality of wafers 10.

More specifically, each wafer 10 is placed inside a chamber 31 formed by two adjacent electrodes 32 of a plurality of electrodes in the furnace 30.

And these electrodes 32, which run parallel to each other in a horizontal direction, define horizontal chambers 31, each of which is capable of accommodating one wafer 10 to be detached, in horizontal position.

Heating is ensured by a gas which penetrates into the chambers 31 by way of respective inlets 310, this gas itself being heated by the electrodes delimiting each chamber.

It should be noted that the "heating" gas may be used solely for the purpose of diffusing the heat coming from the electrodes onto the wafers. It may also have been preheated, prior to its introduction into the furnace.

The specific configuration of the "horizontal" furnace used according to the invention for carrying out a cleaving anneal makes it possible to eliminate the effects of a temperature gradient inside the furnace, between the top and bottom parts of the furnace.

This leads to a substantial improvement in the evenness of the surface roughness of the layers, after they have been detached.

In this regard, the effect of using a "horizontal" furnace according to the invention, for the purpose of a cleaving anneal, has been illustrated in figures 5a and 5b.

Figure 5a shows the distribution of haze on the surface of a detached SOI structure following a conventional cleaving anneal in a "vertical" furnace, as illustrated in figure 2.

This figure, which is analogous to figure 3, reveals a "dense region" corresponding to an irregularity in roughness in the lower right part of the layer.

Conversely, figure 5a shows the perfectly symmetrical roughness of a SOI detached after a cleaving anneal carried out in a "horizontal" furnace according to the invention.

And this roughness no longer exhibits the characteristic of a "dense region" as observed in the case of the SOI structure of figure 5a.

Thus it appears that the use of a "horizontal" furnace according to the invention makes it possible to overcome the problems associated with a "dense region" of roughness as mentioned above with respect to prior art cleaving anneals.

In addition, it indicated that provisions are also made, in the case of the "horizontal" furnace of figure 4, to prevent any movement of the layers which might produce scratches, in particular when the detached layers are being unloaded from the oven.

In this regard, a handling robot 40 has been shown in figure 4, which is capable of :

- individually grabbing :

  ➢ the wafers in order to introduce them into the furnace, and

  ➢ the detached layers, in order to take them out of the oven after cleaving. In addition, it is also possible to anticipate carrying out only a cleaving

anneal without completing the detachment of the wafers, it being possible to complete this detachment outside of the furnace after the robot 40 has unloaded the cleaved wafers (for example, by means of a mechanical action),

- and of moving in one direction 41 (as well as in a "vertical" direction perpendicular thereto) in order to carry out the necessary loading and unloading operations (while processing each wafer individually),

➢ it is added that, in the case where the detachment of the two layers of the wafer is actually carried out during annealing, the two layers of the wafer that are detached may be unloaded by the robot separately. In this regard, the arm 42 of the robot which grabs the wafers and/or the layers may comprise a means such as a suction cup capable of being placed under partial vacuum selectively, or else a means handling the wafers by their edges in order to grab each layer separately from the layer from which it has been detached, or else a means enabling the two layers to be handled simultaneously with a view to detaching them outside of the furnace.

The wafers and layers remain horizontal while the robot 40 is carrying out these handling operations.

In addition, if the above examples were described with reference to a cleaving operation making it possible to produce a SOI structure, in particular by means of a SMARTCUT®-type process, the invention applies to the cleaving of any structure which includes an embrittled surface making it possible to delimit layers.

CLAIMS

1. Process for cleaving two layers of a wafer along an embrittled surface defined between the two layers, the process comprising a thermal anneal for the purpose of cleaving the wafer comprising said layers, characterized in that said wafer is arranged in a substantially horizontal direction during the annealing process.

2. Process according to the preceding claim, characterized in that the structure is placed inside a chamber between two heating electrodes.

3. Process according to one of the preceding claims, characterized in that means are provided for handling the layers of material in a horizontal position.

4. Process according to the preceding claim, characterized in that said handling is carried out individually for each wafer.

5. Process according to one of the preceding claims, characterized in that said handling is carried out individually for each layer.

6. Process according to one of the preceding claims, characterized in that a plurality of wafers are annealed simultaneously, each wafer being placed between two heating electrodes.

7. Application of a process according to one of the preceding claims, for cleaving two layers of material delimited by an embrittled surface, said embrittled surface having been produced by means of a SMARTCUT®-type process.

8. Application according to the preceding claim, characterized in that the two layers of material comprise a silicon layer.

9. Application according to one of the preceding claims, characterized in that the two layers of material are two silicon layers, one of the two layers corresponding to the surface layer of a SOI structure, the other layer corresponding to a silicon residue.

10. Annealing device for cleaving a wafer, comprising a furnace capable of accommodating at least one wafer, characterized in that each wafer is held inside of a chamber in horizontal position, with the result being that the cleaving anneal is carried out while the wafer is in horizontal position.

11. Device according to the preceding claim, characterized in that the device also comprises means for handling the wafers and/or the layers which constitute said wafers, in horizontal position.

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ABSTRACT

The invention relates to a Process for cleaving two layers of a wafer along an embrittled surface defined between the two layers, the process comprising a thermal anneal for the purpose of cleaving the wafer comprising said layers, characterized in that said wafer is arranged in a substantially horizontal direction during the annealing process.

The invention also relates to the application of this process and an associated device (30).

FIGURE 1