WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first conductive gate contact;

a first contact insulating pattern surrounding the first conductive gate contact;

a first conductive pattern surrounding the first contact insulating pattern; and

a second conductive pattern disposed over the first conductive pattern, the second conductive pattern surrounding the first conductive gate contact,

wherein the second conductive pattern includes:

a first edge part overlapping with the first contact insulating pattern, the first edge part being in contact with the first conductive gate contact; and

a first base part, spaced apart from the first conductive gate contact by the first edge part, extending from the first edge part and away from the first conductive gate contact, and the first base part being thicker than the first edge part, and

wherein the first edge part is disposed lower level than a top surface of the first base part.

2. The semiconductor memory device of claim 1, wherein the first conductive pattern includes:

a second base part overlapping with the first edge part of the

second conductive pattern, the second base part being thicker than the first edge part; and

a second edge part extending from the second base part, the second edge part being thinner than the second base part.

3. The semiconductor memory device of claim 2, further comprising a second conductive gate contact surrounded by the second edge part of the first conductive pattern, the second conductive gate contact having a sidewall in contact with the second edge part.

4. The semiconductor memory device of claim 1, further comprising:

an interlayer insulating layer between the first conductive pattern and the second conductive pattern;

a sidewall insulating layer extending along sidewalls of the first conductive pattern, the second conductive pattern, and the interlayer insulating layer;

a conductive vertical contact on the sidewall insulating layer; and

a blocking insulating layer extending along a surface of each of the first conductive pattern and the second conductive pattern.

5. The semiconductor memory device of claim 4, wherein the blocking insulating layer includes a first opening facing the sidewall insulating layer and a second opening facing the first conductive gate

contact, and

wherein the second opening is narrower than the first opening.

6. The semiconductor memory device of claim 1, further comprising:

a dummy contact penetrating the first conductive pattern and the second conductive pattern;

a second contact insulating pattern disposed between the dummy contact and at least one of the first conductive pattern and the second conductive pattern; and

an upper insulating layer on a top surface of the dummy contact.

7. A method of manufacturing a semiconductor memory device, the method comprising:

forming a preliminary stepped stack structure including a lower interlayer insulating layer, a middle interlayer insulating layer, an upper interlayer insulating layer, a lower sacrificial layer including a lower base part between the lower interlayer insulating layer and the middle interlayer insulating layer and a lower edge part which further protrudes to a side portion than the middle interlayer insulating layer from the lower base part and is thinner than the lower base part, and an upper sacrificial layer including an upper base part between the middle interlayer insulating layer and the upper interlayer insulating layer and an upper edge part which further protrudes to a side portion than the upper

interlayer insulating layer from the upper base part and is thinner than the upper base part;

forming a filling insulating layer covering the preliminary stepped stack structure;

forming a contact hole penetrating the filling insulating layer, the upper edge part, the middle interlayer insulating layer, the lower base part, and the lower interlayer insulating layer;

replacing the upper edge part with a sacrificial pad through the contact hole;

replacing a portion of the lower base part with a contact insulating pattern through the contact hole; and

forming a support structure surrounded by the contact insulating pattern and the sacrificial pad in the contact hole.

8. The method of claim 7, further comprising:

forming a channel hole penetrating the upper interlayer insulating layer, the upper base part, the middle interlayer insulating layer, the lower base part, and the lower interlayer insulating layer;

forming a memory layer along a surface of the channel hole;

forming a channel layer along a surface of the memory layer; and

filling a central region of the channel hole with a core insulating pattern and a capping pattern on the core insulating pattern.

9. The method of claim 8, wherein the support structure includes

the memory layer and the channel layer, which extend to the inside of the contact hole, and a dummy core insulating pattern disposed on the channel layer in the contact hole.

10. The method of claim 9, further comprising:

forming an upper protective layer covering the support structure and the capping pattern such that a void is defined in the contact hole;

forming a slit penetrating the upper protective layer, the upper interlayer insulating layer, the upper base part, the middle interlayer insulating layer, the lower base part, and the lower interlayer insulating layer;

removing the lower sacrificial layer, the upper sacrificial layer, and the sacrificial pad to expose the support structure and the contact insulating pattern;

forming a blocking insulating layer along a surface of a lower gate region in which the lower sacrificial layer is removed and an upper gate region in which the upper sacrificial layer and the sacrificial pad are removed; and

filling a central region of each of the lower gate region and the upper gate region with a conductive pattern.

11. The method of claim 10, further comprising:

exposing a portion of the blocking insulating layer and the contact insulating pattern by removing the support structure;

removing the exposed portion of the blocking insulating layer to expose an edge part of the conductive pattern overlapping with the contact insulating pattern; and

filling a region in which the support structure is removed with a conductive gate contact to be in contact with the edge part of the conductive pattern.