Semiconductor Chip Packaging with Reinforcement Frame

Field of Invention

[0001] The present invention relates to surface mount integrated circuit device assembly. In particular, the invention relates to a system and method for improving the reliability of solder joints of semiconductor device by reducing the failure rate caused by mechanical shocks and thermal cyclic stresses.

Background

[0002] Solder joints are used widely in the semiconductor industry for forming physical and electrical connections between device components. Such device components may be, for example, a semiconductor chip package, an integrated circuit substrate or a semiconductor wafer die, and a printed circuit board. Typically, the solder joints are formed by depositing solder onto a surface of at least one of the device components to be joined together followed by solder reflowing in a convectional oven.

[0003] Typically, the device components joined together by a solder joint, such as a semiconductor chip package and printed circuit board (PCB), are made of different materials. As a result, these device components have different coefficients of thermal expansion. Consequently, the solder joints are subject to stresses and strains as the device undergoes thermal cycles during device fabrication, reliability testing and functional operation. FIG. 1A illustrates, in a simplified manner, a side view of a ball grid array (BGA) package 10 mounted on a PCB 14 by means of solder ball joints 18. FIG. 1B illustrates the BGA package 10 in FIG. 1A after thermal deformation. As can be seen from FIG. 1B, the solder ball joints 18 further from the neutral axis of deformation, i.e. near the center of the BGA, undergo higher deformations and stresses. Such cyclic stresses often lead to internal component-level failure at the joints between the wafer die and substrate

and/or board-level failure at the solder joints between a semiconductor package and the PCB.

[0004] In addition to thermal cycle stresses, an electronic device incorporating a semiconductor chip package soldered on a printed circuit board is desired to withstand some amount of impact shocks. This is especially true for mobile and handheld devices, which are more likely to be dropped inadvertently from a height. FIG. 2A illustrates a BGA package 10 mounted on a PCB 14 with the PCB supported between spaced-apart screw mountings (not shown in the figure). As shown in FIG. 2A, the PCB 14 bends upwards when mechanical shock is applied to the PCB in one direction. In another mechanical shock direction or as a result of vibration of the PCB after an initial shock, the PCB 14 bends in an opposite direction as shown in FIG. 2B. Again, it can be seen that the solder ball joints 18 further away from the neutral axis or center of the BGA experience higher deformations and stresses.

[0005] One significant cause for failures of solder joints is the uneven distribution of thermal cyclic and mechanical impact stresses. Typically, the solder joints around the edges or periphery of the BGA package experience higher stresses, especially those at these peripheral corners and are, thus, the first to fail. Failure of solder joints can be at the component-level or board-level. Component-level failure at the solder-to-die interface may lead to internal substrate or die cracking; such a failure may cause the component to fail to conform to one of its characteristic parameters (so-called parametric failure). Board-level failure at the solder-to-package and solder-to-board interfaces may lead to more serious functional failure.

[0006] To improve on both thermal cycle and mechanical impact reliabilities, attempts have been made to improve the reliability of solder joints. For example, one approach uses an underfill in the space between a surface mount component and its circuit board. Another approach uses a convex surface on a solder pad; the resulting solder joint is claimed to exhibit reduced stress and improved reliability. Another approach provides dummy pads

and dummy patterns formed near outer edges of a semiconductor substrate; these dummy pads and dummy patterns formed larger and stronger solder joints. Another approach uses bonding beads between a BGA package and its PCB to lend strength to the solder joints. Another approach transfers solder positions away from corners of an interconnection pattern or adding solder joints to the periphery of the interconnection pattern to achieve a rounded or chamfered corner pattern.

[0007] It can thus be seen that there exists a need in the semiconductor industry for providing another solution to improve solder joint reliability.

Brief Description of the Drawings

[0008] The present invention will be described by way of non-limiting embodiments of the present invention with reference to the accompanying drawings, in which:

[0009] FIG.1A illustrates a cross-sectional view of a prior art ball grid array (BGA) semiconductor package mounted on a printed circuit board (PCB);
FIG. 1B illustrates the BGA and PCB assembly shown in FIG. 1A undergoing thermal deformation;

[0010] FIGs.2A and 2B illustrate a cross-sectional view of a prior art BGA and PCB assembly with the PCB mounted between spaced apart supports and undergoing vibration bending in two different directions;

[0011] FIG. 3A illustrates a side view of a semiconductor package mounted on a reinforcement frame according to an embodiment of the present invention;
FIG. 3B illustrates a bottom view of the semiconductor package as seen in FIG. 3A;
FIG. 3C is a bottom isometric view of the semiconductor package as seen in FIG. 3A;

FIG. 3D illustrates the reinforcement frame mounted on part of a PCB;

[0012] FIG. 4 illustrates a reinforcement frame according to another embodiment of the present invention;

[0013] FIG. 5 illustrates a use of an embodiment of the present invention with a Cavity Down BGA package;

[0014] FIG. 6 illustrates a use of an over-sized reinforcement frame according to another embodiment of the present invention; and

[0015] FIG. 7 illustrates a use of a reinforcement frame as a heat-sink according to yet another embodiment of the present invention.

Detailed Description

[0016] One or more specific and alternative embodiments of the present invention will now be described with reference to the attached drawings. It shall be apparent to one skilled in the art, however, that this invention may be practised without such specific details. Some of the details may not be described at length so as not to obscure the invention. For ease of reference, common reference numerals or series of numerals will be used throughout the figures when referring to the same or similar features common to the figures.

[0017] The present disclosure describes a surface mount semiconductor package, such as a ball-grid array or flip chip, with improved solder joint reliability. One embodiment of the present invention provides the semiconductor device with a reinforcement frame operable for attachment to a peripheral area around an interconnect pattern.

[0018] Another embodiment of the present invention provides a method for improving solder reliability of a semiconductor package mounted on a printed circuit board or substrate by mounting the semiconductor package on a reinforcement frame and mounting the reinforcement frame on the PCB/substrate.

[0019] In one embodiment, the mounting of the semiconductor package on the reinforcement frame and the mounting of the reinforcement frame on the substrate comprises curing an adhesive disposed on both mounting interfaces. In another embodiment, the mounting between the semiconductor package and the reinforcement frame comprises curing an adhesive while the mounting between the reinforcement frame and the PCB comprises reflowing of solder in an oven. In another embodiment, the mountings are done in either a one-step or two-steps process.

[0020] In another embodiment, the semiconductor package further comprises one or more thermal traces for conducting heat away from a semiconductor die to the reinforcement frame.

[0021] FIG. 3A shows a side view of a BGA semiconductor package 100 according to an embodiment of the present invention. As shown in FIG. 3A, the BGA package 10 is made up of a semiconductor die (not shown) mounted on a substrate 12 and a moulding material 13 encapsulating the semiconductor die to the substrate 12. The configuration, as shown in FIG. 3A, where the die is on the upper side of the substrate 12 is called a "cavity-up" BGA package. Internal to the BGA package 10 are bond wires (not shown in the figures) electrically connecting bond pads on the semiconductor die to bond pads on the substrate 12. Each bond pad on the internal side of the substrate 12 is connected to a solder pad on the external side of the substrate 12. The external side of the substrate 12 may have solder balls 18 attached to or formed on the solder pads. The solder balls may be attached to the BGA package 10 just before the package 10 is mounted on a PCB board. Where a silicon chip is populated with solder bumps 18 pre-formed for external inter-connection, the semiconductor chip package is called a flip chip. The entire BGA moulded package or flip

chip is now referred to simply as a semiconductor package 10 regardless of whether the external inter-connections are provided with solder balls or bumps 18. As shown in FIG. 3A, the semiconductor package 10 is mounted on a reinforcement frame 50 around the interconnect pattern, i.e. on the same side as the solder balls or solder bumps 18.

[0022] In one embodiment, the reinforcement frame 50, as shown in FIG. 3A, is of the same external dimensions or outline as the semiconductor package 10. The thickness of the reinforcement frame may range from about 0.1 mm to about 0.5 mm depending on the dimensions of the semiconductor package 10. As shown in FIGs. 3B and 3C, each reinforcement frame 50 is in the form of a quadrilateral ring. As shown in FIGs. 3A, 3C or 3D, each reinforcement frame 50 has a fully height at each of the four raised corners 54a of the reinforcement frame 50. Each linking member 50a of the reinforcement frame 50 between two adjacent corners 54a has a reduced height of substantially half the full height at the corners such that an inside face 58 of the reinforcement frame 50 remains substantially planar and parallel to a plane joining the raised corners 54a. The step-height face 54 of the reinforcement frame 50 allows conductive interconnect traces 20 on the PCB 14 to reach the respective solder balls lands without any structural interference as shown in FIG. 3D.

[0023] In one embodiment of the reinforcement frame, the reinforcement frame 50 is made of copper. In another embodiment, the reinforcement frame 50 is made of aluminum. The metallic reinforcement frame 50 may be fabricated by chemical etching, for example, using a photolithographic masking and etching process. The half-height thickness at each linking member 50a may be formed by controlling the depth of etching. In another embodiment, the reinforcement frame 50 is formed by stamping or casting, followed by a machining or etching process. Other machining method, such as laser cutting is also possible. In yet another embodiment, the reinforcement frame 50 is made of glass or ceramic.

[0024] In one embodiment before using the reinforcement frame 50, the (inside or upper) planar face 58 of the reinforcement frame 50 is attached to the periphery area of the

moulded semiconductor package 10 surrounding the interconnection pattern of solder balls or solder bumps 18. In one embodiment, the reinforcement frame 50 is attached to the package 10 by means of adhesive and delivered with a reinforcement frame 50 attached to a semiconductor package 10 as an integral device. In another embodiment, the reinforcement frame 50 is delivered as a separate device from a semiconductor package 10.

[0025] In use, adhesive or solder paste is coated on the raised corners 54a of the reinforcement frame 50. The raised corners 54a are then aligned with corresponding attachments areas/lands on the PCB 14 and the solder balls/bumps 18 on the bottom side of the semiconductor package 10 are also aligned with the solder pads on the PCB 14, the reinforcement frame 50 and the semiconductor package 10 are then fixed onto the PCB 14 by allowing the adhesive to cure or reflow the solder balls/bumps 18 in an oven.

[0026] In an embodiment, the adhesive is as epoxy glue. In an embodiment of the present invention, the raised corners 54a of the reinforcement frame 50 and the planar surface 58 are coated with adhesive, and the reinforcement frame 50 and semiconductor package 10 are integrally mounted onto the PCB 14 in a one-step process. In a variation, adhesive is applied to the planar surface 58 and the reinforcement frame 50 is mounted to the semiconductor package 10 by curing the adhesive in a first step and then mounting the semiconductor package-reinforcement frame assembly onto the PCB 14 in a second step. In another variation, the reinforcement frame 50 is mounted onto the PCB 14 in a first step and then the semiconductor package 10 is mounted onto the reinforcement frame 50 in a second step. In any one of these variations, after the adhesive is cured, the semiconductor package 10 and the PCB 14 are connected electrically and mechanically by solder reflowing of the solder balls/bumps 18 in an oven. In a further variation, the mounting of the reinforcement frame 50 onto the PCB 14 is carried out by solder reflowing. In yet another variation, mounting of the reinforcement frame onto the PCB is by solder reflowing while the mounting of the semiconductor package 10 on the reinforcement frame 50 is carried out by curing of an adhesive.

[0027] The reinforcement frame 50 when mounted on a PCB 14 serves as a stress buffer for both mechanical shock and thermal cyclic stresses. The joints between the corners 54a of the reinforcement frame 50 and the PCB 14 provide greater resistance to stresses, such as shear stresses that may be induced by both mechanical shock and thermal cyclic loads, than the resistance to stresses by the solder ball/bump 18 joints. Without the reinforcement frame 50, the shear stresses would have to be taken up by the solder ball/bumps 18 joints, especially those at the corners or periphery away from the neutral axis or center of the semiconductor package 10, thereby resulting in premature failure of the solder ball/bump 18 joints at these periphery/corner areas. With an embodiment of the present invention, at least part of the stresses on the solder ball/bump 18 joints are taken up or transferred to by the joints between the reinforcement frame corners 54a and the PCB 14. As a result, the stresses experienced by the solder ball/bump 18 joints are lower, thus, leading to higher solder interconnect reliability when a reinforcement frame of an embodiment of the present invention is attached to a semiconductor package.

[0028] The rigidity provided by the reinforcement frame 50 also lends localised rigidity to the PCB 14 at the semiconductor package 10 footprint area. As a result, localized bending and flexing of the PCB 14 under shock or drop impact is reduced. Thus, the stresses experienced by the solder ball/bump 18 joints, especially those at corners of the semiconductor package 10 are less severe. With the additional advantage of stronger joints between the reinforcement frame 50 and the PCB 14, the solder ball/bump 18 joints between the semiconductor package 10 and the PCB 14 experience lower stresses both under shock impact and thermal cycling. As a result, the reinforcement frame 50 according to an embodiment of the present invention improves the solder joint reliability of an integrated circuit package mounted on a PCB or circuit substrate.

[0029] FIG. 4 illustrates another embodiment of the reinforcement frame 150. FIG. 4 shows a bottom view of the reinforcement frame 150. As shown in FIG. 4, the reinforcement frame 150 has four PCB attachment areas 154a linked by four radial linking members 160 to a central member 170. The PCB attachment areas 154a, as in the previous

embodiment 50, has a full-height thickness, whilst the linking and central members 160, 170 have a reduced height. In a variation, the central member 170 is optional.

[0030] FIG. 5 illustrates the use of the reinforcement frame 50, 150 with a cavity-down ball grid array packaging instead of cavity-up BGA embodiments described earlier.

[0031] FIG. 6 illustrates a reinforcement frame 200 according to another embodiment of the present invention. As shown in FIG. 6, the reinforcement frame 200 has dimensions larger than the outline dimensions of the semiconductor package 10. This embodiment of the reinforcement frame 200 allows additional peripheral rows and columns of solder balls 218 to be provided. These additional rows and columns of solder balls 218 may be dummies, which provide extra mechanical strength to the solder ball/bump 18 joints between the semiconductor package 10 and the PCB 14. In another embodiment, the additional rows and columns of solder balls 218 are disposed at the extreme peripheral corners around active solder joints, i.e. those solder joints that actively conduct electrical signals. The stresses taken up by the dummy solder balls 218 help to reduce the stresses experienced by the active solder balls 18; in this way, the use of the reinforcement frame 200 according to an embodiment of the present invention on a semiconductor package increases the reliability of the solder joints formed between the semiconductor package 10 and the PCB 14. Further, the additional rows and columns of solder balls 218 increases the interconnect density of a semiconductor package 10 thereby providing more functions to a semiconductor package 10 of a given package size.

[0032] In addition, if the reinforcement frame 50, 150, 200 is made of metal, the reinforcement frame 50, 150, 200 can be advantageously used as a heat sink. FIG. 7 shows a cross-section of an integrated circuit package 300. As in the embodiments of the semiconductor packages described earlier, the semiconductor package 300 comprises a moulded compound layer 313 and a substrate 312 layer. As shown in FIG. 7, thermal traces 320 connect the IC wafer die 310 to a peripheral and lower surface of the substrate layer 313. In use, the thermal traces 320 directly conduct heat generated during operation

of the IC die 310 to the reinforcement frame 50, 150, 200 for dissipation, for example, to the ambience. In an embodiment of the present invention, the reinforcement attachment areas on the PCB 314 may be provided with conductor vias 330 in the PCB 314. These conductor vias 330 and PCB 314 provide an additional channel to conduct heat away from the reinforcement frame 50, 150, 200 to ground planes 340 in the PCB 314. This embodiment 300 is advantageous where it is not possible to dedicate a central portion of the solder interconnect pattern to serve as thermal interconnects to conduct heat from the semiconductor package 300 to the PCB 314. In addition, the semiconductor package 300 according to this embodiment doing away with thermal interconnects provide a higher interconnect density; accordingly a semiconductor package 300 with higher interconnect density would also provide a semiconductor package with extra functions.

[0033] While specific embodiments have been described and illustrated, it is understood that many changes, modifications, variations and combinations thereof could be made to the present invention without departing from the scope of the invention. For example, whilst a quadrilateral reinforcement frame is described, the reinforcement frame is not restricted by its outline shape; for instance, it can have a polygonal or round outline. Further, the reinforcement frame attachment area 54a, 154a need not be restricted to a peripheral or corner of the reinforcement frame; for instance, intermediate or interior attachment areas may be provided instead of or in addition to those at the periphery or corners. Furthermore, the attachment area 54a, 154a need not be square or rectangular as shown in the figures; for instance, they may be oval or L-shaped in area.

CLAIMS:

1. A semiconductor package comprising:

a reinforcement frame operable for attachment to a peripheral area around an interconnect pattern of the semiconductor package.

2. A semiconductor package according to claim 1, wherein the reinforcement frame comprises a planar surface interface with the semiconductor package.

3. A semiconductor package according to claim 2, wherein the reinforcement frame comprises a step-height surface substantially parallel to the planar surface.

4. A semiconductor package according to claim 3, wherein the reinforcement frame forms a polygonal outline and the height of the reinforcement frame around each corner of the polygonal outline has a full height.

5. A semiconductor package according to claim 4, wherein the corners of the reinforcement frame are discrete and the discrete corners are joined to each other by linking members disposed to form a polygonal ring.

6. A semiconductor package according to claim 4, wherein the corners of the reinforcement frame are discrete and the discrete corners are joined to each other by radial linking members.

7. A semiconductor package according to claim 5 or 6, wherein the height of each linking member is substantially half the full height of the reinforcement frame at each corner.

8. A semiconductor package according to any one of the preceding claims, wherein the reinforcement frame is operable for mounting onto the semiconductor package by means of adhesive.

9. A semiconductor package according to any one of the preceding claims, wherein the reinforcement frame is selected from the following material: metal, glass or ceramic.

10. A semiconductor package according to claim 9, wherein the semiconductor package further comprising one or more thermal traces connecting a semiconductor die to the reinforcement frame.

11. A semiconductor package according to any one of claims 4-10, wherein each corner of the polygonal reinforcement ring is operable for attachment to an attachment area on a printed circuit board or substrate.

12. A semiconductor package according to claim 11, further comprising PCB/substrate attachment area disposed on one or more linking members.

13. A semiconductor package according to claim 11 or 12, wherein the attachment area of the printed circuit board or substrate comprises one or more thermal conductive vias.

14. A method of improving the solder joint reliability of a semiconductor package mountable on a printed circuit board (PCB) or circuit substrate, the method comprising:

mounting the semiconductor package on a reinforcement frame; and

wherein the reinforcement frame is mountable on a PCB/circuit substrate.

15. A method according to claim 14, wherein the reinforcement frame is mounted to the semiconductor package on a peripheral area around an interconnect pattern of the semiconductor package.

16. A method according to claim 14 or 15, wherein said mounting comprises adhesive curing and wherein said reinforcement frame is mountable on the PCB/circuit substrate by adhesive curing.

17. A method according to claim 14 or 15, wherein said mounting between the semiconductor package and the reinforcement frame comprises adhesive curing, while mounting between the reinforcement frame and the PCB/circuit substrate comprises reflowing of solder in an oven.

18. A method according to claim 14 or 15, wherein said mountings are carried out in a one-step or two-steps process.

19. A method according to any one of claims 14-18, further comprising both aligning interconnects of the semiconductor package with the corresponding solder pads on the PCB/substrate and aligning attachment areas of the reinforcement frame with respective attachment areas on the PCB/circuit substrate prior to curing of the adhesive or reflowing of solder.

20. A method according to claim 19, wherein the reinforcement frame attachment areas are selected furthest from the neutral axis orthogonal to the surface of the semiconductor package mountable to the PCB/substrate assembly.

21. A method according to claim 20, wherein one or more additional reinforcement frame attachment area(s) is/are selected intermediate to the reinforcement frame attachment areas.

22. A method according to any one of claims 14-21, wherein the semiconductor package further comprises one or more thermal traces connecting a semiconductor die to the reinforcement frame.

23. A method according to any one of claims 14-22, wherein the reinforcement frame is manufactured according to any one of device claims 1-13.

24. A method according to any one of claims 14-23, further comprising: mounting the reinforcement frame on the PCB/circuit substrate.