

"AMPLITUDE MODULATOR CIRCUIT FOR MODULATING A VIDEO SIGNAL ON A CARRIER SIGNAL"

The invention relates to an amplitude modulator circuit for modulating a video signal having periodically occurring reference signal portions on a carrier signal, comprising a modulator having a carrier input terminal for receiving the carrier signal, a modulation
 5 input terminal for receiving the video signal and an output terminal for supplying the resulting amplitude-modulated signal, a control loop coupled to the said output terminal and including a sampling circuit which is active for sampling during reference signal intervals, said control loop generating a direct current compensation signal for
 10 addition to the video signal.

Such a modulator circuit must be of such a construction that the amplitude-modulated signal at the output terminal does not contain a carrier signal in the time intervals in which the video signal has a reference value. To this end the video signal is usually brought to
 15 a fixed level, for example by means of a clamping circuit, this level corresponding to an output signal which does not contain a carrier. Such a technique is used in colour encoding circuits for the NTSC or the PAL standards. The amplitude of the colour sub-carrier must then be zero during the reference signal intervals.

20 In practice a carrier signal may however occur at the output terminal of the modulator during these intervals, which is, for example, caused by an asymmetry in the modulator, a direct current offset in the clamping circuit or variations caused by fluctuations in the supply voltage and/or the temperature. In encoding circuits such an unbalance
 25 of the output signal is known as "sub-carrier leakage". This leakage can be eliminated for the greater part by designing the modulator circuit such that a relatively large modulating signal is used to drive the modulator as a result of which the fault is comparatively small. However, this requires a large power. Another possibility is an accurate
 30 adjustment of various portions of the circuit but such an adjustment

is time-consuming, while the result thereof may again be susceptible to an unwanted variation with time.

Swiss Patent Specification 282,896 discloses a circuit in which a control loop produces a direct current compensation signal as a result of which signal portions can be brought to a predetermined level. This level must, however, be adjusted and may vary with time.

The invention has for its object to provide a circuit of the above-mentioned type in which the sub-carrier leakage is automatically reduced to a large extent.

The invention provides an amplitude modulator circuit of the type described in the opening paragraph which is characterised in that the signal at the said modulation input terminal has a value such that the said resulting amplitude modulated signal at the said output terminal is substantially independent of the signal at the said carrier input terminal during those periods when the sampling circuit is active, and that the amplitude modulator circuit further comprises an adder stage connected to the said output terminal and a second control loop may be provided which includes a second sampling circuit which is active for sampling during reference signal intervals, said second control loop generating a second direct current compensation signal for addition to the signal at the said output terminal of the modulator, the first mentioned control loop being coupled to the output terminal of the modulator via the adder stage.

The first control loop may comprise a comparison stage a first input terminal of which carries a reference signal, which comparison stage has a second input terminal and an output terminal included in the first control loop, this reference signal having a value which is substantially equal to that value of the signal at the output terminal of the modulator which is substantially independent of the signal at the carrier input terminal of the modulator. The signal at the said carrier input terminal may have, at least during those periods when the first sampling circuit is active a direct current level of such a polarity that the control loop causes negative feedback.

With the above circuit the first and second circuits may not be active simultaneously. The signal at the carrier input terminal may

have at least during those periods when the second sampling circuit is active a second direct current level of such a polarity that the second control loop also causes negative feedback, the second direct current level deviating from the first direct current level.

5 The second input terminal of the comparison stage may be coupled to the output terminal of the adder stage while the output terminal of the comparison stage may be connected to the first and second sampling circuits. Such sampling circuits may be sample and hold circuits. The circuit may further comprise a second adder stage for
10 adding a pulse-shaped measuring signal to the carrier signal during the period of time in which the first sampling circuit is active, or a change-over switch for applying a direct current level to the said carrier input terminal during those periods when the first sampling circuit is active and for applying the carrier signal to the said
15 input terminal during the period of time in which the first sampling circuit is not active.

 The invention also provides an arrangement of the above circuit in combination with a second amplitude modulator circuit for modulating a second video signal having periodically occurring reference signal
20 portions on a second carrier signal, the second amplitude modulator circuit comprising a second modulator having a second carrier input terminal for receiving the second carrier signal, a second modulation input terminal for receiving the second video signal and a second output terminal for supplying the resulting second amplitude-modulated
25 signal, the arrangement further comprising a further adder stage for adding together the said first and second amplitude-modulated signals, the second amplitude modulator circuit further comprising a further control loop which is coupled to the second output terminal and includes a further sampling circuit which is active for sampling during
30 reference signal intervals, said third control loop generating a further direct current compensation signal for addition to the second video signal, the signal at the second modulation input terminal having a value such that the said resulting amplitude modulated signal at the second output terminal is substantially independent of the signal at
35 the second carrier input terminal during those periods when the further sampling circuit is active. Such an arrangement may further comprise an adder stage connected to the second output terminal and an additional

control loop including an additional sampling circuit which is active for sampling during reference signal intervals, said additional control loop generating an additional direct current compensation signal for addition to the signal at the second output terminal, the said further and additional sampling circuits not being simultaneously active whilst the further control loop is connected to the output terminal of the last mentioned adder stage. The further sampling circuit may be connected to the comparison stage and the second and the further sampling circuits are not simultaneously active.

The sampling circuits may be active during a line blanking interval of the video signal outside the occurrence of the burst of the colour synchronising signal and in addition may be active line-sequentially. A frequency divider circuit may be used for dividing the repetition frequencies of applied pulses of line frequency and for generating line-sequential pulses.

When the circuit forms part of a colour encoding circuit the carrier signal may be a colour sub-carrier signal when the video signal would be a colour difference signal.

Where a circuit or an arrangement is used for modulating a (R-Y) colour difference signal in a colour encoding circuit for the PAL standard a generator may be provided for generating a square-wave switching signal of half the line frequency, whilst adder stage may be provided for adding together every sixth line period the pulse which operates the sampling circuit in the first control loop for the (R-Y) modulator and a switching signal of half the line frequency.

The invention will now be further explained by way of non-limitative examples with reference to the accompanying drawings in which:-

Figure 1 shows an amplitude-modulation circuit,

Figure 2 shows wave forms occurring therein,

Figure 3 shows an embodiment of a circuit according to the invention,

Figure 4 shows an embodiment of a colour encoding arrangement embodying circuits according to the invention,

Figure 5 shows a second, more detailed, and preferred embodiment of a colour encoding arrangement, and

5 Figure 6 shows waveforms occurring therein.

In Figure 1 reference numeral 1 denotes an amplitude modulator in a colour encoding circuit having two input terminals 2 and 3 and an output terminal 4. Input terminal 2 is connected to the output terminal of an adder stage 5. A colour sub-carrier signal Sc
10 having a frequency of for example 3.579545 MHz (NTSC standard) or 4.43361875 MHz (PAL standard) is applied to an input terminal 6 of adder stage 5, while a measuring pulse P, which is generated by a pulse generator 8 is applied to another input terminal 7 of adder stage 5.

15 Input terminal 3 is connected to the output terminal of a further adder stage 9. A video signal, for example a colour difference signal D is applied to an input terminal 10 of adder stage 9, while a compensation voltage v is present across a further input terminal 11 thereof. Via an isolating resistor 12, the amplitude-
20 modulated signal present at output terminal 4 is applied to a parallel circuit 13, which is tuned to the frequency of the colour sub-carrier and the amplitude-modulated signal is thereafter processed in known manner.

Terminal 4 is also connected to the inverting input terminal
25 of a comparison stage 14. The non-inverting input terminal thereof is connected to ground, while the output terminal is connected to a sample and hold circuit including a switch 15 and a capacitor 16. Switch 15 is periodically operated by the pulse P coming from generator 8 and the compensation voltage v is present across capacitor 16
30 for application to terminal 11. It will be clear that elements 14 and 15, as they are arranged in cascade, may be interchanged.

During operation, the colour sub-carrier signal Sc which is applied to terminal 6 has a constant amplitude (Figure 2a). The

colour difference signal D applied to terminal 3 varies with time in the manner shown in Figure 2b, γ indicating the line blanking period in this Figure. During this reference period the signal of Figure 2b has constant value V except for the period of time in which the burst of the colour synchronising signal occurs, the signal of Figure 2b containing in that period of time a pulse which is the envelope of the burst. Prior to and after γ time the said signal is subjected to a variation which depends on the content of the recorded picture. This variation is of little importance to the invention and is therefore shown partly only in Figure 2b.

Without the measure described and with an ideal modulator, value V must be equal to the value for which the amplitude of the amplitude-modulated signal at terminal 4 has zero value. In practice, however, an unbalance in the circuit causes the above-mentioned sub-carrier leakage, that is to say the said amplitude is not zero and may furthermore vary with time.

A measuring pulse P, which occurs in time γ prior to the burst and which has a duration of some μ s (Figure 2c) is applied to terminal 7. The output signal of stage 5 is of the shape shown in Figure 2d. If the control loop which includes elements 14, 15 and 16 were not in operation, the waveform shown in Figure 2e would be found at terminal 4. This waveform is obtained by multiplying the waveforms of Figures 2b and 2d. From this it is apparent that the signal obtained is a modulated sine wave having the frequency of the sub-carrier and that, consequently, the mean value thereof is zero, except during the occurrence of pulse P where the said mean value is equal to the product of the value V and the mean value of sine wave which, in Figure 2b, is superimposed on the pulse. From Figure 2e it is furthermore apparent that the amplitude of the amplitude-modulated signal is not equal to zero during time γ prior to and after the burst.

By means of the comparator stage 14 the signal at terminal 4 is compared with the reference value, in this example zero, at the non-inverting terminal and each value of the signal of Figure 2e not equal to zero is amplified and inverted. Figure 2f shows the shape of the signal obtained at the output terminal of stage 14. As

switch 15 is closed by the measuring pulse, a voltage v equal to the mean value of the signal shown in Figure 2f, is produced across capacitor 16 during the occurrence of the pulse. Until the next sampling interval voltage v remains substantially constant and is added to the signal D.

The unbalance which causes the sub-carrier leakage may be considered to be an offset in the direct current component of the modulating signal at the modulation input terminal of an ideal modulator. When this offset is positive and the measuring pulse has been chosen to be positive, as is the case in Figure 2c, then the offset obtained in Figure 2e during the occurrence of the pulse is also positive. The offset shown in Figure 2f and, consequently, also voltage v are then negative. Voltage v is subtracted from the offset at terminal 3 causing the amplitude of the colour sub-carrier signal in the signal at terminal 4 to become smaller during the occurrence of pulse P, while voltage v becomes less negative. After a number of cycles of pulse P, depending on the time constant of the sample and hold circuit, the control loop so adjusts itself that, during the occurrence of pulse P, the signal at terminal 4 assumes essentially the value of the reference voltage i.e. zero in this example, at the non-inverting terminal of comparator stage 14 and that the resulting offset at terminal 3 is zero. This implies that the signals at terminals 10 and 11 have the same absolute value and are of opposite sign during the occurrence of the measuring pulse and that the amplitude of the colour sub-carrier signal at terminal 4 is substantially zero during the same period of time. As the described situation occurs for a certain value of the signal of Figure 2b, the amplitude at terminal 4 is also substantially zero, each time the signal of Figure 2b assumes this specific value. This holds in particular during the time τ prior to and after the measuring pulse and prior to and after the colour burst, as well as in time intervals, not shown, in which the colour difference signal does not contain colour information.

In these circumstances the signal at terminal 4 is of the shape shown in Figure 2g and is substantially free from sub-carrier leakage. This signal may yet show an asymmetry, the positive and the negative

portions of the waveform then being unequal. This fault is eliminated in known manner by means of circuit 13.

When now the offset at terminal 3 is negative, while the measuring pulse is still positive, then the offset obtained in Figure 2e
5 during the occurrence of the pulse is still negative, so that the voltage v is positive. So the resultant offset at terminal 3 becomes less negative and the control achieves the same result as described in the foregoing. From this it will be apparent that the d.c. offset added to the carrier signal by means of the measuring pulse must be
10 positive in the case of the control loop shown. The inverting action of stage 14 must particularly be taken into consideration. The polarity of the offset applied to terminal 7 must be chosen so that the action of the control results in a negative feedback to terminal 11, while the value of the applied offset must be sufficiently large to
15 achieve that the fault to be corrected has little influence, but it must not be so large that it prevents the modulator from operating properly.

As mentioned above, the offset must be added to the sub-carrier signal and not to the colour difference signal. Thus if the offset
20 were added to the colour difference signal it would produce a symmetrical sine wave after modulation and if the pulse duration of the measuring pulse were not equal to an integral number of periods of the sine function, then an error would be introduced which might be very considerable. When the offset is added to the sub-carrier
25 signal a similar error is introduced which is, however, much smaller provided the pulse has a sufficiently large amplitude and provided the loop gain is large enough. It will also be noted that the sub-carrier signal present at terminal 6 during the occurrence of the pulse has no function in the control. Adder stage 5 may therefore
30 be replaced by a change-over switch which is operated by the pulse and by means of which terminal 2 is supplied with either the sub-carrier signal, or, more specifically during the occurrence of the pulse, with a direct current signal, as a result of which the above-mentioned error, that is to say the minor error introduced by the sub-carrier
35 present during the occurrence of the pulse, is completely eliminated.

In the case of Figure 1 and also in the case just described, it is not necessary for the measuring pulse to have the line frequency: the repetition frequency thereof may be lower. The only requirement the circuit must satisfy is that the charge of capacitor 16 is retained between two sampling intervals, which can be improved by including an isolating stage in the connection between capacitor 16 and terminal 11. It will be clear that the direct current offset applied to terminal 7 need not be square wave pulse-shaped. When, namely, such an offset is present during the entire line period the amplitude of terminal 4 is made equal to zero during the occurrence of the pulse, due to the action of sample and hold circuit 15, 16. A signal of video frequency is then indeed generated at terminal 4 but it can be eliminated in a simple manner by means of frequency-selective means, for example by means of circuit 13.

In the foregoing it was mentioned that the value of the reference voltage at the non-inverting terminal of comparison stage 14 is zero. From this it follows that the voltage at terminal 4 is substantially zero at the occurrence of the pulse which closes switch 15. However, this is only applicable when modulator 1 is of such a construction that the output voltage terminal is zero when the modulating signal has the value at which the output signal is independent of the value of the signal at the sub-carrier input terminal. When the modulator is of such a construction that, in the absence of a control, the output voltage of the modulator does not have zero value when the modulating signal has the above-mentioned value, then the reference voltage must be given a value which is somewhat higher than the value of the output voltage in the above-mentioned circumstances. This also determines the direct current level at terminal 4.

As the direct current offset at terminal 3 has automatically become almost zero because of the action of the circuit shown in Figure 1, a clamping circuit for fixing the direct current level of the colour difference signal is not required. It may, however, happen that modulator 1 has a variable direct current unbalance at output terminal 4, while the control loop owing to the non-infinite gain thereof introduces a slight direct current error. A direct current

error may alternatively be caused by one or more amplifiers, not shown in Figure 1. For these reasons the reference voltage at the non-inverting terminal of comparison stage 14 should be variable or at least adjustable. For the circuit shown in Figure 3 a constant reference voltage can be used which is furthermore independent of the properties of the modulator. Components in Figure 3 which correspond to those of Figure 1 have been given the same reference numerals.

In Figure 3, terminal 4 is connected to an input terminal 18 of an adder stage 17. The output terminal thereof is connected to the input terminal 20 of a non-inverting amplifier 19, whose output terminal 21 is connected to resistor 12 and to the inverting input terminal of comparison stage 14. The output terminal of stage 14 is connected to sample and hold circuit 15, 16 and to a further sample and hold circuit having a switch 22 and a capacitor 23, which is connected to a second input terminal 24 of adder stage 17. Switch 22 is periodically operated by a pulse P_1 generated by pulse generator 8, while switch 15 is also periodically operated by a pulse P_2 generated by generator 8, this pulse P_2 also being applied to terminal 7. Pulses P_1 and P_2 occur during reference intervals which occur in the same manner as pulse P in Figure 2c, but they must not coincide.

When in the output circuit of modulator 1 a direct current offset occurs, then, in the absence of the control loop which comprises elements 14, 22 and 23, a direct voltage level would be superimposed on the signals at terminal 21 shown in Figure 2g. The operation of this loop produces across capacitor 23 a voltage v' which has a polarity which is the opposite of the polarity of this voltage level and after a number of periods of pulse P_1 the loop adjusts itself such that the d.c. voltage level at terminal 21 has substantially the same value as the reference voltage, zero in this example, at the non-inverting terminal of comparator stage 14. In this manner a d.c. voltage level at terminal 21 is kept at a constant, predetermined value. This value may be determined by the d.c. voltage level of the further stages, not shown in Figure 3, which are connected to resistor 12 and to circuit 13.

The control loop, comprising elements 14, 15 and 16 operates in Figure 3 in the same manner as the corresponding control loop in Figure 1. In the equilibrium condition of the loop the signal at terminal 4 during the occurrence of pulse P_2 is independent of the sub-carrier signal at terminal 6 and of the value of the reference voltage at the non-inverting terminal of stage 14. When the signal at terminal 4 varies for some reason or another, then this variation is processed thus by the control loop comprising elements 14, 22 and 23 such that the output signal at terminal 21 is not influenced by it. A signal which is amplified and inverted with respect to the signal at terminal 21 is obtained from the output terminal of comparator stage 14. During the occurrence of pulse P_1 the voltage v' of capacitor 23 is available at this output terminal and during the occurrence of pulse P_2 the voltage v of capacitor 16 is available at the output terminal. Voltage v' depends on the reference voltage but voltage v does not. These voltages are therefore unequal. If the reference voltage is given a value other than zero, then voltage v' and the d.c. voltage level at terminal 21 assume another value, while voltage v and the signal at terminal 4 are not changed. For simplicity, the two loop gains are assumed to be infinitely large.

Pulses P_1 and P_2 can be generated line-sequentially, that is to say that during a line blanking period pulse P_1 is applied to switch 22 and that pulse P_2 is applied to switch 15 during the next following line blanking period. As was the case in Figure 1, a lower repetition frequency may, however, be opted for. At the same manner as in Figure 1, a direct current offset is introduced in the signal applied to terminal 2, at least during the occurrence of pulse P_2 but not during the occurrence of pulse P_1 . For the described circuit this deviation must be positive in order to obtain a negative feedback. It will be clear that the same result may be obtained when a negative direct current offset is introduced, at least during the occurrence of pulse P_1 but not during the occurrence of pulse P_2 .

Figure 4 shows a circuit for a NTSC- or PAL-encoding circuit, in which consequently two colour difference signals are processed. In Figure 4, the portion comprising elements 1 to 7 inclusive, 9 to 11

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inclusive and 14 to 24, inclusive, corresponds to the circuit shown in Figure 3 and this portion is used to modulate the colour sub-carrier wave with the colour difference signal D, i.e., for example, the (B-Y) signal for the PAL standard or the I-signal for the NTSC standard.

5 A circuit portion comprising elements 1' to 7' inclusive, 9' to 11' inclusive and 14' to 24' inclusive, and having the same construction as the first-mentioned portion, is used for modulation with the other colour difference signal D', which here refers to modulation with the Q-signal of the NTSC standard. For the (R-Y) signal of the PAL
10 standard measures must be taken to ensure the prescribed line-sequential inversion thereof, which is realised by means of a pulse $\frac{H}{2}$ of half the line frequency, which is applied to modulator 1'. This is shown in Figure 4 by means of a broken line.

The output terminal 21 of the (B-Y) or the I-portion, respectively,
15 of the circuit shown in Figure 4 is connected to an input terminal of an adder stage 25. The output terminal 21' of the (R-Y) or Q-portion, respectively, is connected to another input terminal thereof. Elements 12 and 13 have further been provided at the output terminal of stage 25 and the total modulated output signal is available at
20 the junction of these elements. For this purpose 90° phase shifted colour sub-carrier signals Sc and Sc' are applied to terminals 6 and 6', while pulses P_1 and P_2 , which are similar to those in Figure 3 are operative therein in the same way.

The circuit of Figure 4 has the drawback that two amplifiers 19
25 and 19' and two comparator stages 14 and 14', respectively, which in practice may have different properties, are required and which may introduce errors. The circuit of Figure 5 does not have this drawback as the two portions thereof have the control loop fixing the direct current level at the output terminal of the circuit in common.
30 Elements in Figure 5 which correspond to those in Figure 4 have been given the same reference numerals.

Modulators 1 and 1' are constructed symmetrically in Figure 5. The non-inverting output terminal 4_1 and $4'_1$ of modulator 1 and 1', respectively, is connected to a non-inverting input terminal of
35 amplifier 19 via a resistor 26_1 and $26'_1$, respectively, while the

inverting output terminal 4_2 and $4'_2$, respectively, of modulator 1 and $1'$, respectively, is connected to an inverting input terminal of amplifier 19 via a resistor 26_2 and $26'_2$, respectively. Capacitor 23 is connected to the non-inverting input terminal of amplifier 19
 5 via a non-inverting buffer amplifier 27 and a resistor 28. An isolating resistor 29 is provided between comparator stage 14 and switch 22. Switches 15 and $15'$ are both connected to the junction of switch 22 and resistor 29. A buffer amplifier 30 and $30'$, respectively, is included in the lead between capacitor 16 and $16'$, respectively, and
 10 terminal 11 and $11'$, respectively. Resistor 29 is used in conjunction with further resistances, for example the output resistance of stage 14, and in conjunction with capacitor 23, 16 or $16'$ to determine the time constant of the three sample and hold circuits. In all other respects the circuit shown in Figure 5 is the same to that of Figure 4.

15 The control loop comprising elements 14, 22 and 23 operate in the same way as the corresponding loop of Figure 3. For this purpose switch 22 is operated by the same pulse P_1 as in Figure 3. The output signals of modulators 1 and $1'$ and also the compensation voltage produced across capacitor 23 are added together by means of resistors
 20 26_1 , $26'_1$, 26_2 , $26'_2$ and 28. In the same way as in Figure 3 the d.c. voltage level of the modulated signal is fixed at the output terminal of amplifier 19, and that at substantially the value, zero in this example, of the reference voltage at the non-inverting terminal of comparator stage 14.

25 Switch 15 is operated by a pulse P_2 , which is also applied to terminal 7 and which occurs one line period later than pulse P_1 . The control loop comprising elements 14, 15 and 16 eliminates in the manner explained hereinbefore the sub-carrier leakage of modulator 1. In a similar manner switch $15'$ is operated by a pulse P'_2 , which is also
 30 applied to terminal $7'$ and which occurs one line period later than in pulse P_2 . The control loop comprising elements 14, $15'$ and $16'$ eliminates the sub-carrier leakage of modulator $1'$.

Pulse generator 8 comprises a frequency divider circuit which is
 35 supplied with pulses H of line frequency and which divides the repetition frequency thereof by three, causing the pulse trains P_1 , P_2 and P'_2

to be generated line-sequentially (see Figure 6 in which time τ has been shown once). Generator 3 also generates a signal $\frac{H}{2}$ of half the line frequency for the (R-Y) change-over for the PAL standard, this signal not being utilized when the NTSC standard is used. As
5 the repetition frequency of pulse P'_2 is equal to one third the line frequency, signal $\frac{H}{2}$ must have the shape shown in Figure 6. Pulse P'_2 is added to the original squarewave switching signal at half the line frequency every 6 lines. For simplicity, Figure 5 does not show the adder stage which is then required. No (R-Y) inversion is thus
10 effected for the offset applied to terminal 2', which would cause the control operating by means of elements 14, 15' and 16' to cause positive feedback. It will be obvious that the same applies for the signal $\frac{H}{2}$ in Figure 4. Alternatives are possible, for example the operation of amplifier 30' may be reversed every six line periods.
15 Finally, it should be noted that all the described portions of the modulator circuit, the capacitors and circuit 13 excepted, can be advantageously integrated in a semiconductor body.



CLAIMS:-

1. An amplitude modulator circuit for modulating a video signal having periodically occurring reference signal portions on a carrier signal, comprising a modulator having a carrier input terminal for receiving the carrier signal, a modulation input terminal for receiving the video signal and an output terminal for supplying the resulting amplitude modulated signal, a control loop coupled to the said output terminal and including a sampling circuit which is active for sampling during reference signal intervals, said control loop generating a direct current compensation signal for addition to the video signal, characterised in that the signal at said modulation input terminal has a value such that the said resulting amplitude modulated signal at the said output terminal is substantially independent of the signal at the said carrier input terminal during those periods when the sampling circuit is active, and that the amplitude modulator circuit further comprises an adder stage connected to the said output terminal and a second control loop which includes a second sampling circuit which is active for sampling during reference signal intervals, said second control loop generating a second direct current compensation signal for addition to the signal at the said output terminal, the first mentioned control loop being coupled to the output terminal of the modulator via the said adder stage.

2. A circuit as claimed in Claim 1, characterised in that the first control loop also comprises a comparison stage a first input terminal of which carries a reference signal, which comparison stage has a second input terminal and an output terminal included in the first control loop, this reference signal having a value which is substantially equal to that value of the signal at the output terminal of the modulator which is substantially independent of the signal at the carrier input terminal of the modulator.



3. A circuit as claimed in Claim 1 or 2, characterised in that the signal at the said carrier input terminal has at least during those periods when the first sampling circuit is active, a direct current level of such a polarity that the first control loop causes negative feedback.

4. A circuit as claimed in Claim 1, 2 or 3, characterised in that the said first and second sampling circuits are not active simultaneously.

5. A circuit as claimed in Claim 3 or 4, characterised in that the signal at the carrier input terminal has at least during those periods when the second sampling circuit is active a second direct current level of such a polarity that the second control loop also causes negative feedback, the second direct current level deviating from the first direct current level.

6. A circuit as claimed in Claim 2, characterised in that the second input terminal of the comparison stage is coupled to the output terminal of the adder stage, while the output terminal of the comparison stage is connected to the first and second sampling circuits.

7. A circuit as claimed in any of the preceding Claims, characterised in that the first and second sampling circuits are sample and hold circuits.

8. A circuit as claimed in Claim 7, characterised in that it comprises a second adder stage for adding a pulse-shaped measuring signal to the carrier signal during the period of time in which the first mentioned sampling circuit is active.

9. A circuit as claimed in Claim 7, characterised in that it comprises a change-over switch for applying a direct current level to the said carrier input terminal during those periods when the first mentioned sampling circuit is active and for applying the carrier signal to the said carrier input terminal during the periods when the first sampling circuit is not active.

10. An arrangement comprising a circuit as claimed in any of the preceding Claims in combination with a second amplitude modulator circuit for modulating a second video signal having periodically occurring reference signal portions on a second carrier signal, said second amplitude modulator circuit comprising a second modulator having



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a second carrier input terminal for receiving the second carrier signal, a second modulation input terminal for receiving the second video signal and a second output terminal for supplying the resulting second amplitude modulated signal, said arrangement further comprising
5 a further adder stage for adding together the said first and second amplitude-modulated signals, characterised in that the second amplitude modulator circuit further comprises a further control loop which is coupled to the second output terminal and includes a further sampling circuit which is active for sampling during reference signal intervals,
10 said further control loop generating a further direct current compensation signal for addition to the second video signal, the signal at the second modulation input terminal having a value such that the said resulting amplitude modulated signal at the second output terminal is substantially independent of the signal at the second carrier
15 input terminal during those periods when the further sampling circuit is active.

11. An arrangement as claimed in Claim 10, characterised in that it comprises an adder stage connected to the second output terminal and an additional control loop including an additional sampling circuit
20 which is active for sampling during reference signal intervals, said additional control loop generating an additional direct current compensation signal for addition to the signal at the second output terminal, the said further and additional sampling circuits not being simultaneously active whilst the further control loop is
25 connected to the output terminal of the last mentioned adder stage.

12. An arrangement as claimed in Claim 10, characterised in that the further sampling circuit is connected to the comparison stage and that the second and the further sampling circuits are not simultaneously active.

30 13. A circuit or an arrangement as claimed in any of the preceding claims, characterised in that the sampling circuits are active during a line blanking interval of the video signal outside the occurrence of the burst of the colour synchronising signal.

35 14. A circuit or an arrangement as claimed in Claim 4, 12 or 13, characterised in that the sampling circuits are active line-sequentially.



15. A circuit or an arrangement as claimed in Claim 14, characterised in that it further comprises a frequency divider circuit for dividing the repetition frequency of applied pulses of line frequency and for generating line-sequential pulses.

5 16. A circuit or an arrangement as claimed in one of the preceding claims, characterised in that the carrier signal is a colour sub-carrier signal while the video signal is a colour difference signal.

10 17. A circuit or an arrangement as claimed in Claim 16 for modulating an (R-Y) colour difference signal in a colour encoding circuit for PAL standard, comprising a generator for generating a square-wave switching signal of half the line frequency, characterised in that it further comprises an adder stage for adding together every sixth line period the pulse which operates the sampling circuit in
15 the first control loop for the (R-Y) modulator and a switching signal of half the line frequency.

18. An amplitude modulator circuit substantially as herein described with reference to the accompanying drawings.

20 19. An arrangement of amplitude modulator circuits substantially as herein described with reference to Figures 4 or 5 of the accompanying drawings.

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