

FIG. 1

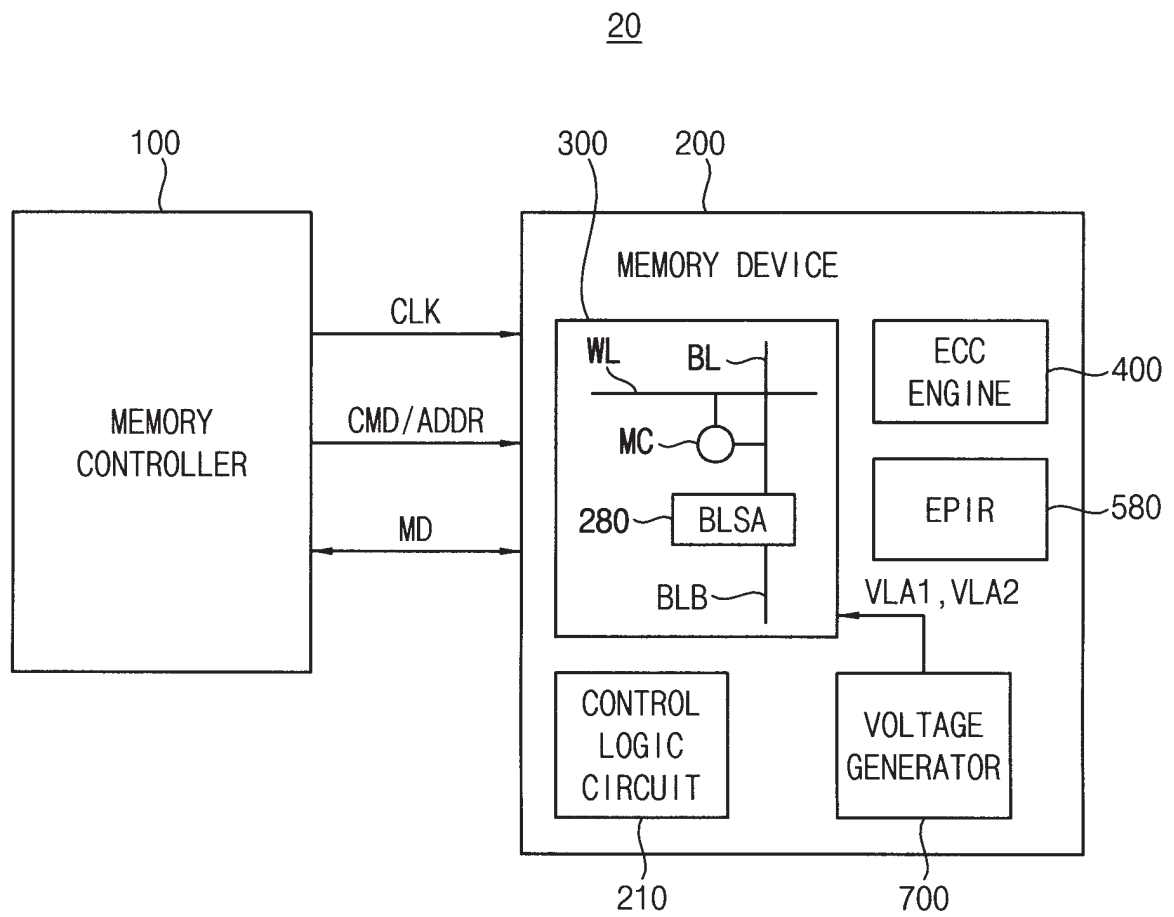


FIG. 2

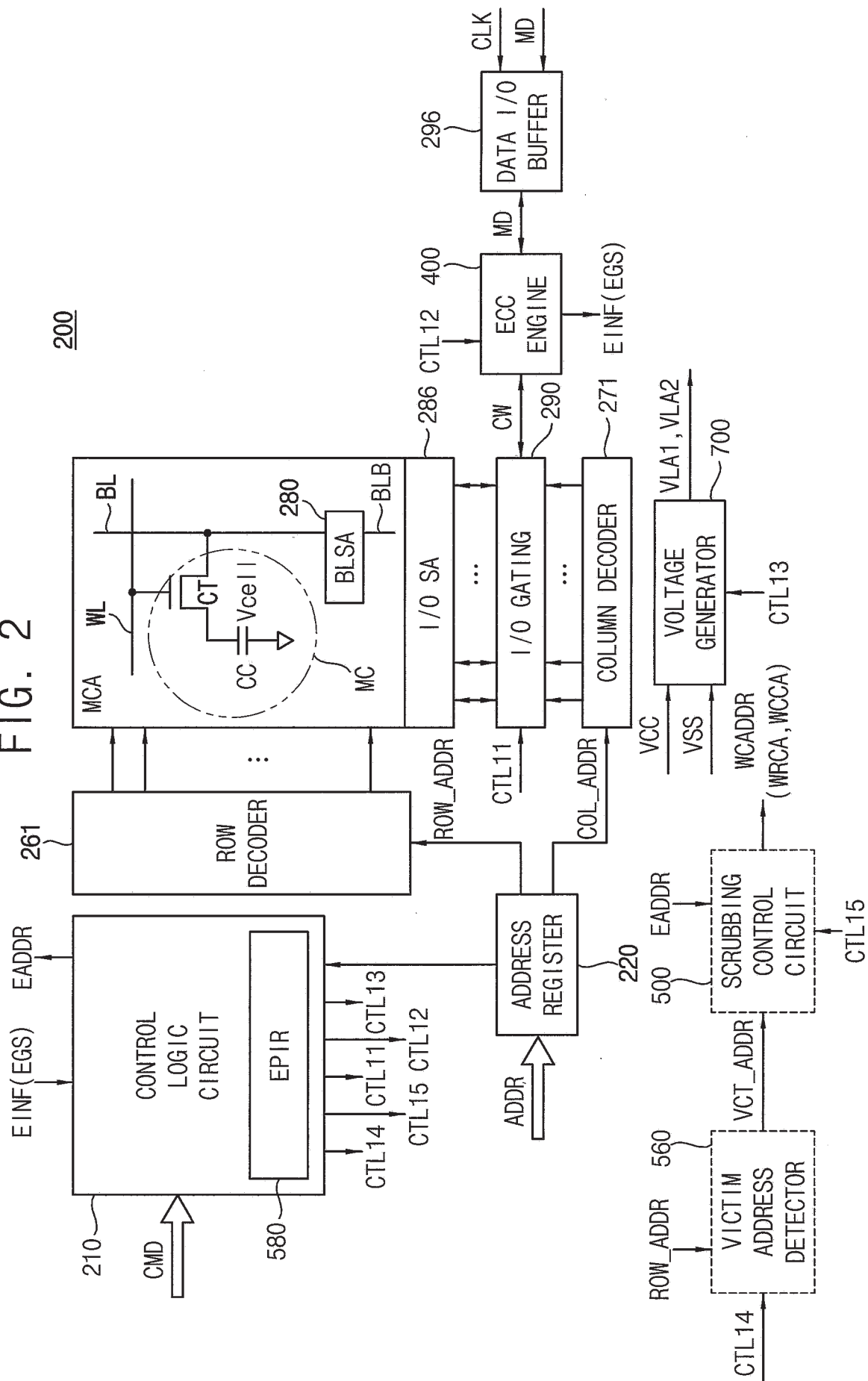


FIG. 3

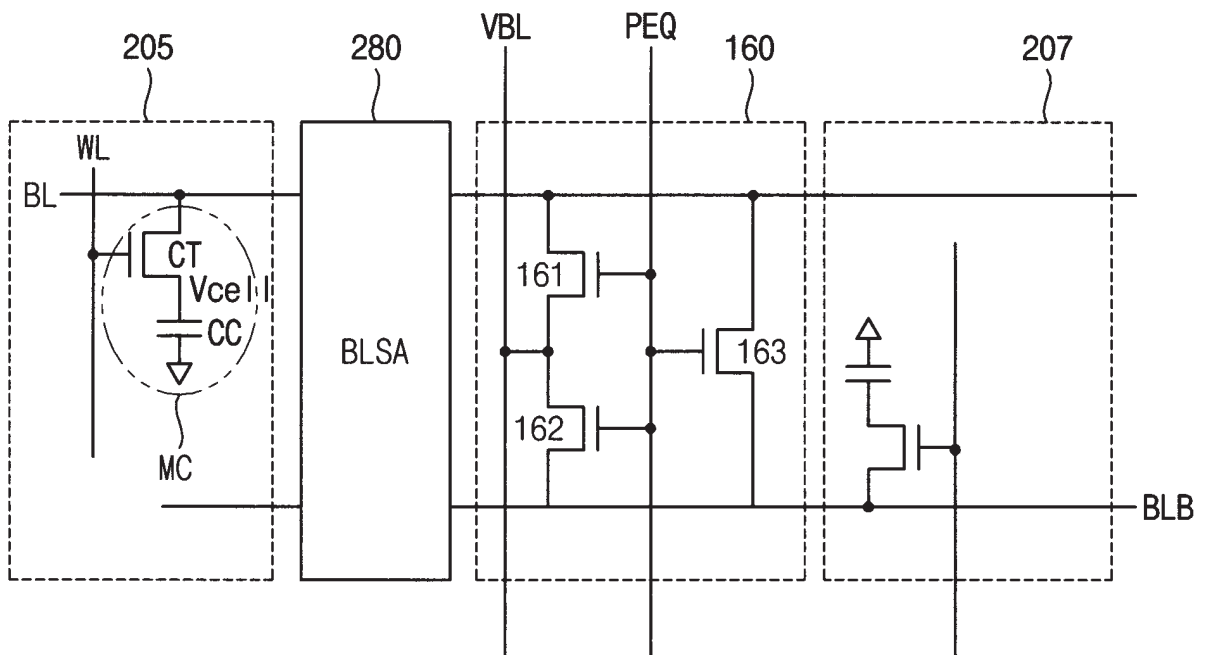


FIG. 4

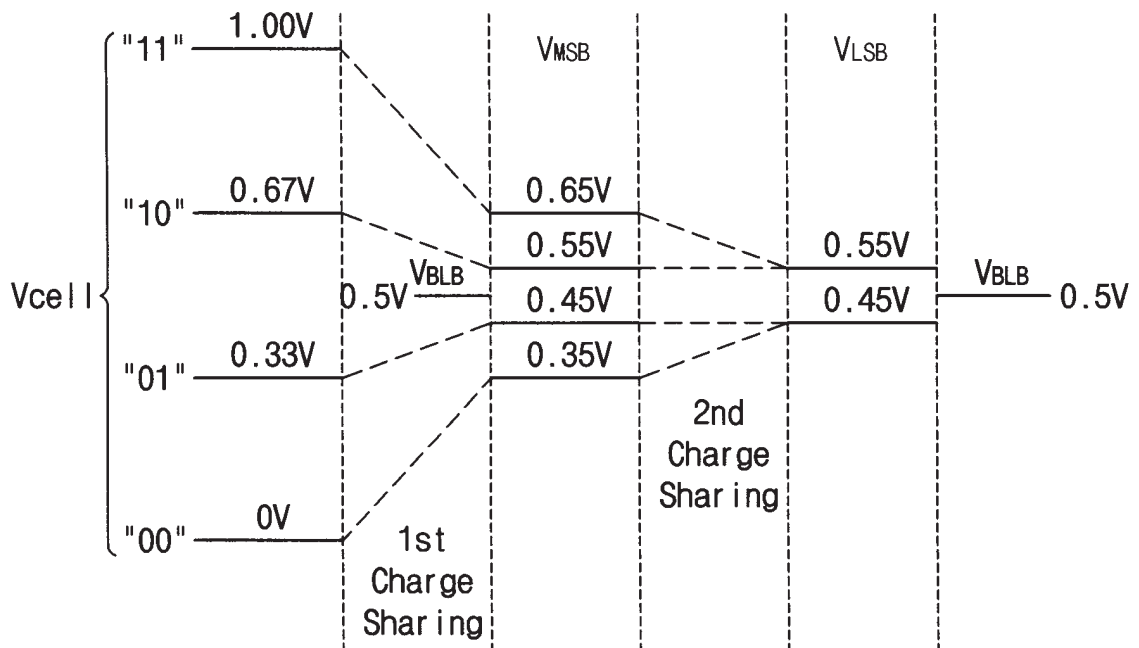


FIG. 5

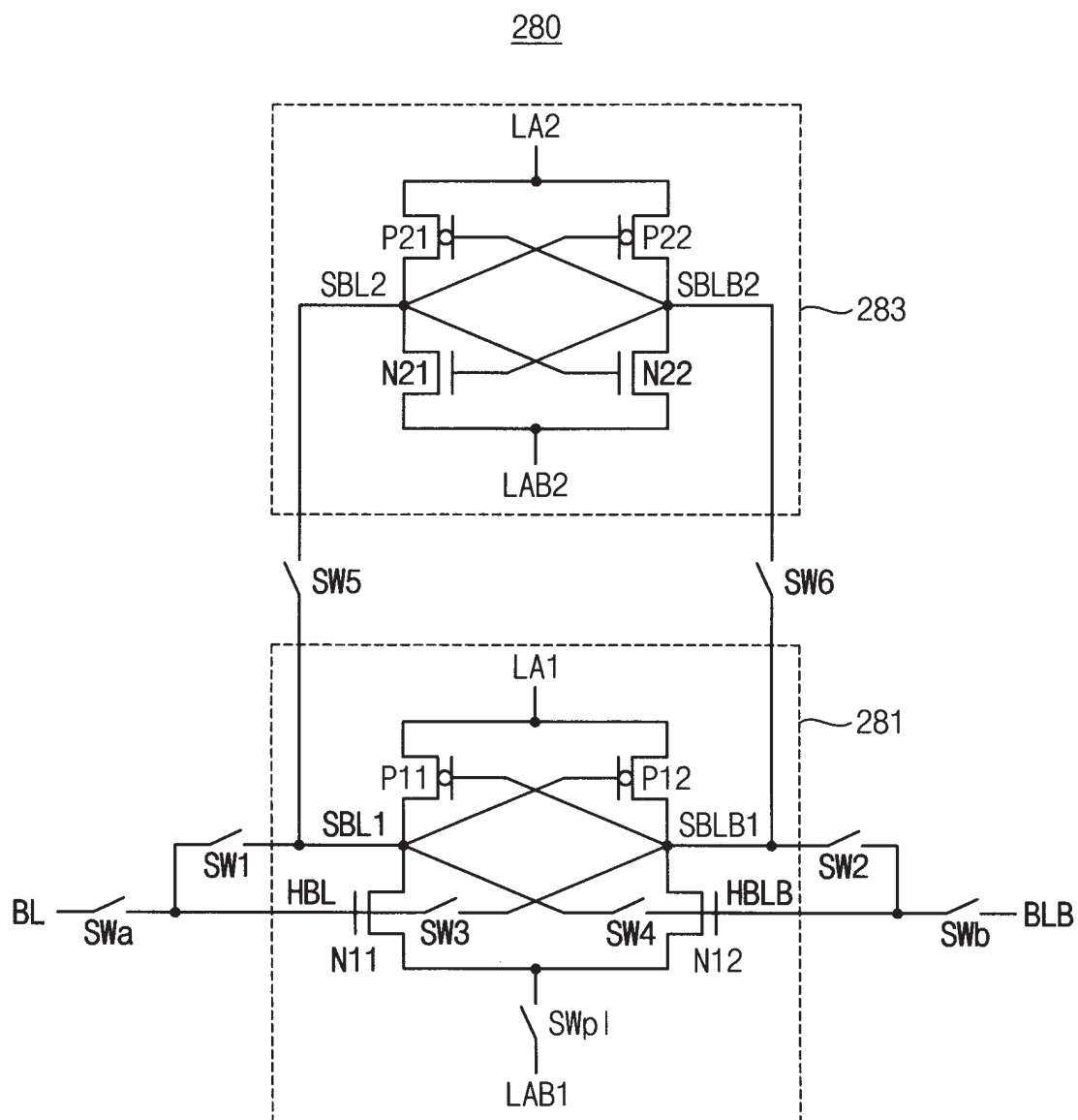


FIG. 6

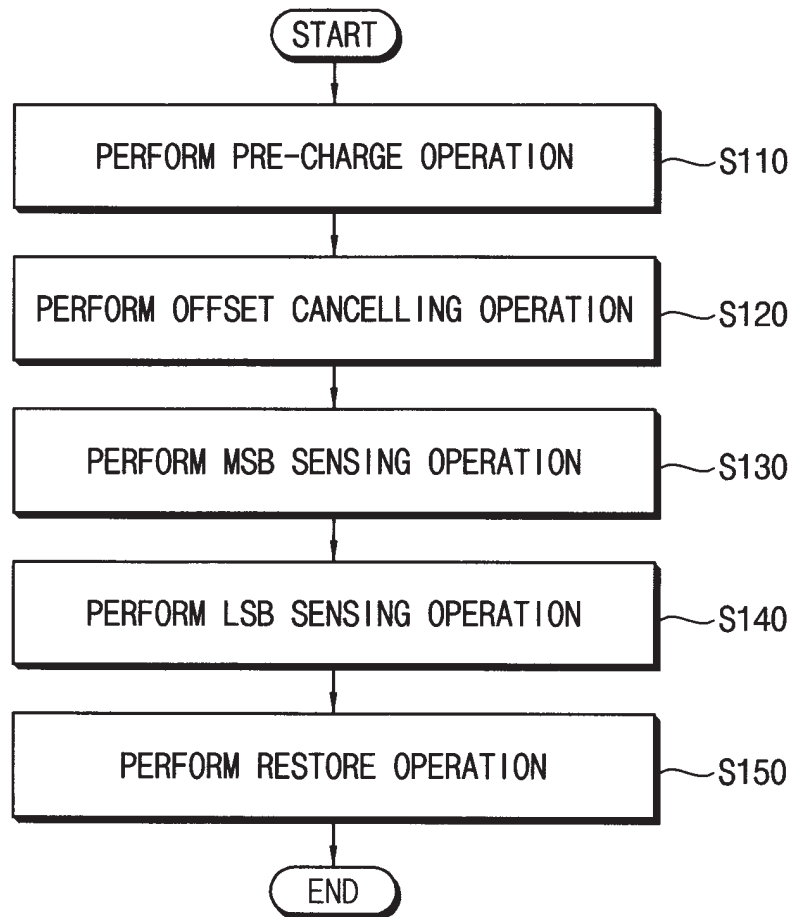


FIG. 7A

280

Pre-Charge Operation

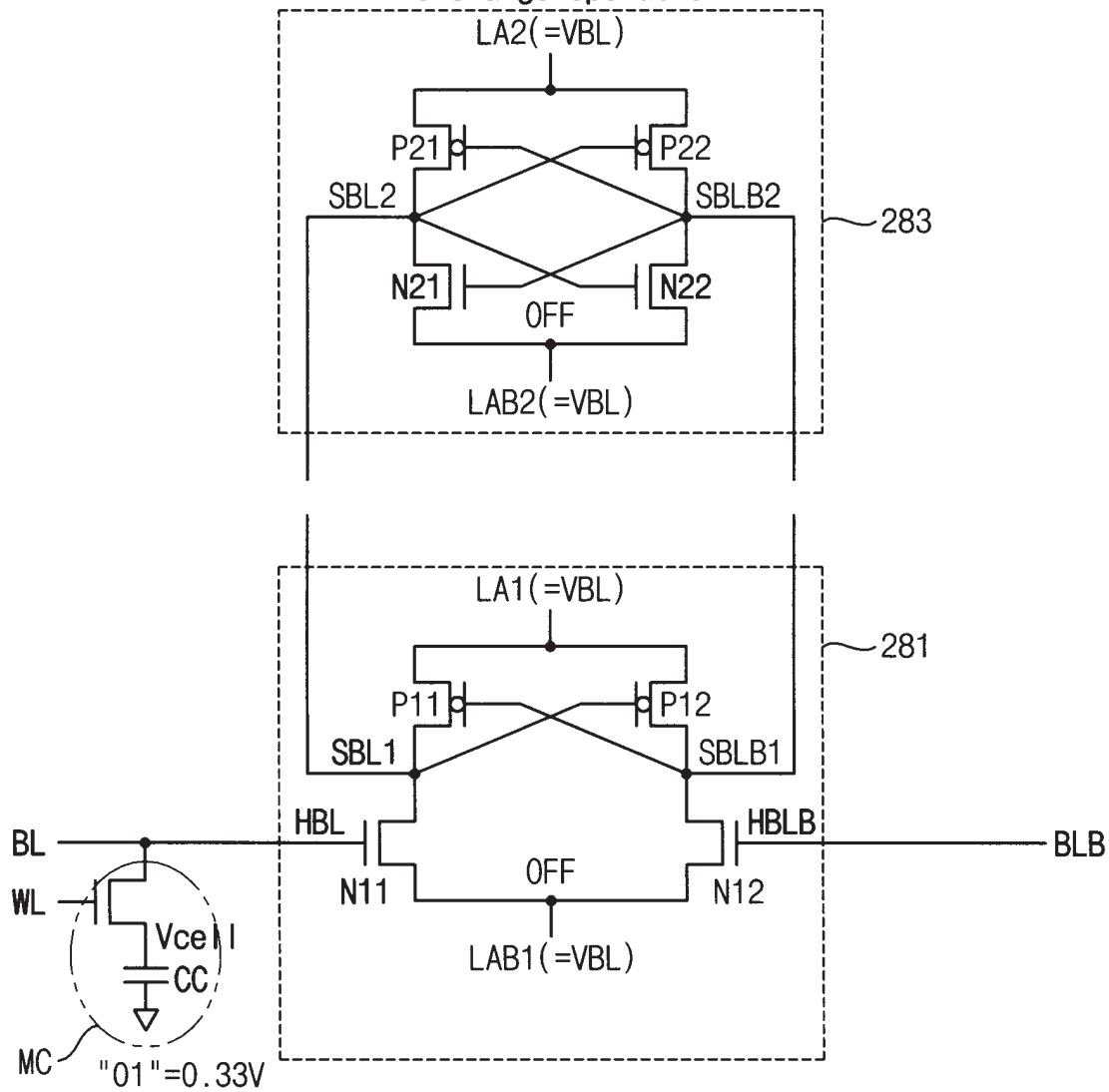


FIG. 7B

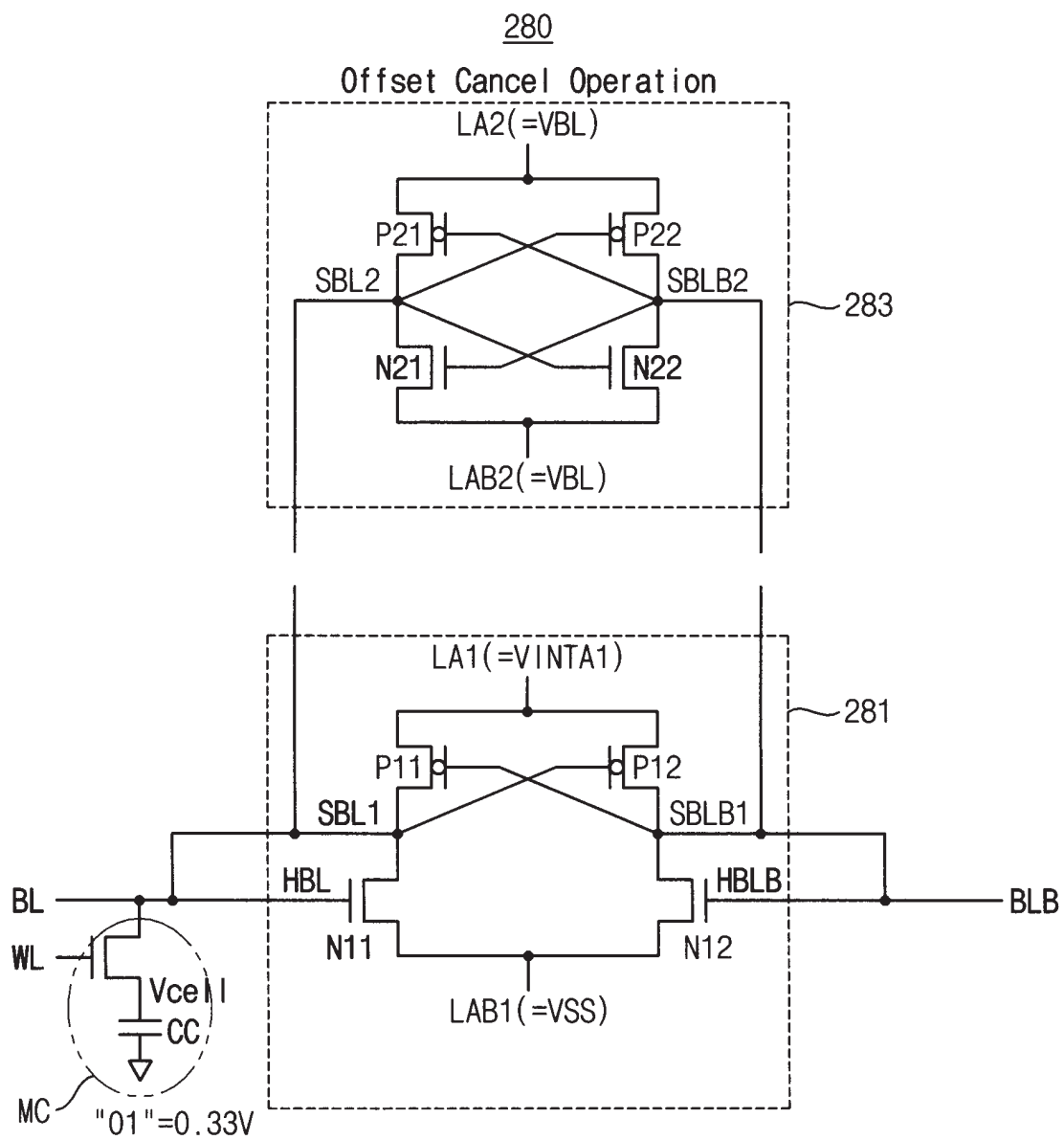


FIG. 7C

280

1st Charge Sharing Operation

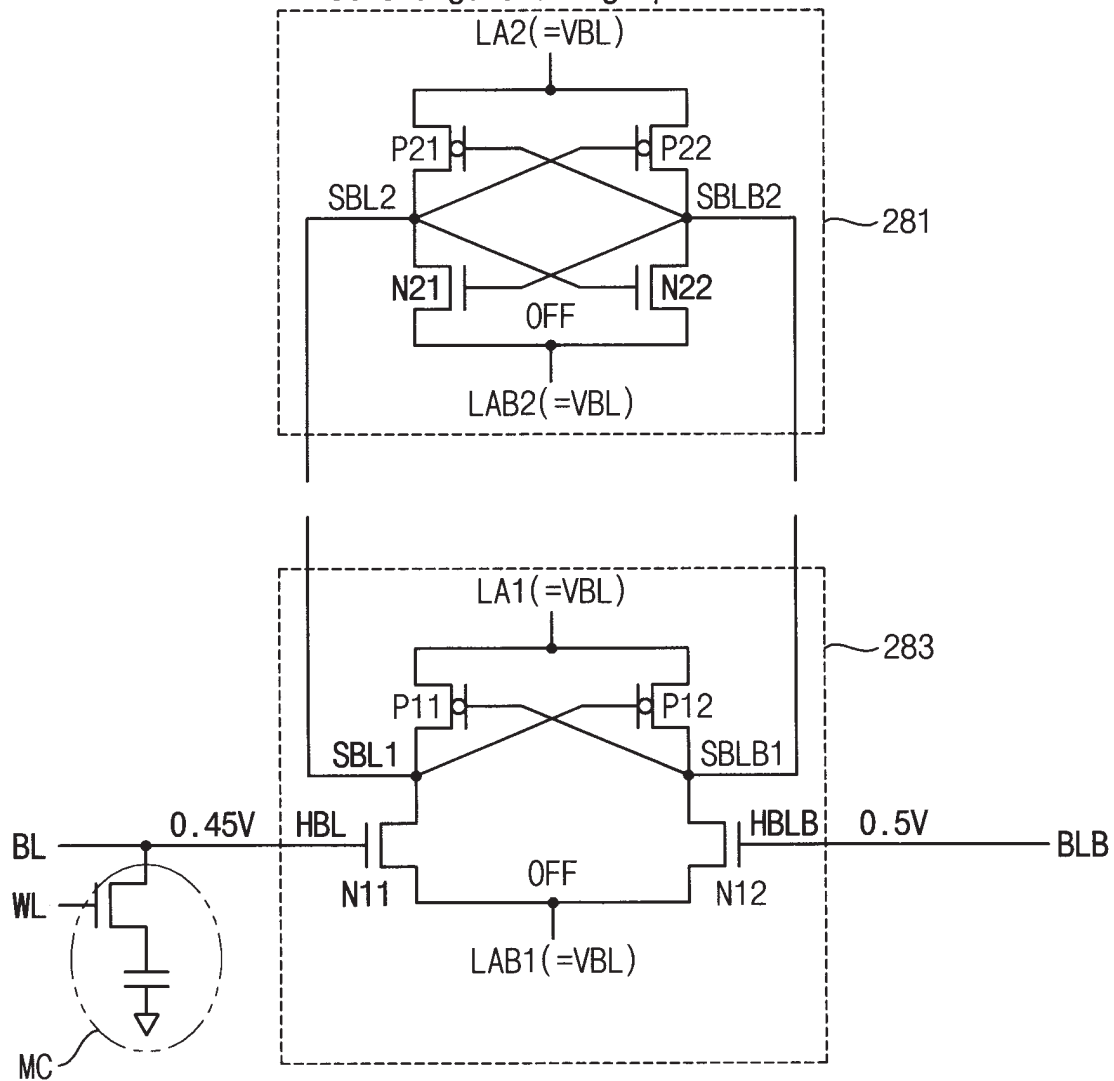


FIG. 7D

280

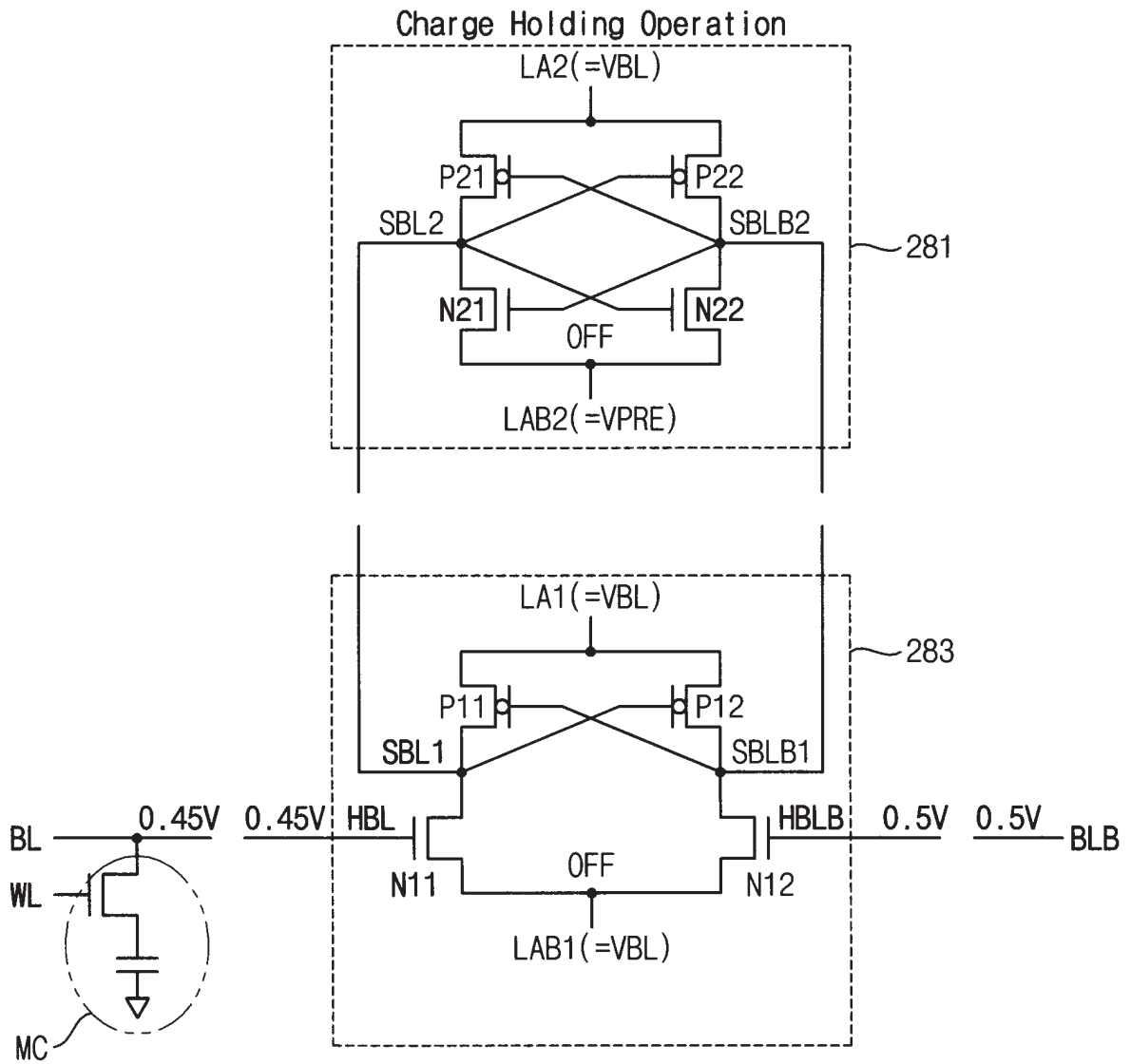


FIG. 7E

280

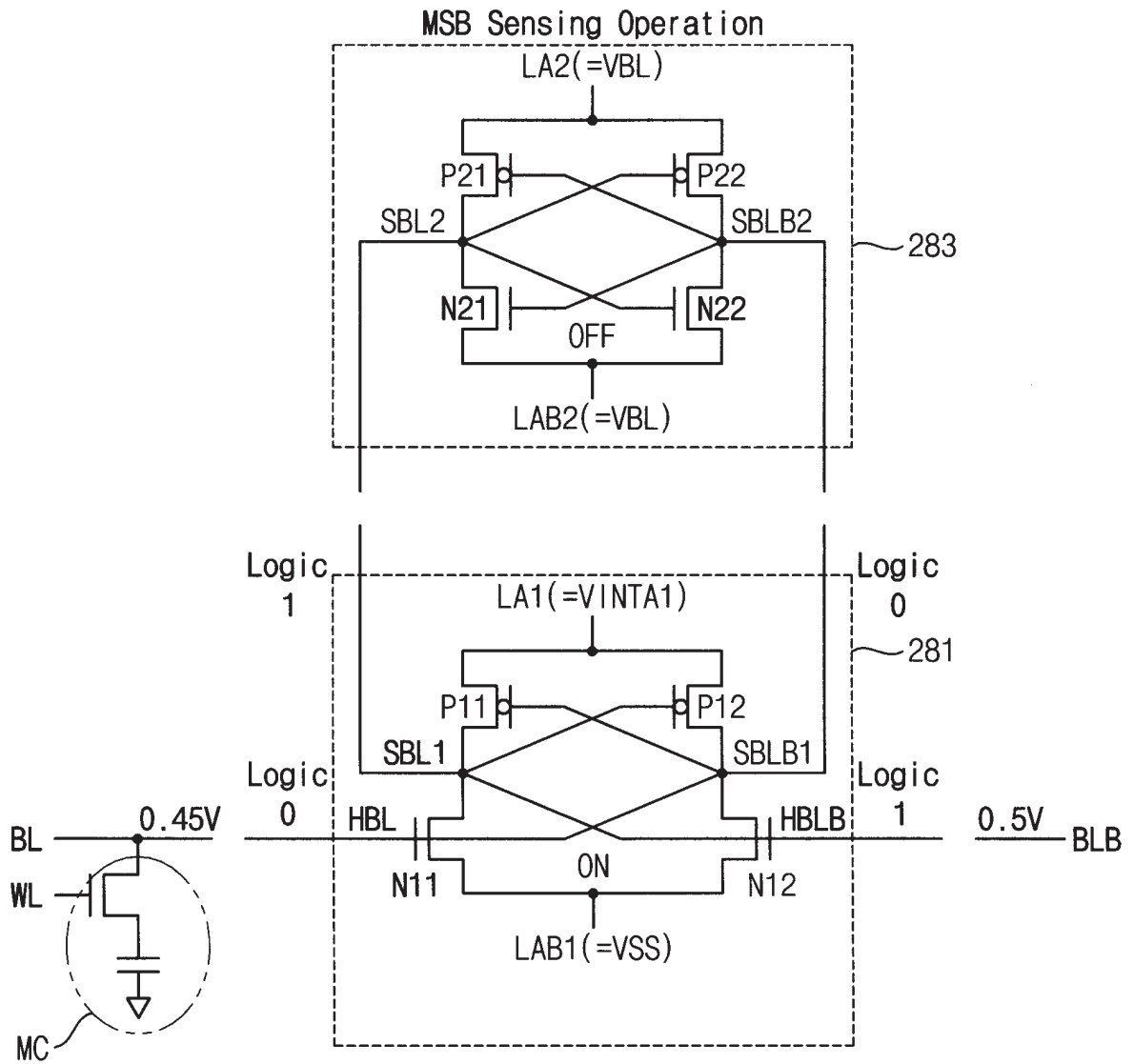


FIG. 7F

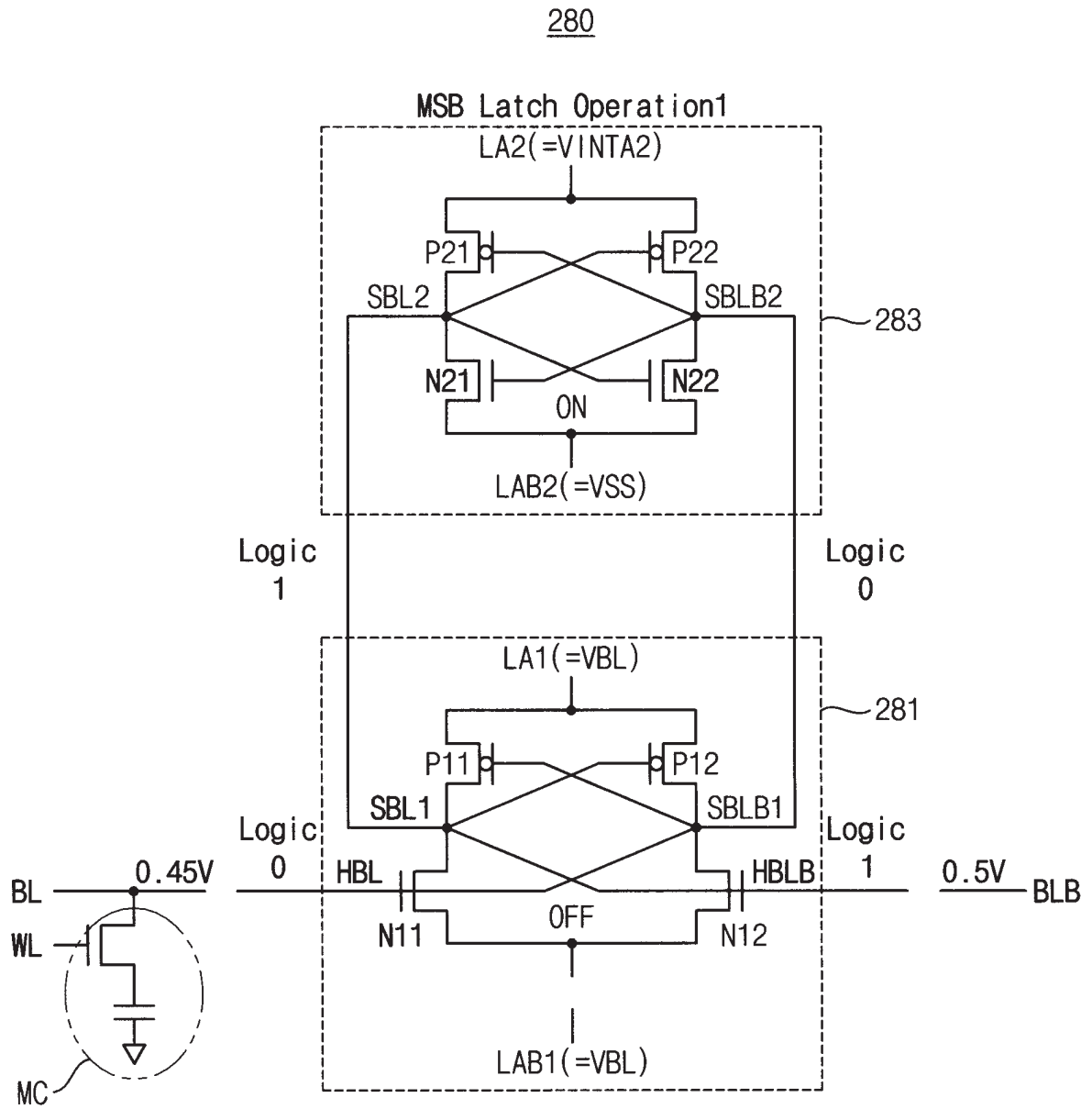


FIG. 7G

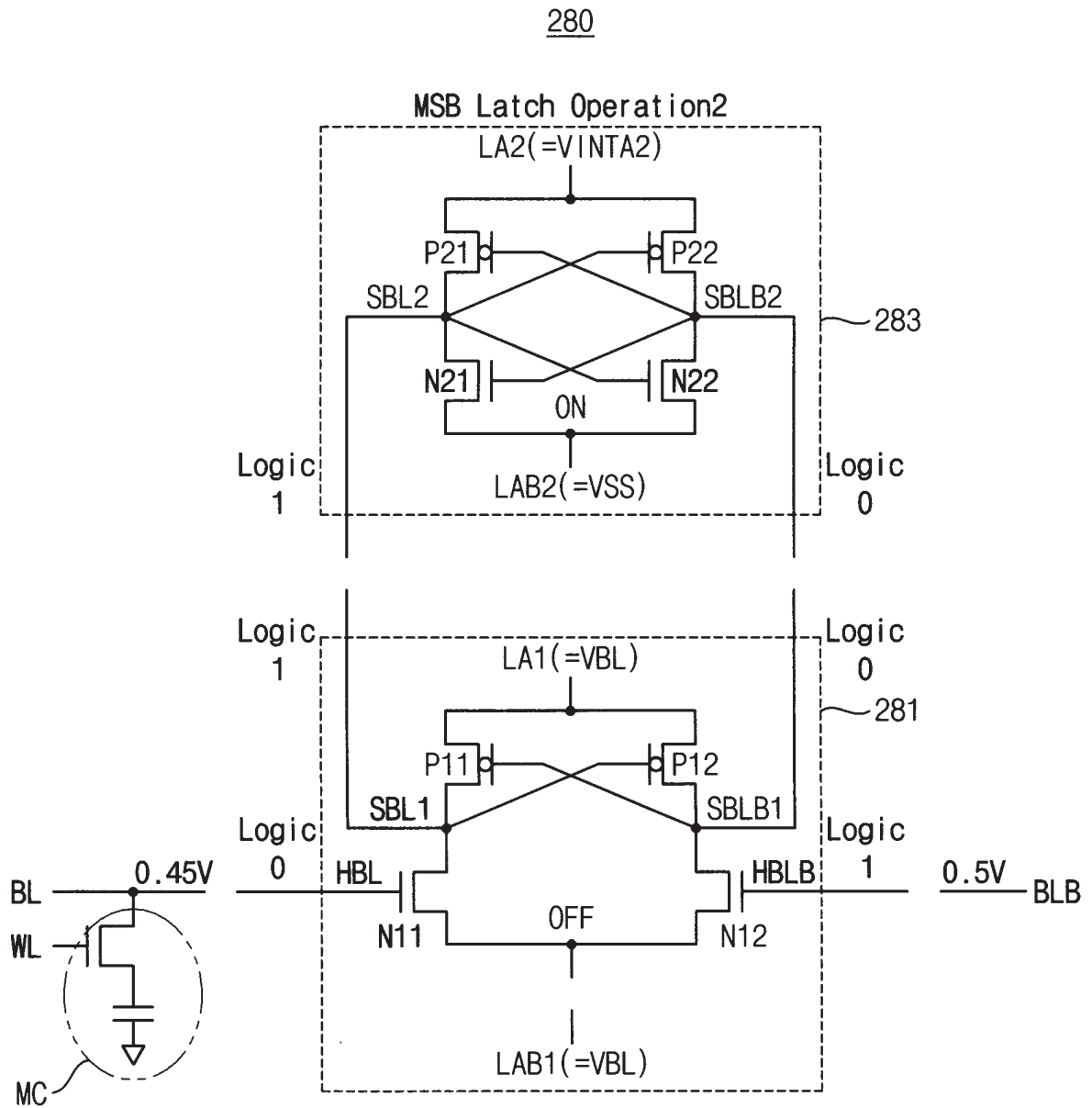


FIG. 7H

280

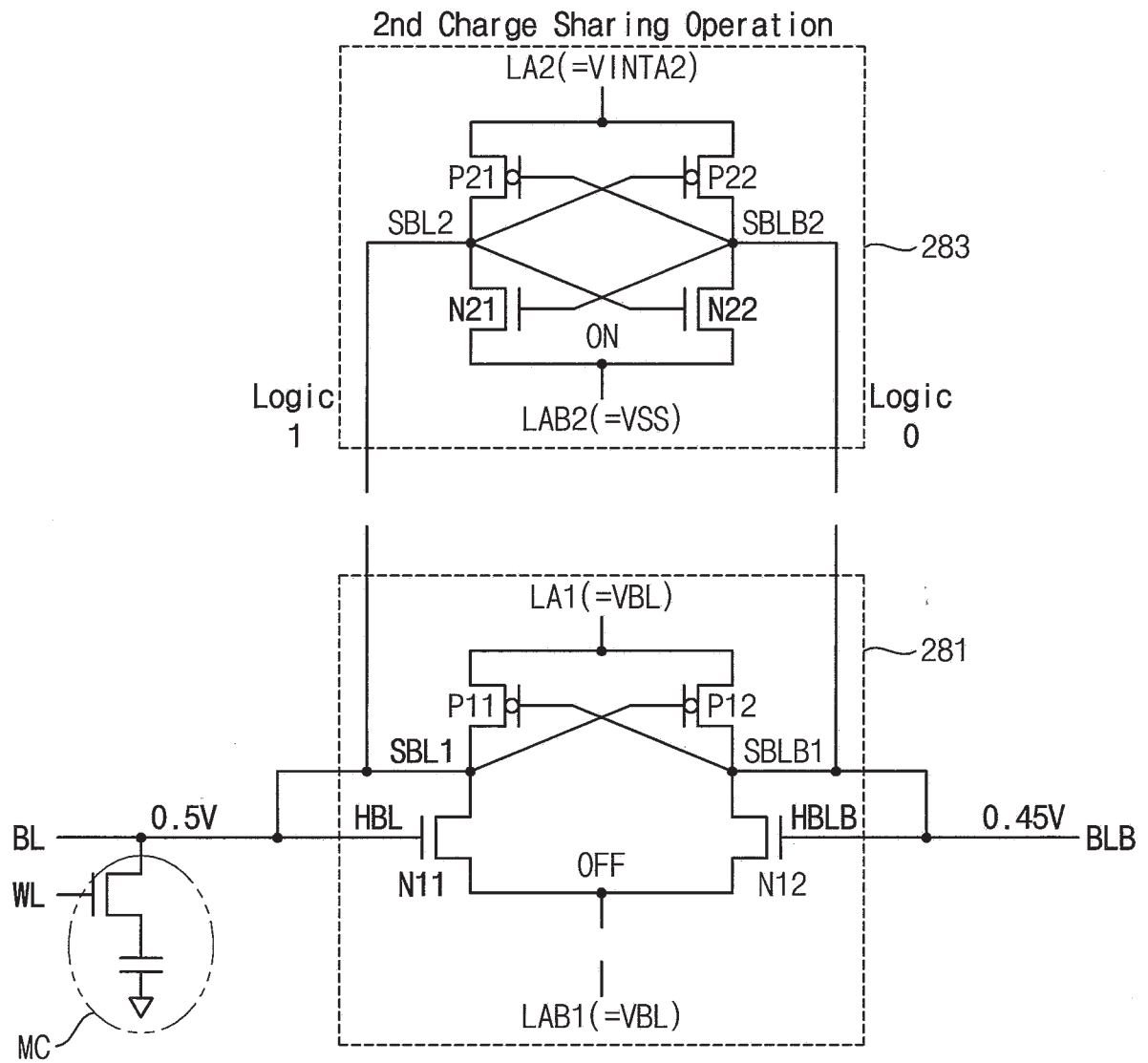


FIG. 71

280

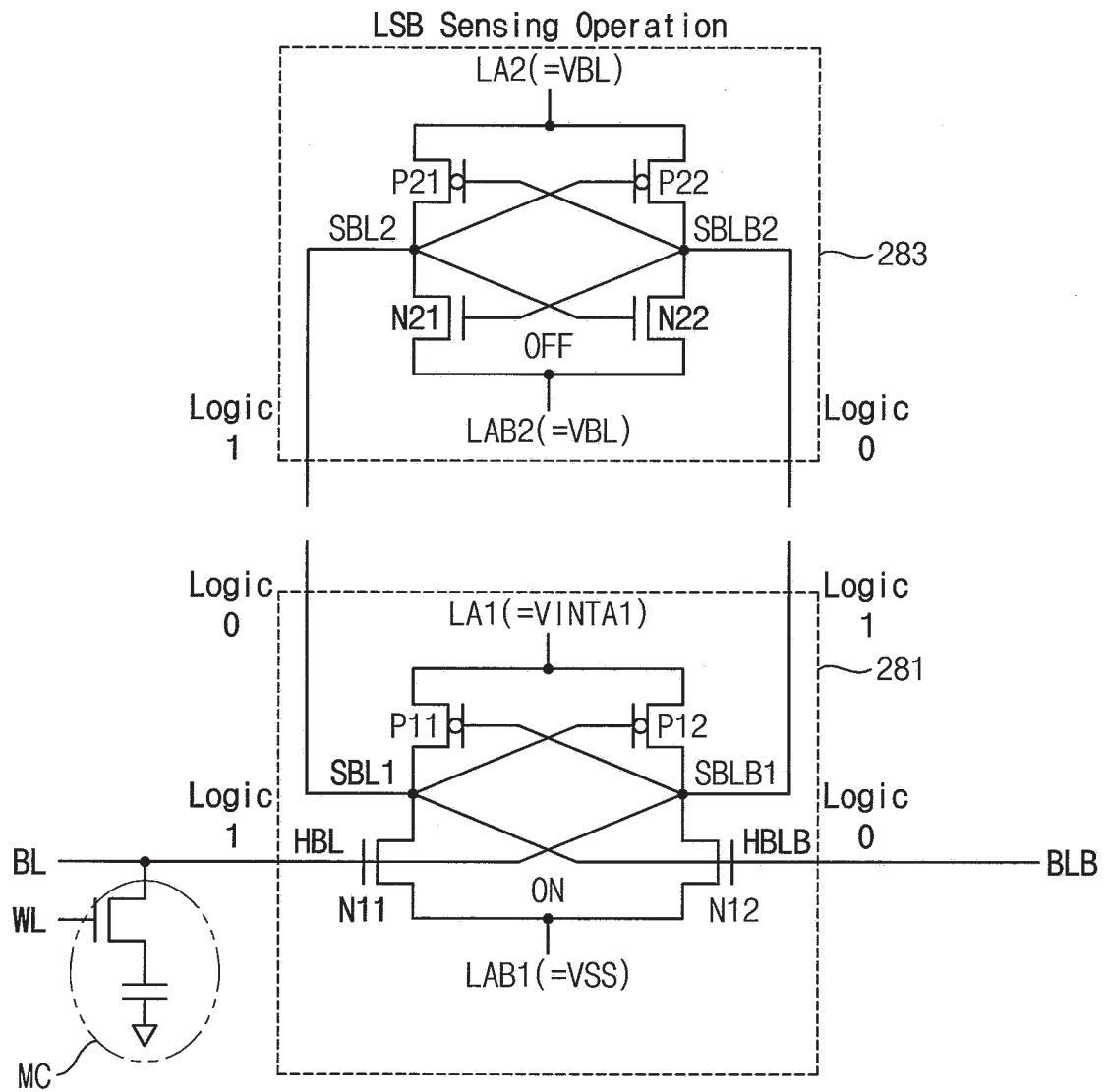


FIG. 7J

280

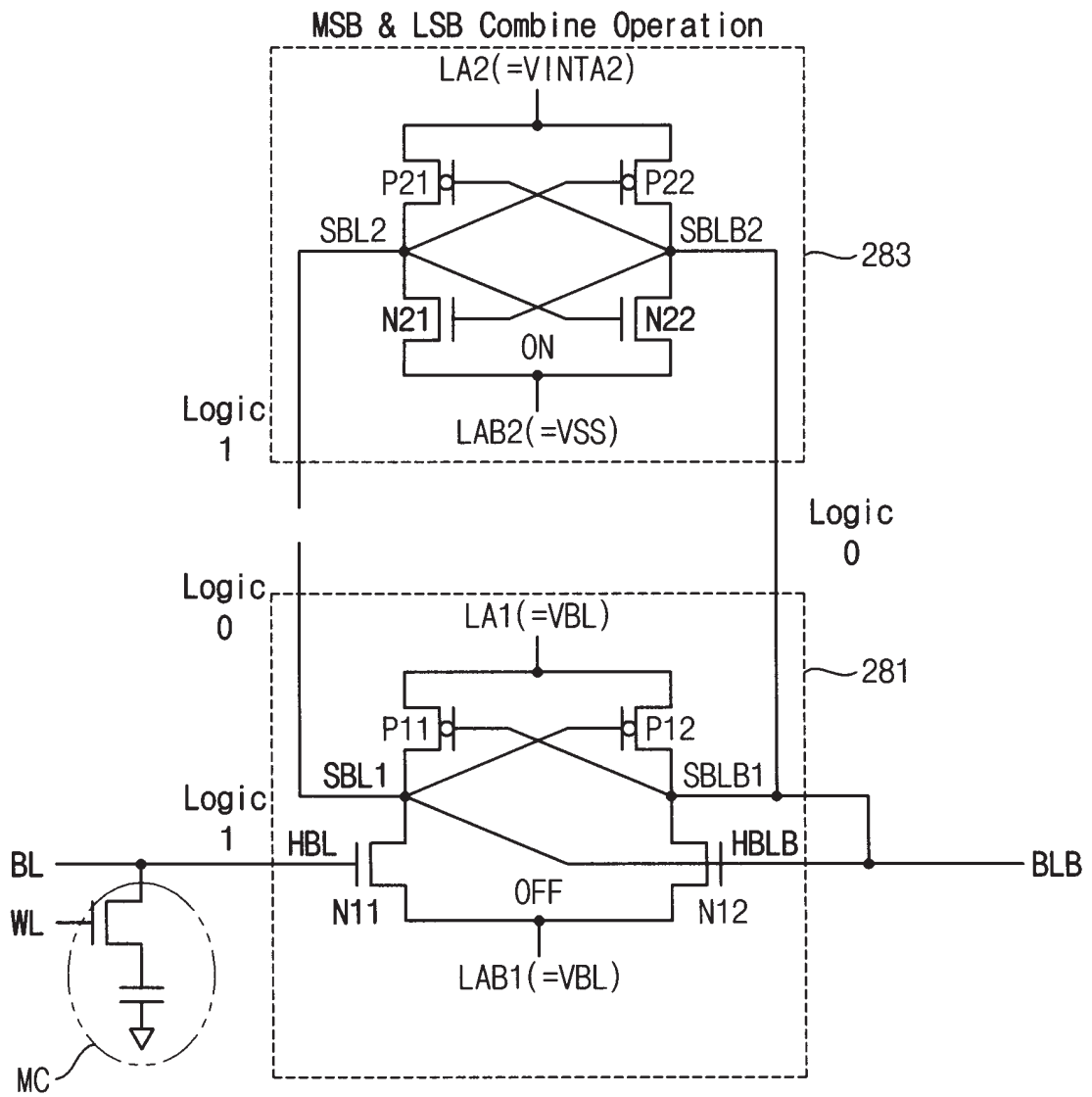


FIG. 7K

280

3rd Charge Sharing Operation

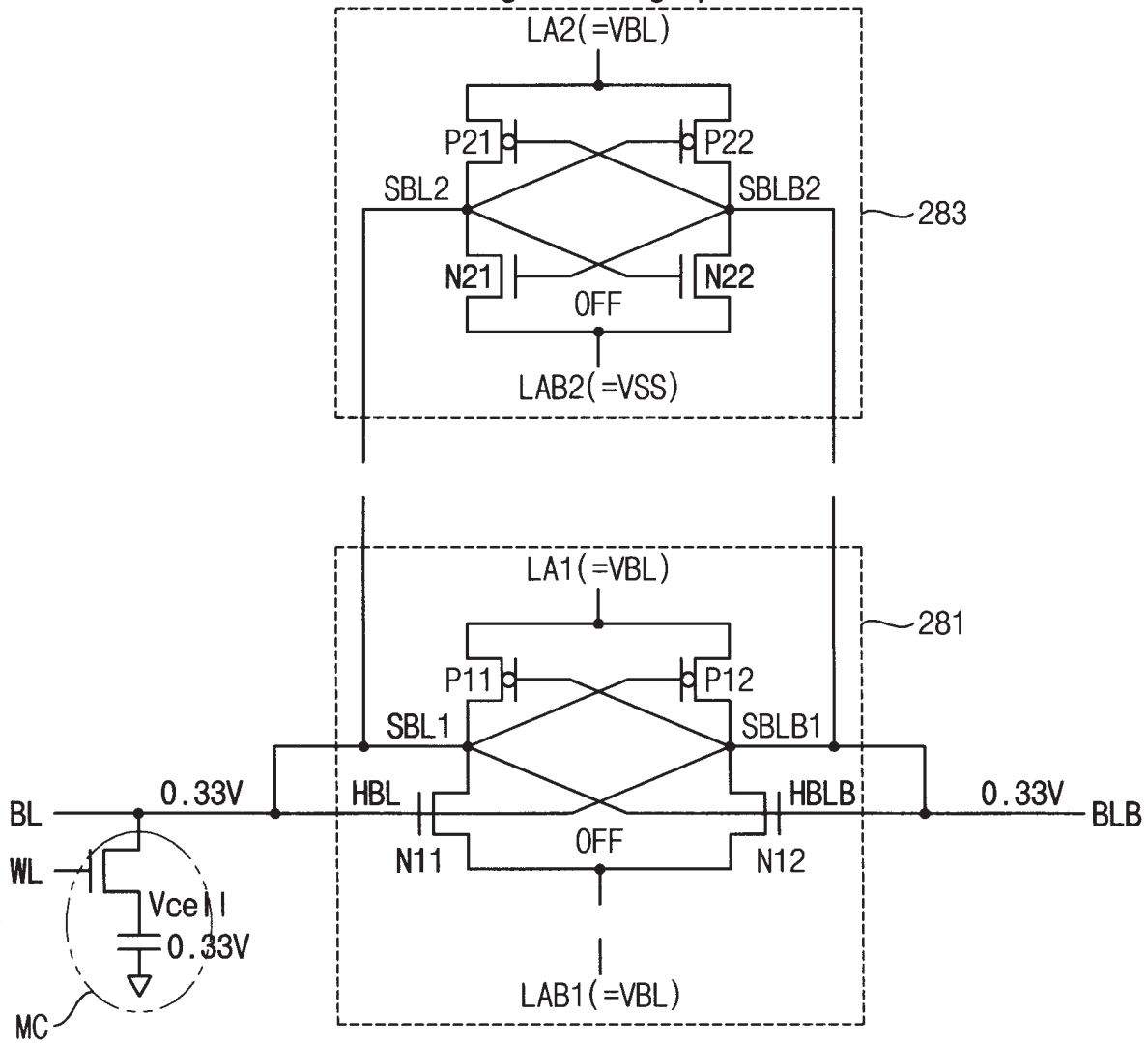


FIG. 8

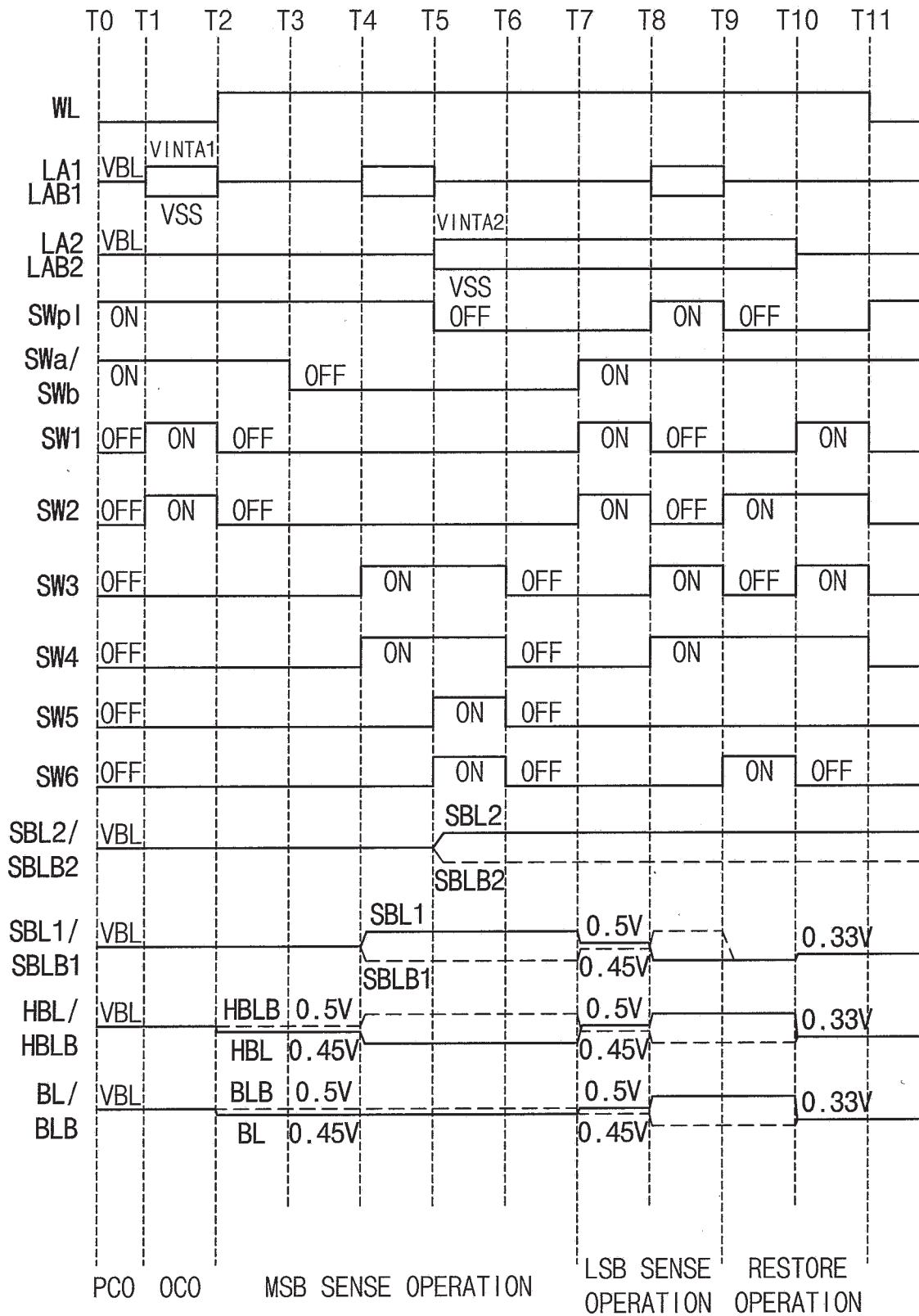


FIG. 9

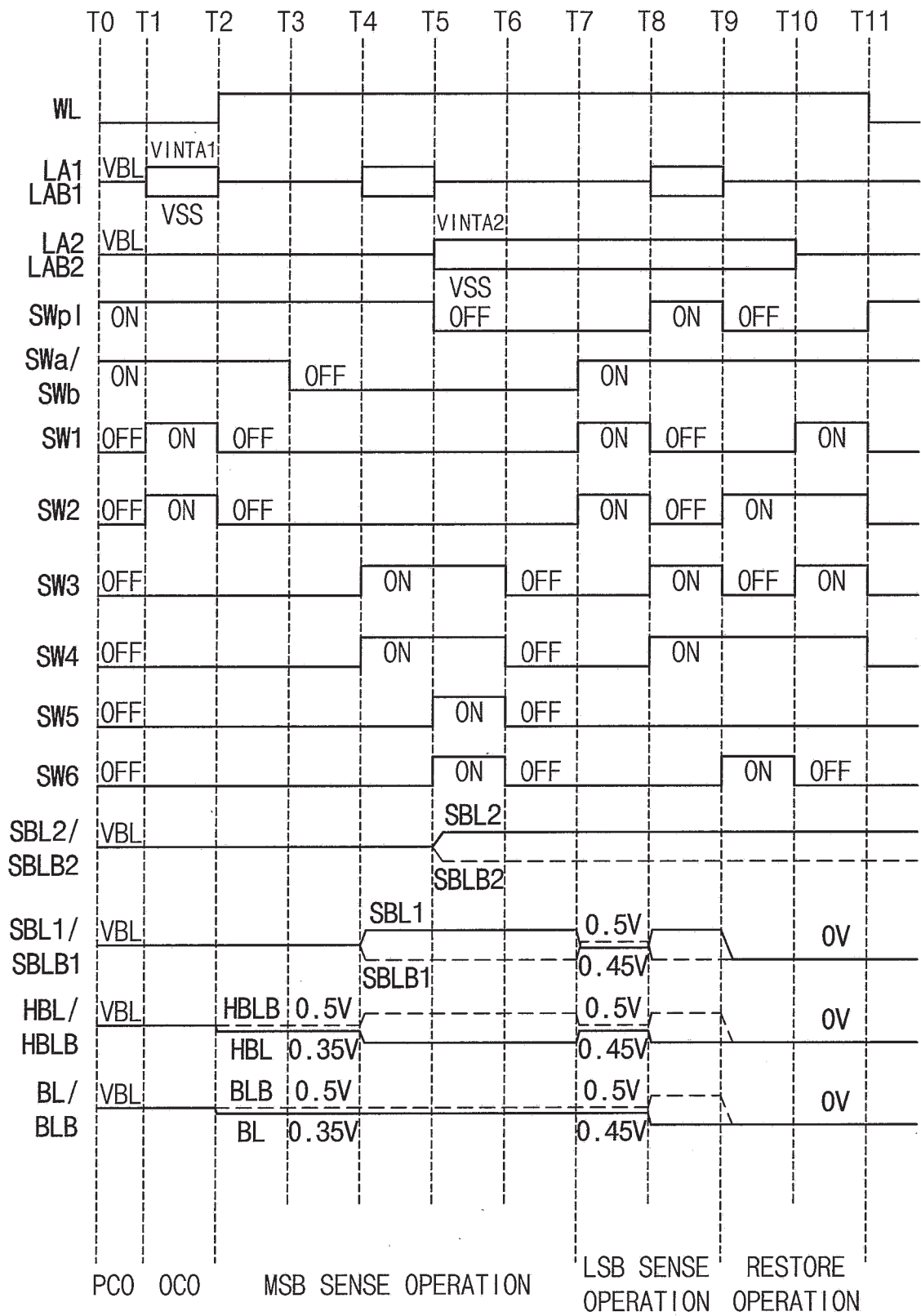


FIG. 10

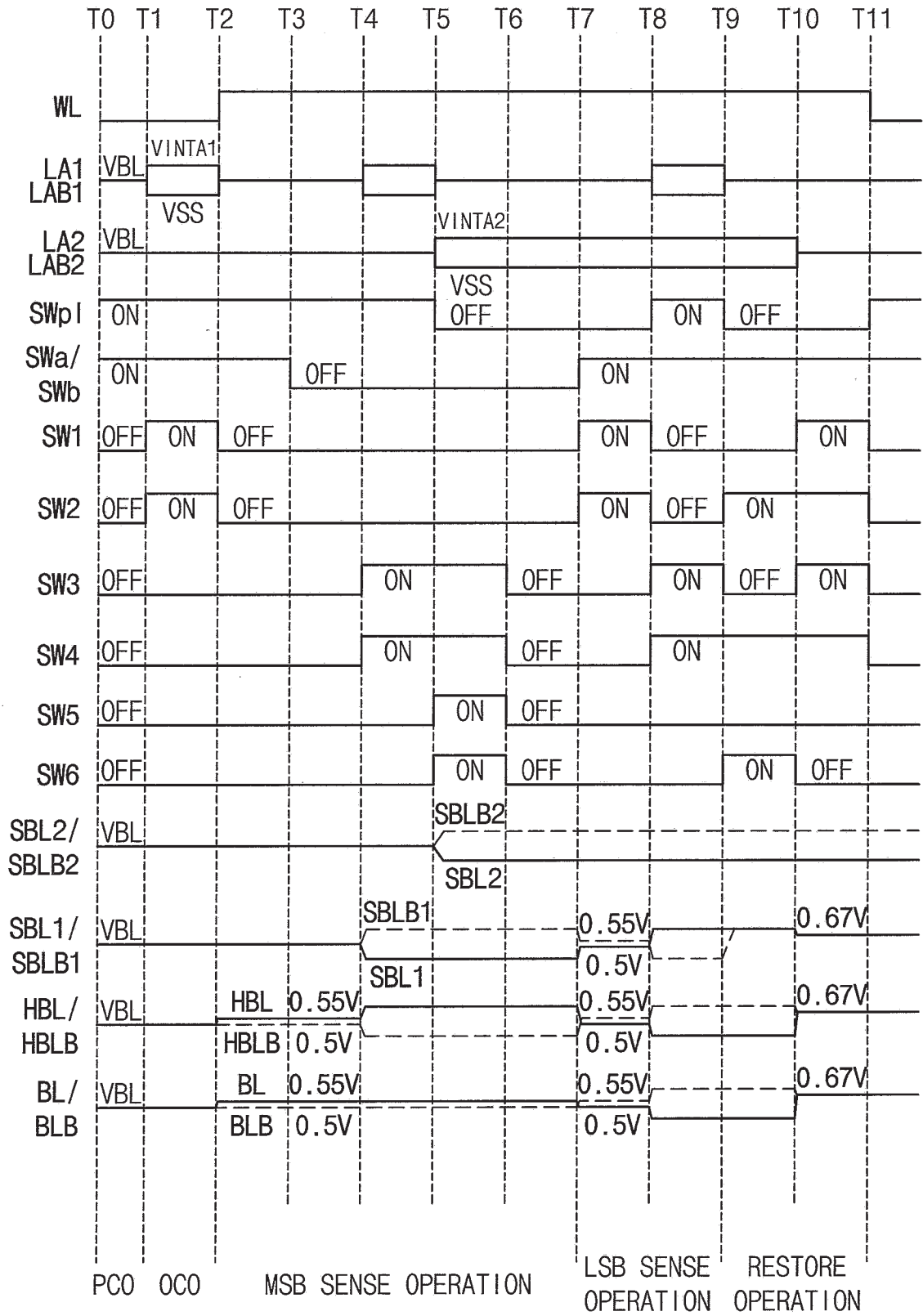


FIG. 11

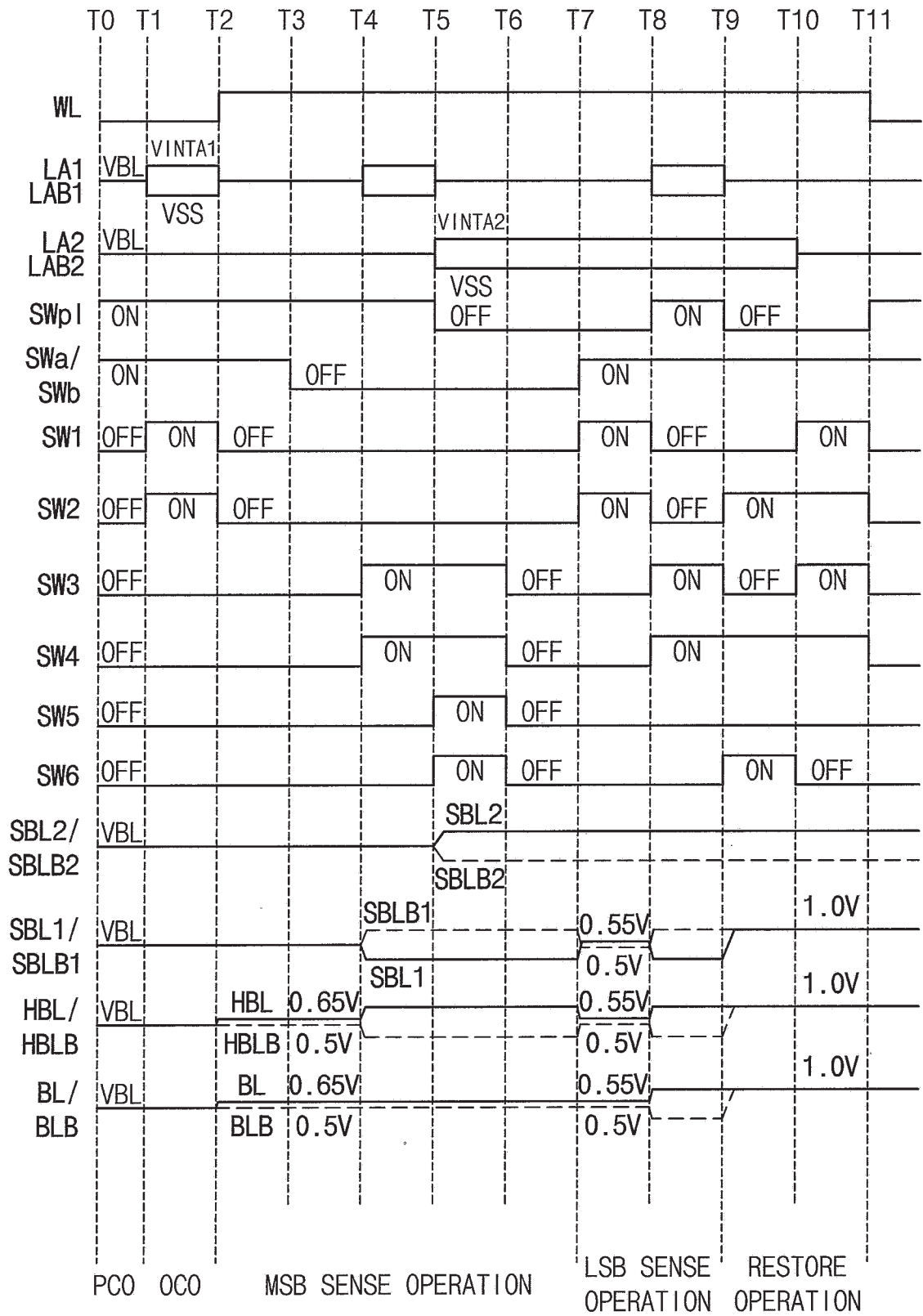


FIG. 12

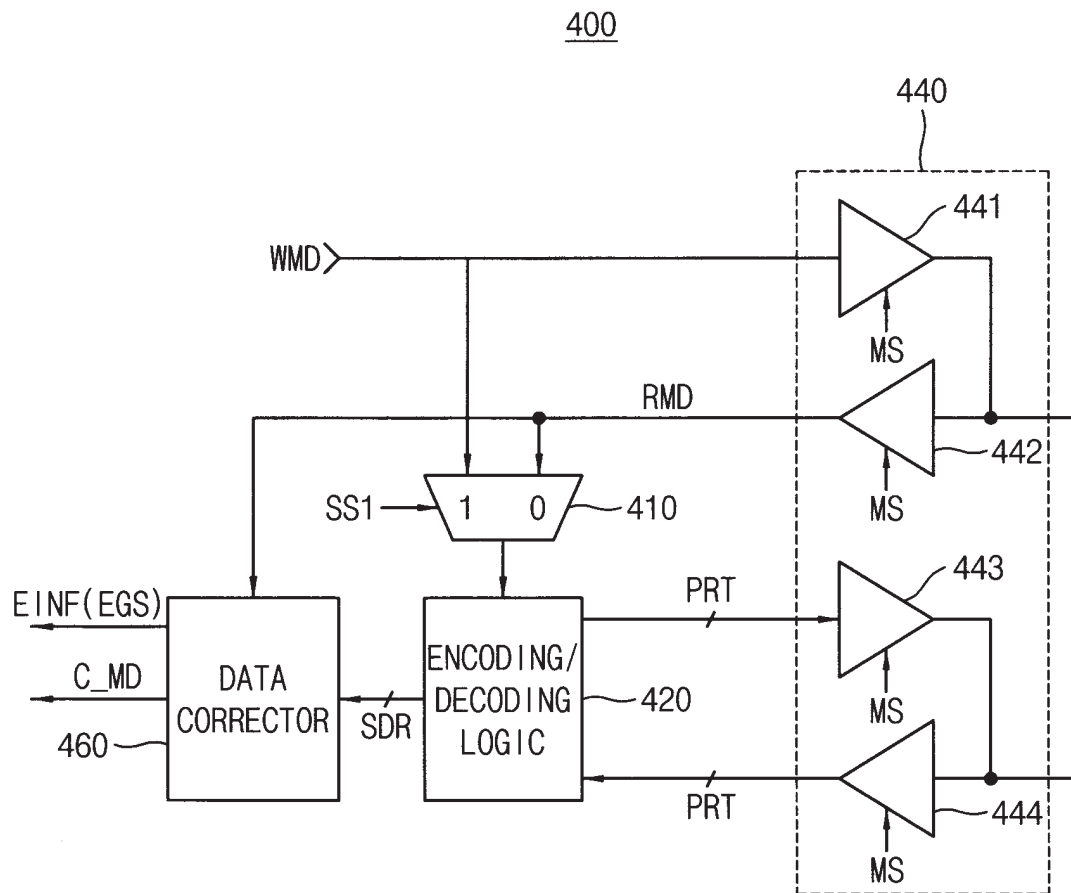


FIG. 13

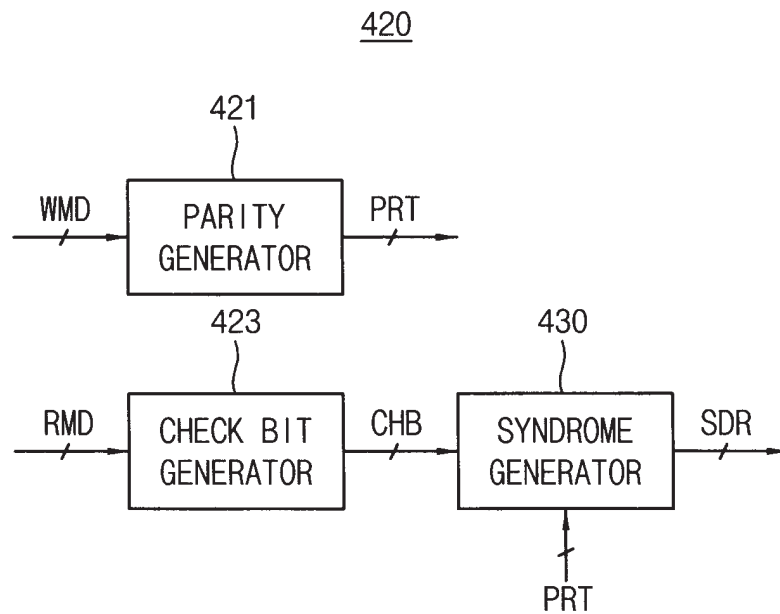


FIG. 14

460

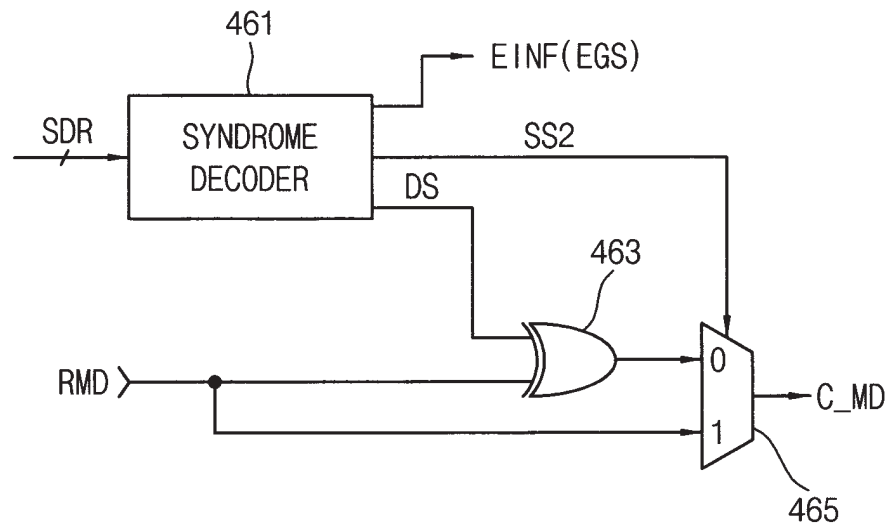


FIG. 15

200

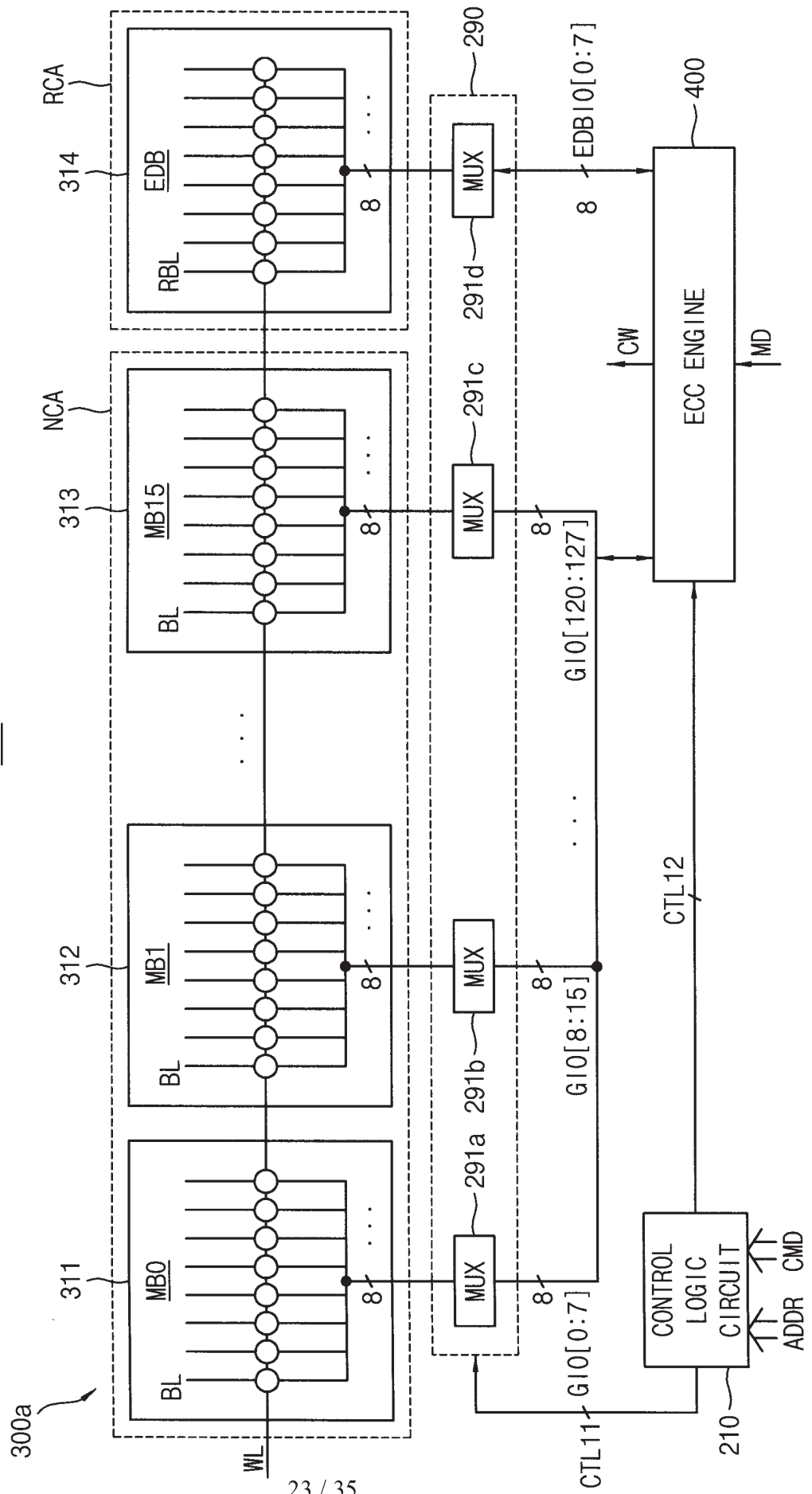


FIG. 16

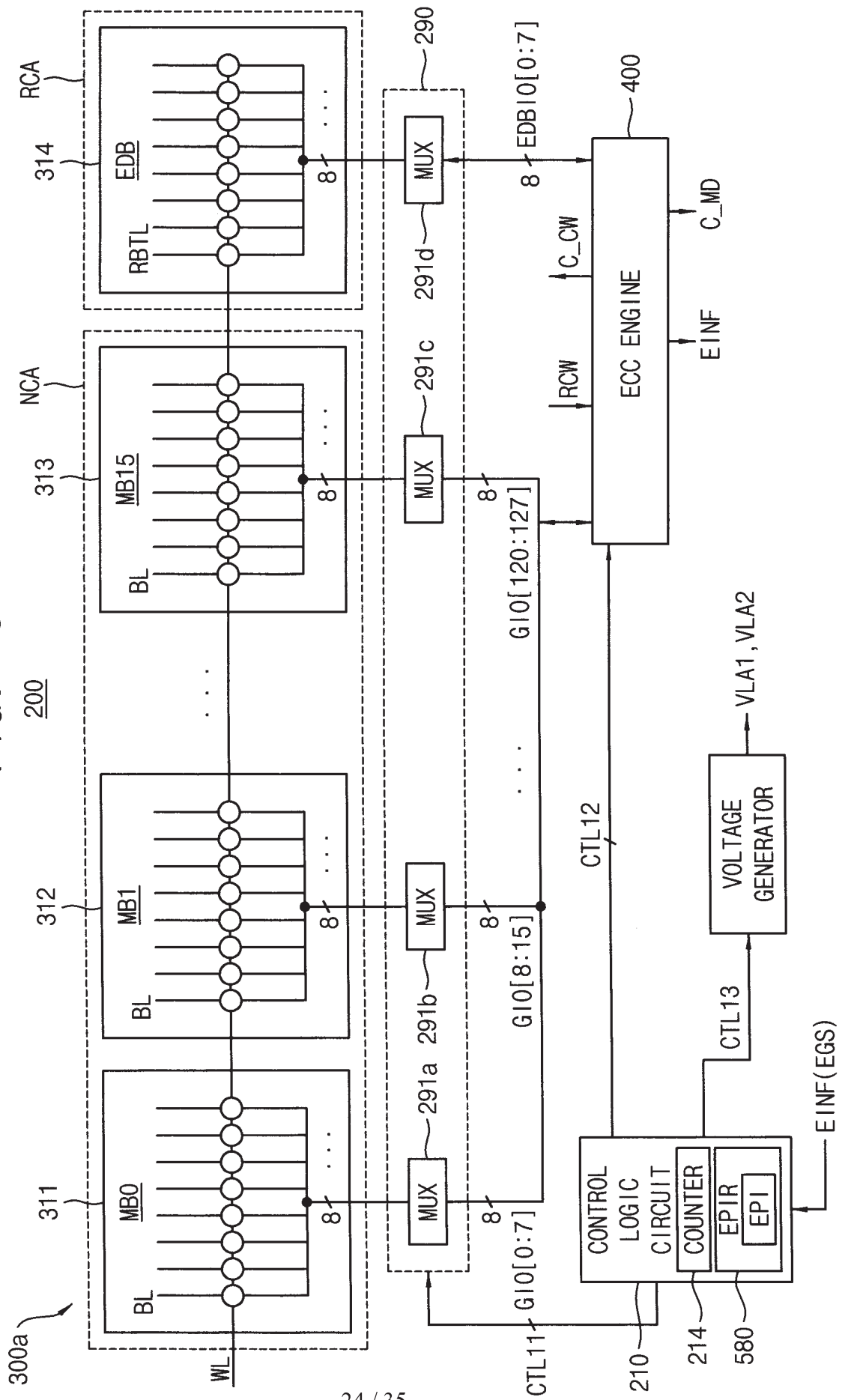


FIG. 17

580

	RNK	ADD INF (BGA,BA,RA)	ECNT	FCWCNT	FG
Idx1	2	A	2	2	0
Idx2	1	B	4	3	0
⋮	⋮	⋮	⋮	⋮	⋮
Idxu	3	X	1	1	1

↘
581
↘
582
↘
583
↘
584
↘
585

FIG. 18

700

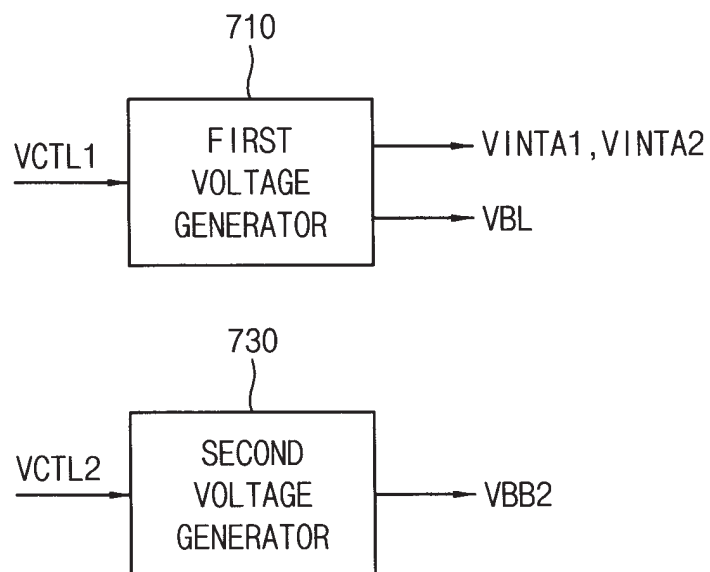


FIG. 19

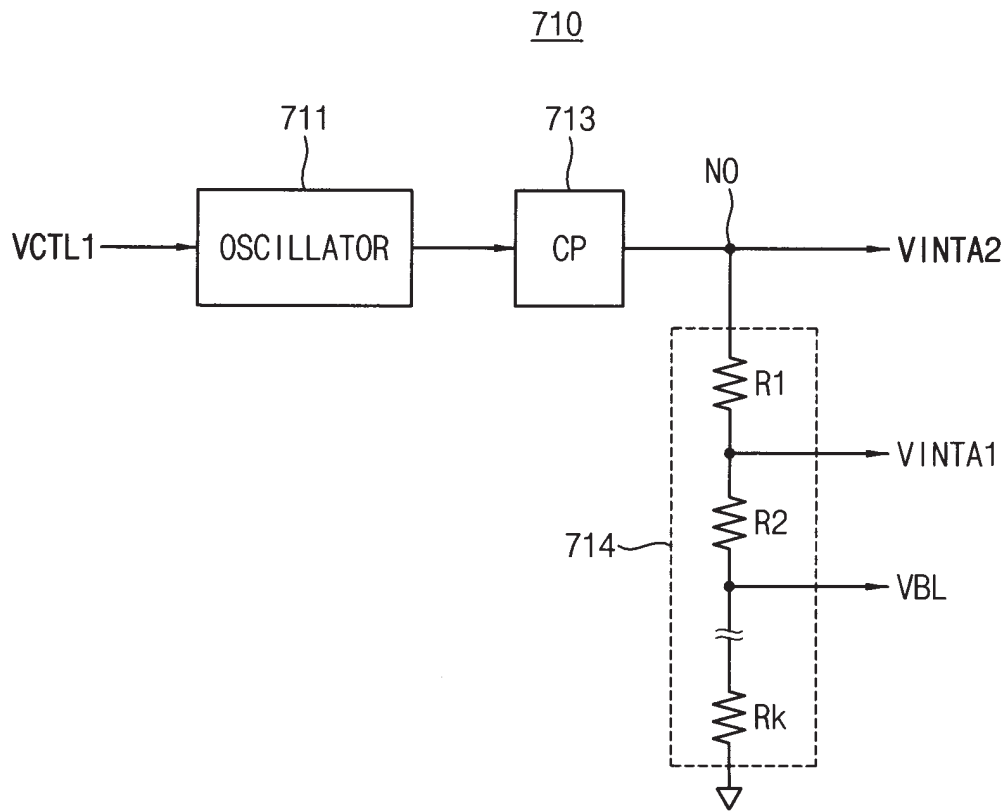


FIG. 20

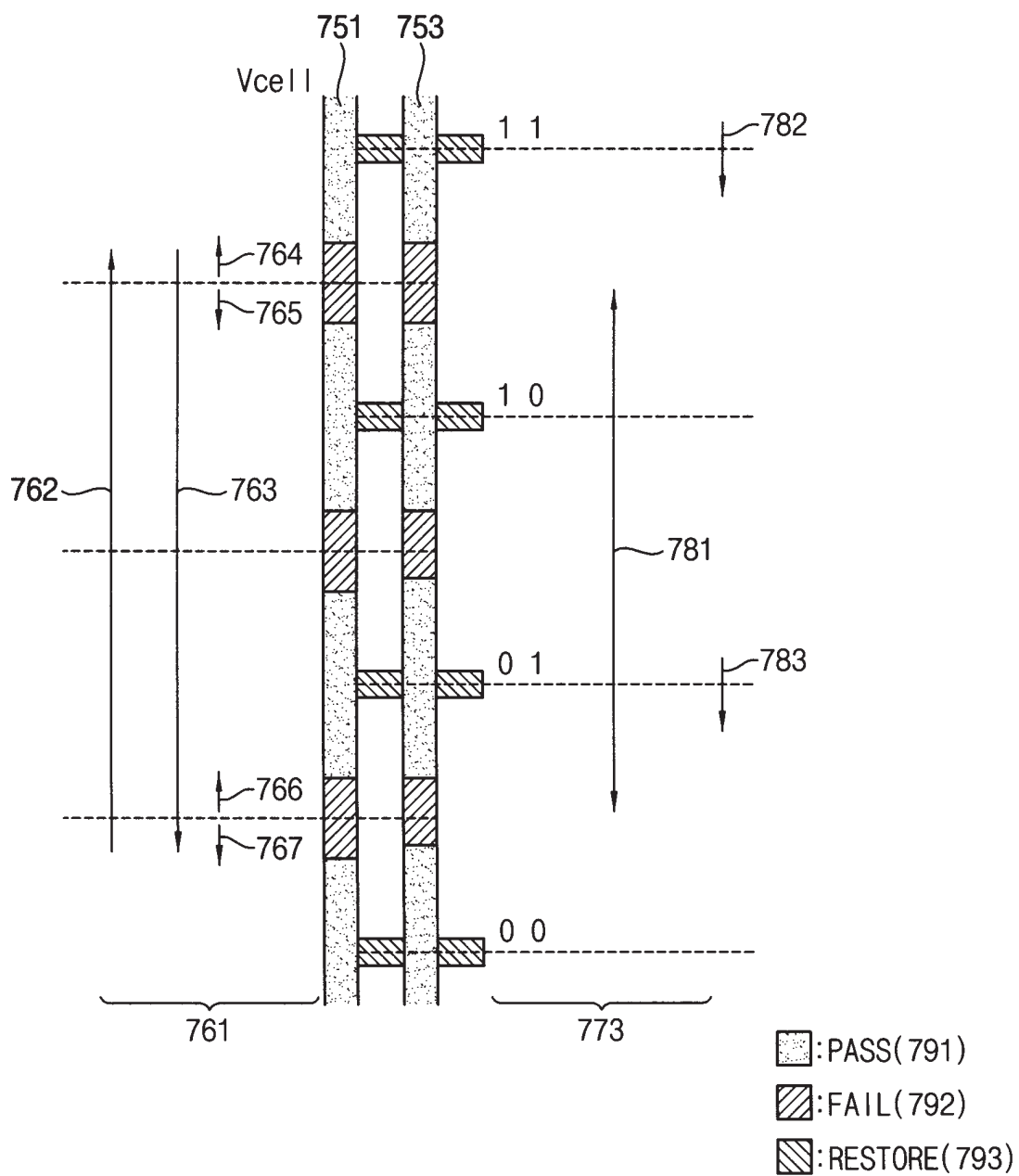


FIG. 21A

MULTI-BIT	DC CONTROL
1 1	VINTA1 UP
1 ☐	
0 ☐	
0 0	

☐:ERROR

FIG. 21B

MULTI-BIT	DC CONTROL
1 ☐	VINTA1 DOWN
1 0	
0 1	
0 ☐	

☐:ERROR

FIG. 21C

MULTI-BIT	DC CONTROL
1 1	VBL DOWN
1 0	
0 1	
0 0	

:ERROR

FIG. 21D

MULTI-BIT	DC CONTROL
1 1	VBL UP
1 0	
0 1	
0 0	

:ERROR

FIG. 21E

MULTI-BIT	DC CONTROL
1 ☐	VINTA2 & VBB2 UP
☐ 0	
☐ 1	
0 ☐	

☐:ERROR

FIG. 21F

MULTI-BIT	DC CONTROL
☐ 1	VIN2A & VBB2 DOWN
1 ☐	
0 ☐	
☐ 0	

☐:ERROR

FIG. 22

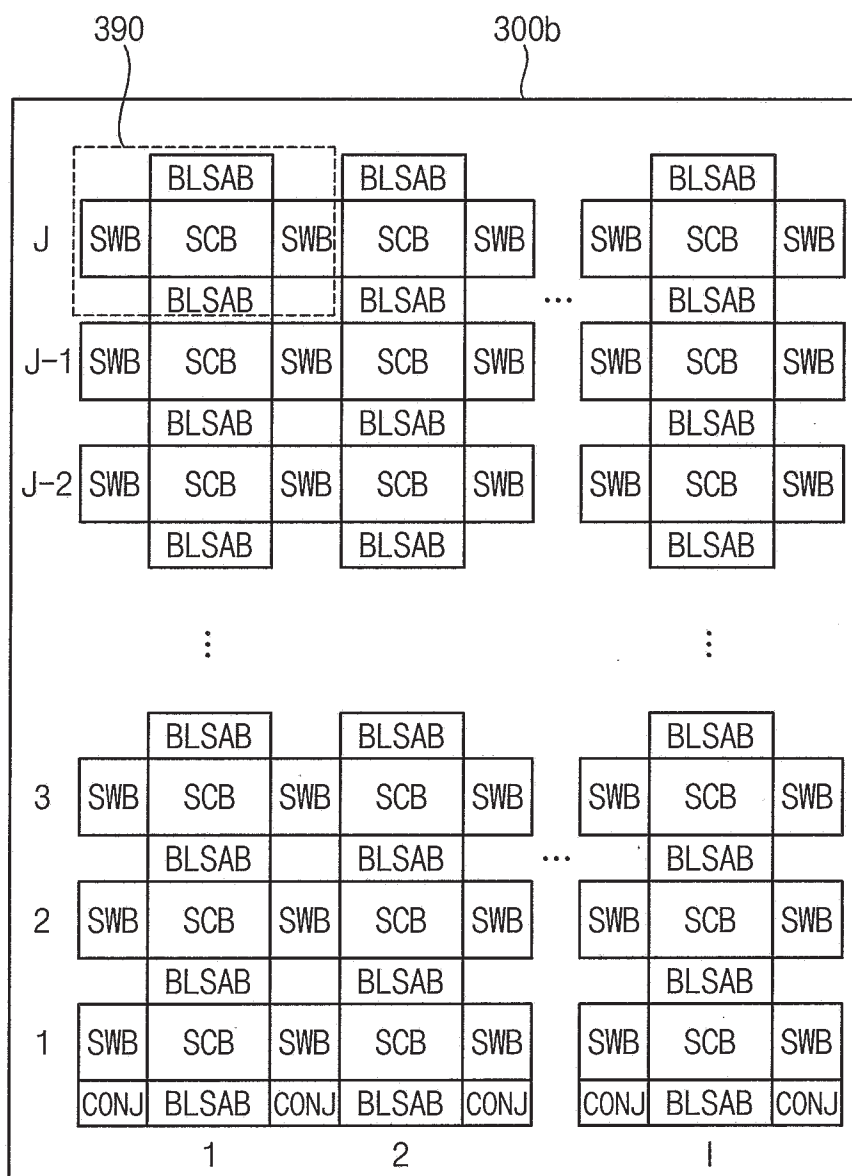


FIG. 23

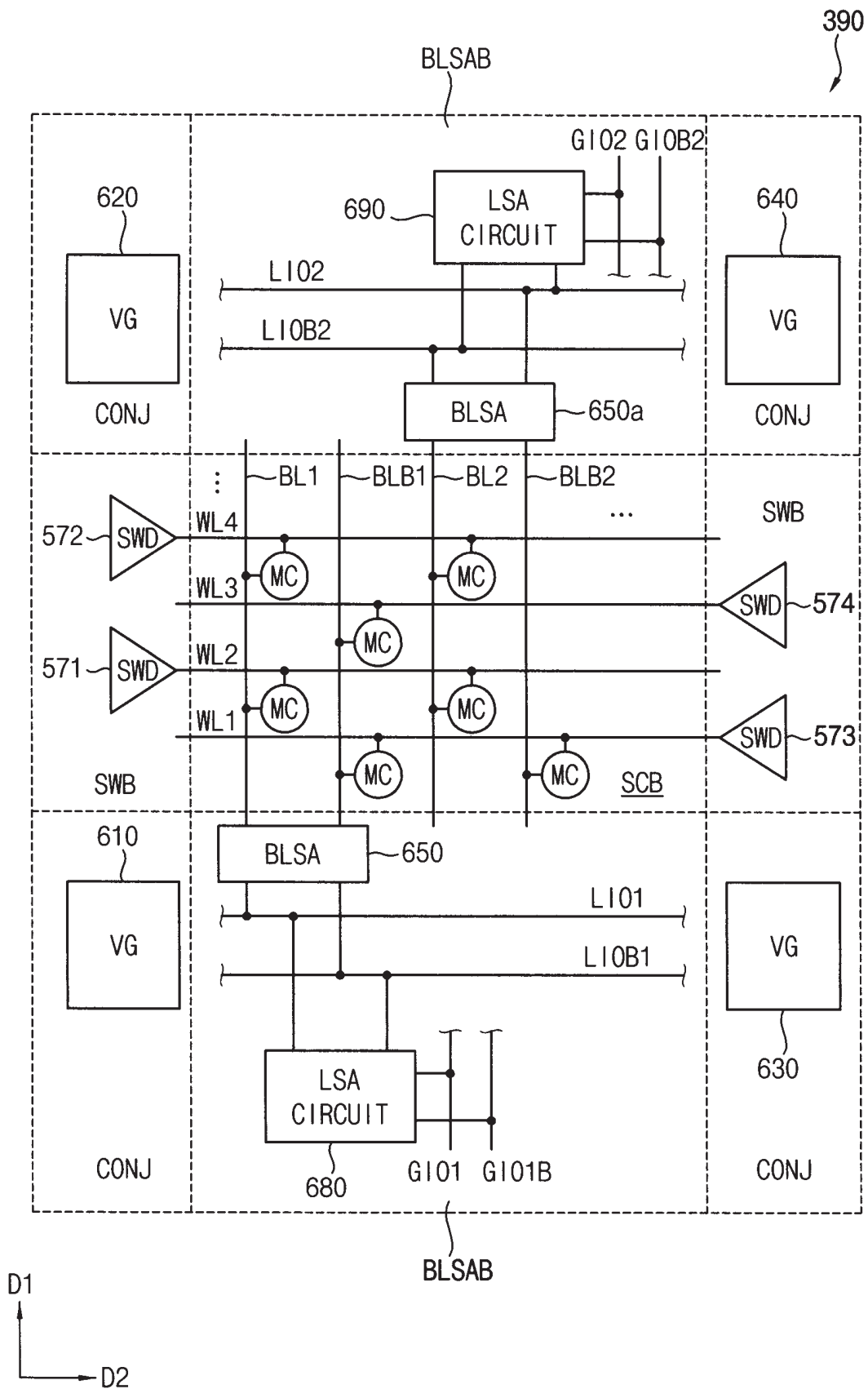


FIG. 24

650

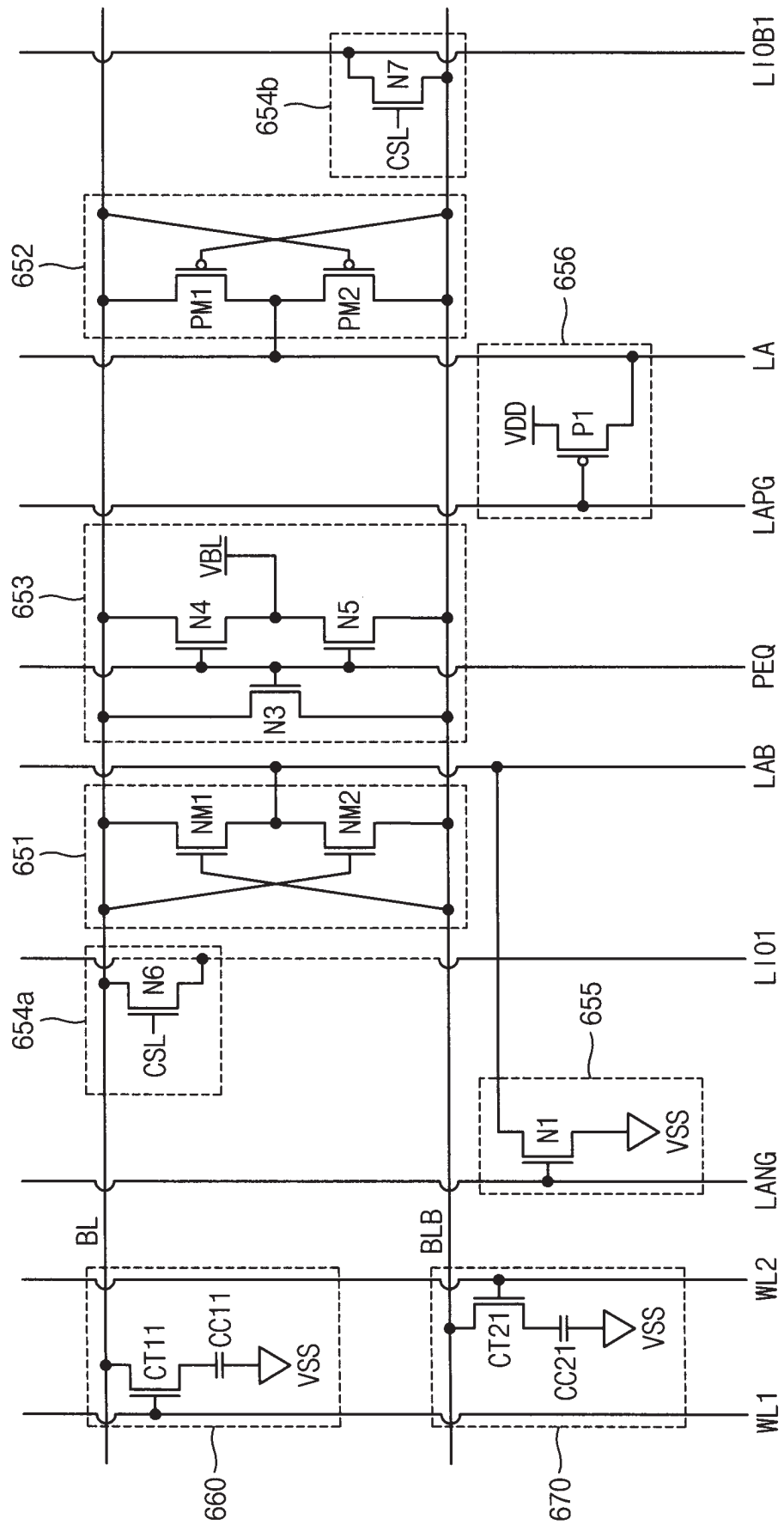


FIG. 25

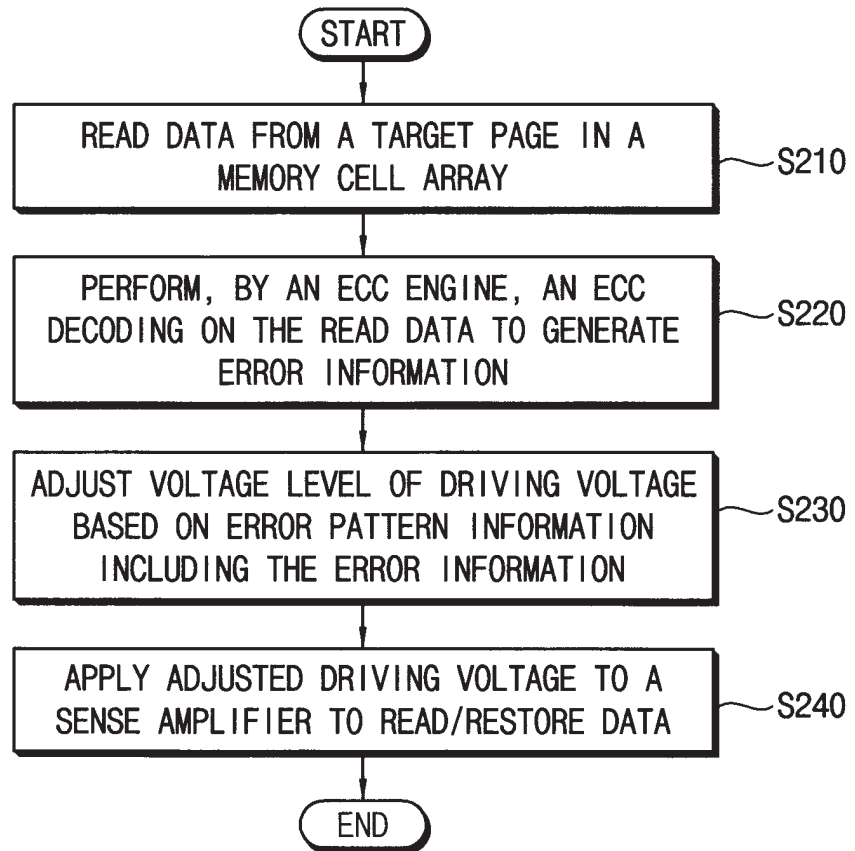


FIG. 26

