WHAT IS CLAIMED IS:

1. A method of fabricating a microelectronic assembly including a built-in TEC and a microelectronic device coupled to the TEC, the method comprising:

providing the microelectronic device;

fabricating the TEC directly onto the microelectronic device such that there is no mounting material between the TEC and the microelectronic device.

2. The method of claim 1, wherein the TEC comprises at least one couple including an N-type electrode, a P-type electrode, a plurality of conductive elements electrically coupling the N-type electrode and P-type electrode of the couple to one another, and a patterned electrical insulator layer between respective ones of the conductive elements, respective ones of the N-type electrodes and respective ones of the P-type electrodes.

3. The method of claim 2, wherein fabricating the TEC comprises:

providing a plurality of first conductive elements directly on the microelectronic device;

providing a plurality of N-type electrodes each electrically coupled to a corresponding one of the first conductive elements;

providing a plurality of P-type electrodes each P-type electrode electrically coupled to a corresponding one of the first conductive elements, an N-type electrode and a P-type electrode coupled to each given one of the first conductive elements together forming a pair of N-type and P-type electrodes;

providing a patterned electrical insulator layer between respective ones of the first conductive elements, respective ones of the N-type electrodes and respective ones of the P-type electrodes; and

providing a plurality of second conductive elements such that each of the second conductive elements is adapted to allow electrical current to flow in series through respective pairs of N-type and P-type electrodes.

4. The method of claim 3, wherein providing a plurality of first conductive elements comprises:

providing a first conductive layer directly on the microelectronic device; and

providing an interconnect pattern in the first conductive layer to yield the plurality of first conductive elements.

5. The method of claim 4, wherein providing a first conductive layer comprises depositing the first conductive layer using one of plating, sputtering and evaporation.

6. The method of claim 4, wherein providing the interconnect pattern comprises using lithography.

7. The method of claim 3, wherein providing a plurality of N-type electrodes comprises:

providing an N-type layer of TE material on the first patterned metallization layer; and

providing an electrode pattern in the N-type layer to yield the plurality of N-type electrodes.

8. The method of claim 7, wherein providing an N-type layer of TE material comprises using one of CVD or PVD deposition of a TE material precursor.

9. The method of claim 7, wherein the TE material precursor is implanted with dopants prior to deposition thereof.

10. The method of claim 7, further comprising implanting the TE material after deposition thereof.

11. The method of claim 7, wherein providing an electrode pattern in the N-type layer comprises using lithography.

12. The method of claim 3, wherein providing a patterned electrical insulator layer comprises:

providing an electrical insulator layer on the N-type electrodes and on the first conductive elements; and

providing an electrode pattern in the electrical insulator layer to define vias therein, the electrode pattern corresponding to a pattern of P-type electrodes to be provided as part of the TEC .

13. The method of claim 12, wherein providing the electrical insulator layer comprises using one of CVD deposition of a Teox precursor and spin deposition of a flowable oxide precursor.

14. The method of claim 12, wherein providing the electrode pattern comprises using lithography.

15. The method of claim 12, wherein providing the plurality of P-type electrodes comprises:

providing a plurality of P-type legs of TE material in vias defined in the electrical insulator layer; and

etching back the P-type legs of TE material to yield the plurality of P-type electrodes.

16. The method of claim 15, wherein providing a plurality of P-type legs comprises using one of CVD or PVD deposition of a TE material precursor.

17. The method of claim 16, wherein the TE material precursor is implanted with dopants prior to deposition thereof.

18. The method of claim 16, further comprising implanting the TE material after deposition thereof.

19. The method of claim 3, wherein providing a plurality of second conductive elements comprises:

providing a second conductive layer on the N-type electrodes and P-type electrodes; and

providing an interconnect pattern in the second conductive layer to yield the plurality of second conductive elements.

20. The method of claim 19, wherein providing a second conductive layer comprises depositing the second conductive layer using one of plating, sputtering and evaporation.

21. The method of claim 19, wherein providing the interconnect pattern comprises using lithography.

22. The method of claim 1, wherein providing a microelectronic device comprises providing a die having an oxide layer on a side thereof adapted to be coupled to the TEC.

23. A microelectronic assembly comprising:

a microelectronic device; and

a TEC coupled to the microelectronic device such that there is no mounting material between the TEC and the microelectronic device.

24. The microelectronic assembly of claim 23, wherein the TEC comprises at least one couple including an N-type electrode, a P-type electrode, a plurality of conductive elements electrically coupling the N-type electrode and P-type electrode of the couple to one another, and a patterned electrical insulator layer between respective ones of the conductive elements, respective ones of the N-type electrodes and respective ones of the P-type electrodes.

25. The microelectronic assembly of claim 23, wherein the microelectronic device includes an oxide layer on a side thereof adapted to be coupled to the TEC.

26. A system comprising:

a microelectronic assembly including:

a microelectronic device; and

a TEC coupled to the microelectronic device such that there is no mounting material between the TEC and the microelectronic device; and

a graphics processor coupled to the microelectronic assembly.

27. The system of claim 26, wherein the TEC comprises at least one couple including an N-type electrode, a P-type electrode, a plurality of conductive elements electrically coupling the N-type electrode and P-type electrode of the couple to one another, and a patterned electrical insulator layer between respective ones of the conductive elements, respective ones of the N-type electrodes and respective ones of the P-type electrodes.

28. A microelectronic arrangement comprising:

a microelectronic assembly including:

a microelectronic device; and

a TEC coupled to the microelectronic device such that there is no mounting material between the TEC and the microelectronic device; and

an electrical circuit electrically connected to the TEC and including a power source adapted to supply current to the TEC.

29. The arrangement of claim 28, wherein the TEC comprises at least one couple including an N-type electrode, a P-type electrode, a plurality of conductive elements electrically coupling the N-type electrode and P-type electrode of the couple to one another, and a patterned electrical insulator layer between respective ones of the conductive elements, respective ones of the N-type electrodes and respective ones of the P-type electrodes.

30. The arrangement of claim 28, further comprising a feedback control loop coupled to the microelectronic device, to the TEC and to the electrical circuit to control an extent of cooling provided by the TEC as a function of a temperature of the microelectronic device.

What is claimed is:

1. A method of fabricating a microelectronic assembly including a built-in thermoelectric cooler (TEC) and a microelectronic device coupled to the built-in TEC, the method comprising:

providing the microelectronic device; fabricating the built-in TEC directly onto the microelectronic device such that there is no mounting material between the built-in TEC and the microelectronic device;

wherein fabricating the built-in TEC comprises:

initially forming a plurality of first conductive elements of the built-in TEC directly onto the microelectronic device;

subsequently forming a first conductivity type layer of TE material on the plurality of first conductive elements;

forming an electrode patterned in the first conductivity type layer to yield a plurality of first conductivity type electrodes;

depositing an electrical insulator layer between the first conductivity type electrodes and between the first conductive elements;

forming an electrode pattern in the electrical insulator layer to define vias therein;

forming a plurality of second conductivity type legs of TE material in the vias defined in the electrical insulator layer; and

etching back the second conductivity type legs to yield a plurality of second conductivity type electrodes.

2. The method of claim 1, wherein forming said plurality of first conductive elements comprises:

providing a first conductive layer directly on the microelectronic device; and

providing an interconnect pattern in the first conductive layer to yield the plurality of first conductive elements.

3. The method of claim 2, wherein providing a first conductive layer comprises depositing the first conductive layer using one of plating, sputtering and evaporation.

4. The method of claim 1, wherein the first conductivity type layer of TE material is implanted with dopants.

5. The method of claim 1, wherein providing the electrical insulator layer comprises using one of CVD deposition of a TEOS precursor and spin deposition of a flowable oxide precursor.

6. The method of claim 1, wherein providing a plurality of second conductivity type legs comprises using one of CVD or PVD deposition of a TE material precursor.

7. The method of claim 6, wherein the second conductivity type TE material precursor is implanted with dopants prior to deposition thereof.

8. The method of claim 6, further comprising implanting the second conductivity type TE material after deposition.

9. The method of claim 1, further comprising:

providing a plurality of second conductive elements comprises:

providing a second conductive layer on the first conductivity type electrodes and second conductivity type electrodes; and

providing an interconnect pattern in the second conductive layer to yield the plurality of second conductive elements.

10. The method of claim 9, wherein providing a second conductive layer comprises depositing the second conductive layer using one of plating, sputtering and evaporation.

11. The method of claim 1, wherein providing a microelectronic device comprises providing a die having an oxide layer on a side thereof adapted to be coupled to the TEC.

12. The method of claim 11, wherein the built-in TEC is fabricated directly onto the oxide layer of the die.

13. The method of claim 12, wherein forming said plurality of first conductive elements comprises:

depositing a first conductive layer directly onto the oxide layer of the die during fabrication of the built-in TEC.