PHOTONICS STRUCTURE WITH INTEGRATED LASER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority of U.S. Provisional Application No. 62/770,623 filed November 21, 2018, titled "Photonics Structure with Integrated Laser", which is incorporated by reference herein in its entirety. This application claims the benefit of priority of U.S. Non-Provisional Application No. 16/575,820, filed September 19, 2019, titled "Photonics Structure with Integrated Laser", which is incorporated by reference herein in its entirety. This application claims the benefit of priority of Taiwan Application No. 108133747, filed September 19, 2019, titled "Photonics Structure with Integrated Laser", which is incorporated by referenced herein in its entirety. The aforementioned U.S. Non-Provisional Application No. 16/575,820, filed September 19, 2019, titled "Photonics Structure with Integrated Laser", which is incorporated by reference herein in its entirety, claims the benefit of priority of U.S. Provisional Application No. 62/770,623 filed November 21, 2018, titled "Photonics Structure with Integrated Laser", which is incorporated by reference herein in its entirety. The aforementioned Taiwan Application No. 108133747, filed September 19, 2019, titled "Photonics Structure with Integrated Laser", which is incorporated by referenced herein in its entirety, claims the benefit of priority of U.S. Provisional Application No. 62/770,623 filed November 21, 2018, titled "Photonics Structure with Integrated Laser", which is incorporated by reference herein in its entirety.

GOVERNMENT RIGHTS STATEMENT

[0002] This invention was made with government support under grant contract number FA8650-15-2-5220 ARPA-E, DE-AR0000672, and DARPA DODOS HR0011-15-C-0055. The government may have certain rights in the invention.

FIELD

[0003] The present disclosure relates to photonics generally and specifically to fabricating of photonics structures.

BACKGROUND

[0004] Commercially available photonics integrated circuits are fabricated on wafers, such as bulk silicon or silicon-on-insulator wafers.

[0005] In one aspect photonics integrated circuits can include waveguides for transmission of optical signals between different areas of a photonics integrated circuit chip as well as on and off the chip. Commercially available waveguides are of rectangular or ridge geometry and are fabricated in silicon (single or polycrystalline) or silicon nitride.

[0006] Commercially available photonics integrated circuits can include photodetectors and other optical components. Photonics integrated circuits rely on the emission, modulation and the detection of light in the communication band (about 1.3 μm to about 1.55 μm). A bandgap absorption edge in

germanium is near 1.58 μm. Germanium has been observed to provide sufficient photo-response for optoelectronic applications using 1.3 μm and 1.55 μm carrier wavelengths.

[0007] Commercially available photonics integrated circuit chips are available on systems having a photonics integrated circuit chip disposed on a printed circuit board.

BRIEF DESCRIPTION

[0008] The shortcomings of the prior art are overcome, and additional advantages are provided, through the provision, in one aspect, of a photonics structure.

[0009] There is set forth herein a structure including: a substrate; a dielectric stack disposed on the substrate; one or more photonics device integrated in the dielectric stack; and a laser light source having a laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are integrated in the dielectric stack, wherein the laser stack includes an active region configured to emit light in response to the application of electrical energy to the laser stack.

[0010] There is set forth herein a method including: patterning a waveguide in a silicon layer of a silicon on insulator (SOI) wafer of a photonics structure having a dielectric stack defined by an insulator of the SOI wafer; forming in the photonics structure a trench extending through dielectric layers of the dielectric stack; and epitaxially growing a laser stack within the trench, the laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are disposed within the dielectric stack and include an active region configured to emit light in response to the application of electrical energy to the laser stack.

[0011] Additional features and advantages are realized through the techniques of the present disclosure.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0012] One or more aspects of the present disclosure are particularly pointed out and distinctly claimed as examples in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the disclosure are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0013] Fig. 1 is a cutaway side view of an optoelectronics system; and

[0014] Figs. 2A-2I are fabrication stage views illustrating a method for fabrication of the optoelectronics system as shown in Fig. 1 according to one embodiment;

[0015] Fig. 3 is a cutaway side view of an optoelectronics system according to one embodiment;

[0016] Figs. 4A-4B are fabrication stage views illustrating a method for fabrication of the optoelectronics system according to Fig. 3;

[0017] Figs. 5A-5D are fabrication stage views in a Z-Y plane illustrating photonics structures fabricated for coupling light from an active region of a laser stack into one or more waveguide;

[0018] Fig. 5E is a top view of first and second evanescently coupled waveguides in a Y-X plane.

DETAILED DESCRIPTION

[0019] Aspects of the present disclosure and certain features, advantages, and details thereof, are explained more fully below with reference to the non-limiting examples illustrated in the accompanying drawings. Descriptions of well-known materials, fabrication tools, processing techniques, etc., are omitted so as not to unnecessarily obscure the disclosure in detail. It should be understood, however, that the detailed description and the specific examples, while indicating aspects of the disclosure, are given by way of illustration only, and not by way of limitation. Various substitutions, modifications, additions, and/or arrangements, within the spirit and/or scope of the underlying inventive concepts will be apparent to those skilled in the art from this disclosure.

[0020] Fig. 1 illustrates photonics structure 10 having a photonics dielectric stack 200, in which there can be integrally formed and fabricated one or more photonics device, such as one or more photonics device integrally formed and fabricated within photonics dielectric stack 200, and one or more laser light source having a laser stack integrally formed and fabricated within dielectric stack 200.

[0021] One or more photonics device integrally formed and fabricated within dielectric stack 200 can include, e.g. waveguide 402 provided by a silicon (Si) ridge waveguide and can include waveguide 404 provided by a silicon rectangular waveguide. Waveguide 411 provided by a rectangular silicon nitride waveguide, waveguide 412 provided by a rectangular silicon nitride waveguide, waveguide 421 provided by a rectangular silicon waveguide, and waveguide 422 provided by a rectangular silicon nitride waveguide.

[0022] Photonics structure 10 can have integrated therein other types of waveguides integrally formed and fabricated within dielectric stack 200. Photonics structure 10 can include integrally formed and fabricated within dielectric stack 200, e.g. a photodetector 406 having waveguiding material formation 401, light sensitive material formation 407, upper contact C1, and lower contact C2.

[0023] Photonics structure 10 can include integrally formed and fabricated within dielectric stack 200, modulator 408 having waveguiding material formation 403, contact C3, and contact C4. Photonics structure 10 can include integrally formed and fabricated within dielectric stack 200 other types of photonics devices, e.g. one or more grating, one or more polarizer, and/or one or more resonator. In the described embodiment set forth in reference to Fig. 1, waveguides integrally formed and fabricated within dielectric stack 200 can be, e.g. single crystalline silicon waveguides or

waveguides formed of nitride, e.g. SiN, polycrystalline silicon waveguides, amorphous silicon waveguides, and/or silicon nitride or silicon oxynitride waveguides.

[0024] According to one embodiment, photonics structure 10 can be fabricated using silicon on insulator (SOI) wafer. Referring to Fig. 1, substrate 100 can be a substrate of an SOI wafer, layer 202 can be an insulator layer of an SOI wafer, and layer 302 can be a silicon layer of an SOI wafer. Layer 302 can have patterned therein waveguiding formation 401, ridge waveguide 402, waveguiding material formation 403 (defining modulator 408), and waveguide 404. Substrate 100 can have a bottom elevation at elevation 2000. Substrate 100 according to one embodiment can have a thickness in a range of from about 10um to about 1000um. Substrate 100 according to one embodiment can have a thickness in a range of from about 100um to about 1000um. Layer 202 according to one embodiment can have a thickness of from about 100nm to about 10um. Layer 202 according to one embodiment can have a thickness of from about 1um to about 5um. Layer 302 according to one embodiment can have a thickness of from about 10nm to about 1000nm. Layer 302 according to one embodiment can be formed of monocrystalline silicon.

[0025] Photonics structure 10 can have integrally formed and fabricated therein integrated laser light sources 500. Each integrated laser light source can include a laser stack 510 defined by buffer material formation 502, contact layer 505, aluminum tuning layer 511A, cladding layer 512A, aluminum tuning layer 513A, spacer layer 514, active region 515, patterned layer 516, aluminum tuning layer 513B, cladding layer 512B, aluminum tuning layer 511B, and contact layer 506. According to one embodiment, each successive layer of laser stack 510 can be deposited on a preceding layer. The depositing of each layer on a preceding layer can be performed by epitaxially growing the layer on a preceding layer.

[0026] Each integrated laser light source 500 can also include a dielectric liner 503 defined by a layer, one or more lower contacts (C5 and C6) for the integrated at location A, C8 and C9 for the integrated laser light source 500 at location B, and C11 an C12 for the integrated laser light source 500 at location C. Each integrated laser light source 500 can include an upper contact (C7 for integrated laser light source 500 at location A, C10 for integrated laser light source 500 at location B, and C13 for integrated laser light source 500 at location C).

[0027] Photonics structure 10 can further have formed and fabricated therein one or more metallization layer and one or more vias layer. Integrated photonics structure 10 as shown in Fig. 1 can include metallization layer 602 that can be patterned to define metallization formations M1, vias layer 702 can be patterned to define vias V1, and metallization layer 612 can be patterned to define metallization layer formations M2. Metallization layers 602 and 612 can define horizontally extending wires. Wires defined by metallization layers 602 and 612 can be horizontally extending through areas of photonics dielectric stack 200.

[0028] Horizontally extending wires defined by metallization layer 602 can be electrically connected to one or more vertically extending contact conductive material formations C1-C12 and vias V1

defined by vias layer 702 for distribution of one or more of control logic and/or power signals vertically and horizontally to different areas of photonics dielectric stack 200. Horizontally extending wires defined by metallization layer 612 can be electrically connected to one or more of vertically extending vias V1 defined by vias layer 702 for distribution of one or more electrical control logic and/or power signals vertically and horizontally between different areas of photonics dielectric stack 200.

[0029] Photonics structure 10 can include one or more photonics devices, e.g. one or more waveguides in the foreground and/or background (extending out of and/or into the paper of the drawing representation of Fig. 1) of laser light sources 500 can be aligned with respective active regions 515 of integrated laser light sources 500 at locations A, B, and C, as described further in connection with Figs. 5A-5E herein. Photonics structure 10 can include, e.g. tens, hundreds, or thousands of photonics devices and/or integrated laser light sources 500 of which representative photonics devices and integrated laser light sources 500 are described in reference to Fig. 1.

[0030] Photonics structure 10 as shown in Fig. 1 according to one embodiment can refer to a wafer based photonics structure, prior to dicing to define integrated circuit chips. Photonics structure 10 according to one embodiment refers to an entire wafer based structure.

[0031] Photonics structure 10 as shown in Fig. 1 according to one embodiment can refer to a photonics integrated circuit chip formed by fabrication processing that includes dicing of a photonics wafer based structure. Photonics structure 10 according to one embodiment can refer to photonics structure integrated circuit chip defined by dicing of an entire wafer based structure.

[0032] Providing photonics structure 10 so that active region 515 of an integrated laser light source 500 is integrally formed and fabricated within dielectric stack 200 along with a waveguide into which the active region 515 emits light can facilitate precision alignment of an active region of an integrated laser light source 500 and a waveguide. Active regions 515 can emit light into such aligned waveguides in the foreground and/or in the background of integrated laser light sources 500. Integrally fabricating photonics devices and laser light sources on a common photonics structure, so that a photonics device in an active region of an integrated laser light source are commonly fabricated and disposed within a common dielectric stack facilitates precision alignment between such photonics device and integrated laser light source 500 and alleviates a need for packaging technologies for facilitation of alignment.

[0033] Photonics structure 10 can include one or more termination 6002 formed on metallization layer 612. Termination 6002 can include, e.g., one or more of (a) an opening formed in dielectric stack 200 opening to metallization layer 612; (b) a pad formed on metallization layer 612 and an opening to the pad; (c) an under bump metallization (UBM) layer formed on the metallization layer 612 with an opening formed in dielectric stack 200 to the UBM; (d) a UBM formed on metallization layer 612 and a solder bump formed on the UBM externally protruding from dielectric stack 200.

[0034] A method for fabrication of photonics structure 10 is described with reference to the fabrication stage views of Figs. 2A-2J. In Fig. 2A there is illustrated an intermediary stage view of photonics structure 10. Photonics structure 10 according to one embodiment can be fabricated using a SOI wafer having a substrate 100 formed of silicon (Si), insulator layer 202, and silicon layer 302. Within layer 302 there can be patterned waveguiding material formation 401 defining photodetector 406, waveguide 402 provided by a ridge waveguide, waveguiding material formation 403 defining a modulator, and waveguide 404 provided by a rectangular waveguide. On the patterning of formations 401-404 a layer of dielectric material, e.g. SiO_2 can be deposited over the formations 401-404 and can be subject to chemical mechanical planarization (CMP) so that a horizontal plane is defined at elevation 2020. In each instance herein where there is described CMP, the CMP can be accompanied by chemical mechanical polishing so that an atomically smooth surface is yielded as a result of the performing CMP.

[0035] In Fig. 2B there is illustrated photonics structure 10 as shown in Fig. 2A in an intermediary stage of fabrication, after performance of further processes to define waveguide 411 and waveguide 412. Waveguides 411 and 412 can be formed of silicon nitride. For the formation of waveguides 411 and 412, layer 312 formed of silicon nitride can be deposited at an elevation 2020 and can be subject to patterning to define waveguides 411 and 412. Subsequent to the defining of waveguides 411 and 412, by patterning of layer 312, dielectric layer can be deposited over waveguides 411 and 412 and can then be subject to CMP to reduce an elevation of the formed photonics dielectric stack 200 to elevation 2022 to define a horizontally extending top surface of photonics structure 10 at elevation 2022 in the intermediary stage of fabrication shown partially defined by dielectric material, e.g. SiO2, and waveguides 411 and 412.

[0036] In Fig. 2C there is shown photonics structure 10 as depicted in Fig. 2B in an intermediary stage of fabrication after further patterning to define waveguide 421 and waveguide 422. For the fabrication of waveguides 421 and 422 formed of nitride a dielectric layer can be deposited on the planar horizontal surface extending in elevation 2022 followed by a further CMP process to define a horizontal plane extending at elevation 2023. At elevation 2023 layer 322 can be deposited and then subjected to patterning to define waveguides 421 and 422. Layer 322 can be subject to CMP prior to the defining of sidewalls of waveguides 421 and 422. On the patterning of waveguides 421 and 422, a layer of dielectric material can be deposited over waveguides and can then be subject to CMP to define a horizontally extending planar surface at elevation 2024. An additional layer of dielectric material can be deposited on the horizontally extending planar surface at elevation 2024 and can be subject to CMP to define a horizontally extending planar surface at elevation 2025.

[0037] Fig. 2D illustrates photonics structure 10 as shown in Fig. 2C in an intermediary stage of fabrication after further patterning to define light sensitive material formation 407, defining photodetector 406. For the providing of light sensitive material formation 407 a plurality of layers of germanium can be epitaxially grown and annealed in a trench that can be formed between vertically

extending plane 7001 and vertically extending plane 7003 formed by reactive ion etching (RIE). The formed trench can include vertically extending center axis 7002. The formed trench at the range of elevations depicted can include a perimeter intersecting vertically extending plane 7001 and vertically extending plane 7003. In one embodiment germanium can be selectively grown using reduced pressure chemical vapor deposition (RPCVD). Multiple epitaxially growing and annealing stages can be used for the formation of light sensitive material formation 407. Multiple depositing and annealing cycles, light sensitive material formation 407, e.g. formed of germanium can initially overflow the defined trench and then can be subject to CMP so that a planar horizontal surface is defined at elevation 2025.

[0038] Fig. 2E illustrates photonics structure 10 as shown in Fig. 2D in an intermediary stage of fabrication after additional processing to increase an elevation of photonics dielectric stack 200. As shown in Fig. 2E subsequent to the formation of light sensitive material formation 407, an additional layer of dielectric material, e.g., SiO2 can be deposited and then subject to CMP to define a horizontal planar top surface of photonics dielectric stack 200 at elevation 2030 as shown in the intermediary fabrication stage view of Fig. 2E.

[0039] In Fig. 2F there is shown photonics structure 10 as shown in Fig. 2E in an intermediary stage of fabrication after initial fabrication to define buffer material formations 502 defining laser stacks 510 and integrated laser light sources 500. For providing buffer material formations 502 generally at locations A, B, and C respectively, first, second, and third trenches can be generated at locations A, B, and C.

[0040] A first trench can have a vertically extending center axis 7012 and can include sidewalls within photonics dielectric stack 200 intersecting vertically extending plane 7011 and vertically extending plane 7013. A second trench can have a vertically extending center axis 7022 and can have vertically extending sidewalls intersecting vertically extending plane 7021 and vertically extending plane 7023. A third trench can have a vertically extending center axis 7032 and can have sidewalls intersecting vertically extending plane 7031 and vertically extending plane 7033. The formed first, second, and third trenches can extend from bottom elevation 2002 to top elevation 2030.

[0041] The formation of each of the first, second, and third trenches generally at locations A, B, and C can include a two stage RIE process. In a first RIE stage wherein material can be etched to elevation 2010 etching can be performed that is selective to oxide so that oxide material defining photonics dielectric stack 200 is removed without removal of silicon defining substrate 100 in the described embodiment. In a second RIE stage etching can be performed selective to silicon so that material of substrate 100 is removed without removal of oxide defining photonics dielectric stack 200.

[0042] With the trenches formed having respective vertically extending center axes 7012, 7022, and 7032 a layer 503 formed of dielectric material and providing a dielectric liner can be deposited. Layer 503 can initially have a sacrificial portion that extends the respective bottoms of the formed trenches having center axes 7012, 7022, and 7032. That is, layer 503 of each integrated laser light source 500

can initially have bottom elevations adjacent to and formed on material of substrate 100 formed of silicon at elevation 2010.

[0043] Buffer material formation 502 can be epitaxially grown on silicon defining substrate 100. For epitaxially growing an initial layer of material defining buffer material formation 502, material of layer 503 can be removed from a bottom of the respective trenches associated to axes 7012 and 7022, and 7032 to expose the silicon surface of substrate 100 at elevation 2002. For removal of material of layer 503 at the bottom of the respective trenches, a punch through RIE process can be used that is selective to dielectric material, e.g. SiO_2 forming layer 503 so that dielectric material of layer 503 is removed without removal of silicon that forms substrate 100.

[0044] Buffer material formation 502 can be grown using a multistage growing and annealing process, wherein layers forming buffer material formation 502 can be epitaxially grown and then annealed. Material that can be epitaxially grown to form buffer material formation 502 include III-V material, e.g. gallium arsenide or gallium phosphide. Prior to the growing of an initial layer of III-V material, a bottom surface of trenches associated with center axes 7012 and 7022, and 7032 can be subject to further treatment, e.g. treatment to clean RIE products and/or treatment to epitaxially grow a thin layer of silicon, e.g. monocrystalline silicon on the silicon surface (monocrystalline defining a bottom of the trenches associated with center axes 7012 and 7022, and 7032). Multiple epitaxially growing and annealing stages can be used for the providing of buffer material formations 502. Embodiments herein recognize that when III-V material is epitaxially grown on a silicon surface defining a bottom of the trench, there will be a lattice mismatch which can induce defects. Annealing stages can be used to annihilate defects.

[0045] Growing and annealing of III-V material to provide buffer material formations 502 can be performed using a restricted thermal budget. Employing a restricted thermal budget for the fabrication of buffer material formations 502 can mitigate thermal degradation of photonics devices, such as photonics devices and components 401-406, 411-412, and 421-422. According to one embodiment, epitaxially growing stages for epitaxially growing layers forming buffer material formations 502 can be performed at a temperature of between about 400°C and about 600°C, whereas annealing stages for annealing of defined sublayers of buffer material formations 502 can be performed at temperatures of from between about 500°C and about 700°C.

[0046] Buffer material formation 502 can be formed of, e.g. gallium arsenide (GaAs) deposited with multiple epitaxially growing and annealing cycles, with annealing cycles being performed for removal of defects to provide a low defect density of buffer material formation 502. Buffer material formation 502 can include a thickness, e.g. in the range of from about 1000nm to about 4000nm according to one embodiment. Buffer material formation 502 according to one embodiment can be formed primarily of gallium arsenide (GaAs). According to one embodiment, buffer material formation 502 can include a gallium arsenide (GaAs)/indium gallium arsenide (InGaAs) strained superlattice (SSL). An SSL can be included in buffer material formation 502 to mitigate treading location defect (TDD)

propagation to active region 515. The SSL can also reduce surface roughness. Buffer material formation 502 according to one embodiment, can include a specialized bottom layer e.g. deposited on, e.g. directly on a silicon surface of substrate 100. The specialized bottom layer can include e.g. GaP/Si or GoVS (001) and can mitigate anti- phase domain defects (APDs).

[0047] With further reference to the stage view of Fig. 2F, each buffer material formation 502 on being grown to an elevation exceeding elevation 2010 depicted as a top elevation of substrate 100 can be subject to treatment to define a planar horizontal surface at about elevation 2010. At locations A and B, contact layer 505 can be deposited on a top surface of buffer material formation 502. Contact layer 505 can include, e.g. gallium arsenide (GaAs) doped with an N type dopant, e.g. silicon (Si). Contact layer 505 can include a thickness in the range of from about 100nm to about 500nm.

[0048] At location C, buffer material formation 502 can be absent of an associated deposited contact layer deposited thereon as in locations A and B. Subsequent to the formation of contact layer 505 by the process of ion implantation at locations A and B, the trenches associated with vertically extending center axes 7012 and 7022, and 7032 can be filled with oxide. Oxide can be deposited within the various trenches associated to center axes 7012 and 7022, and 7032 and can overfill the trenches. Photonics structure 10 can then be subject to CMP to reduce a top elevation of photonics dielectric stack 200 so that a planar and horizontally extending surface is defined at elevation 2030.

[0049] Buffer material formation 502 can provide a defect reduced interface for growing of remaining structures of laser stack 510. A laser stack 510 can include in addition to buffer material formation 502, contact layer 505, aluminum tuning layer 511A, cladding layer 512A, aluminum tuning layer 513A, spacer layer 514, active region 515, patterned layer 516, aluminum tuning layer 513B, cladding layer 512B, aluminum tuning layer 511B, and contact layer 506. Active region 515 can include quantum dots. In some embodiments buffer material formation 502 can be sacrificially formed, i.e. fabricated and then removed prior to fabricating of photonics structure 10 in its final form, e.g. as a photonics integrated circuit chip.

[0050] Fig. 2G illustrates photonics structure 10 as shown in Fig. 2F in an intermediary stage of fabrication after performance of further processes to grow additional layers of respective laser stacks 510 generally at locations A, B, and C.

[0051] For growing of additional layers of laser stacks 510, stack trenches can be formed in photonics dielectric stack 200. Referring to Fig. 2G a first trench generally at location A can be formed having vertically extending center axis 7042 and sidewalls intersecting vertically extending planes 7041 and 7043. A second trench formed generally at location B can be formed having vertically extending center axis 7052 and sidewalls intersecting vertically extending planes 7051 and 7053. A third trench formed generally at location C can be formed having vertically extending center axis 7062 and sidewalls intersecting vertically extending planes 7061 and 7063. The first and second laser stack trenches can extend downward to have bottom surfaces defined by contact layer 505

formed of conductive material. The laser stack trench at location C can extend downward to have a bottom surface defined by a top surface of buffer material formation 502 at location C.

[0052] Referring to Fig. 2G aluminum tuning layer 511A can be deposited within each trench at location A, B, and C followed by cladding layer 512A which can be deposited on aluminum tuning layer 511A. At location A and B the aluminum tuning layer 511A can be epitaxially grown on contact layer 505. At location C, aluminum tuning layer 511A can be epitaxially grown on buffer material formation 502. With cladding layer 512A formed, aluminum tuning layer 511A of each laser stack 510 can be deposited by epitaxially growing of aluminum tuning layer 511A on cladding layer 512A.

[0053] Aluminum tuning layer 511A can be formed of a plurality of sublayers, each sublayer having a different index of a refraction. The different sublayers of aluminum tuning layer 511A can have different concentrations of aluminum. The different concentrations of aluminum can result in different indices of refraction. The concentrations of aluminum can transition from about 40% aluminum at distances farthest away from active region 515 to concentrations of about 0% aluminum at locations of aluminum tuning layer in closest proximity to active region 515. The index of refraction of aluminum tuning layer 511A can increase at distances closer to active region 515 which can reduce concentration of aluminum (Al).

[0054] Cladding layer 512A provide light confinement and also separates the active region 515 and the contact layer 505. Cladding layer 512A can be formed of, e.g. aluminum gallium arsenide (AlGaAs) having a fixed concentration of aluminum, e.g. 40% aluminum concentration. Cladding layer 512A according to one embodiment can include a thickness in the range of from about 500nm to about 2000nm.

[0055] With cladding layer 512A formed, aluminum tuning layer 513A can be epitaxially grown on cladding layer 512A. During the growth of the tuning layer 513A, the aluminum content of this region is adjusted to enable a transition from about 40% aluminum at the interface of layer 512A to 0% at the junction between 513A and the spacer layer 514. The thickness of 513A ranges from 50nm to 100nm.

[0056] Cladding layer 512A and aluminum tuning layers 511A and 513A can function to confine light and can mitigate light interaction with lossy contact layer 505.

[0057] At the laser stack trenches of locations A, B, and C, spacer layer 514 can be epitaxially grown on the top surface of aluminum tuning layer 513A, followed by active region 515 which can be epitaxially grown on spacer layer 514 and patterned layer 516 which can be epitaxially grown on active region 515. Spacer layer 514 can be formed, e.g. of gallium arsenide (GaAs) and can have a thickness in the range of from about e.g. 200nm to about 700nm. Patterned layer 516 can have a thickness in a range of from about e.g. 200nm to about 1000nm.

[0058] Active region 515 can be defined by a layer that includes multiple sublayers, e.g. including from about 3 to about 9 sublayers formed of indium gallium arsenide (InGaAs) and defining quantum dots and from about 3 to 9 sublayers of gallium arsenide (GaAs). The respective thin layers (e.g. about 40nm) of gallium arsenide (GaAs) can separate the InGaAs layers defining quantum dots. Active region 515 can include N repeats of the following layers: {indium gallium arsenide (InGaAs) embedded quantum dots/ indium gallium arsenide (InGaAs)/gallium arsenide (GaAs)}xN wherein N can range from about 3 to about 9.

[0059] Active region 515 according to one embodiment can include a plurality, e.g. from about 3 to about 9 sublayers of epitaxially grown indium gallium arsenide (InGaAs) layers with embedded quantum dots and a gallium arsenide. Each of the sublayers can include a thickness, e.g. of about 3nm to about 50nm. According to one embodiment, each layer of quantum dots can be separated by a layer of gallium arsenide (GaAs) having a thickness of about 40nm so that active region 515 has a thickness in the range of from about 150nm to 500nm.

[0060] Patterned layer 516 can be formed e.g. of gallium arsenide (GaAs) and can be patterned for selection of the wavelength at which active region 515 operates. Patterned layer 516 can be patterned e.g. as a waveguide and/or as a grating. Patterned layer 516 according to one embodiment can have a thickness e.g. of from about 50nm to about 100nm.

[0061] Patterned layer 516 can be formed, e.g. of gallium arsenide (GaAs) and can be patterned to form a grating, e.g. double side band (DSB) grating or can be alternatively patterned to define a reflector, e.g. a distributed Bragg reflector (DBR). Patterned layer 516 can be patterned to define, e.g. a grating or reflector for use in selecting an operational band of laser stack 510. Patterned layer 516 can be patterned for selection of an operating wavelength.

[0062] For each laser stack 510 at location A, B, and C, aluminum tuning layer 513B can be epitaxially grown on patterned layer 516, cladding layer 512B can be epitaxially grown on aluminum tuning layer 513B and aluminum tuning layer 511B can be epitaxially grown on cladding layer 512B.

[0063] Aluminum tuning layer 513B can be formed of a plurality of sublayers, each sublayer having a different index of a refraction. The different sublayers of aluminum tuning layer 513B can have different concentrations of aluminum. The different concentrations of aluminum can result in different indices of refraction. The concentrations of aluminum can transition from about 40% aluminum at distances farthest away from active region 515 to concentrations of about 0% aluminum at locations of aluminum tuning layer in closest proximity to active region 515. The index of refraction of aluminum tuning layer 513B can increase at distances closer to active region 515 as a result of the reduced concentration of aluminum (Al).

[0064] Cladding layer 512B can provide light confinement and can provide spacing between aluminum tuning layer 513B and aluminum tuning layer 513A. Cladding layer 512B can be formed of, e.g. aluminum gallium arsenide (AlGaAs) having a fixed concentration of aluminum, e.g. 40%

aluminum concentration. Cladding layer 512B according to one embodiment can include a thickness in the range of from about 500nm to about 2000nm.

[0065] With cladding layer 512B formed, aluminum tuning layer 511B can be epitaxially grown on cladding layer 512B. Aluminum tuning layer 511B can be formed of a plurality of sublayers, each sublayer having a different index of a refraction. The different sublayers of aluminum tuning layer 511B can have different concentrations of aluminum. The different concentrations of aluminum can result in different indices of refraction. The concentrations of aluminum can transition from about 40% aluminum at distances farthest away from active region 515 to concentrations of about 0% aluminum at locations of aluminum tuning layer 511B in closest proximity to active region 515. The index of refraction of aluminum tuning layer 511B can increase at distances closer to active region 515 which can reduce concentration of aluminum (Al).

[0066] Cladding layer 512B and aluminum tuning layers 511B and 513B can function to confine light and can mitigate light interaction with contact layer 506 which can be a lossy contact layer.

[0067] With aluminum tuning layer 511B formed, contact layer 506 can be epitaxially grown on aluminum tuning layer 511B. Conductive material forming contact layer 506 can include e.g. gallium arsenide (GaAs) doped with e.g. Beryllium (Be), Zinc (Zn) or Carbon (C) (p-type contact). Thickness of contact layer 506 can be in a range of e.g. from about 100nm to about 500nm. Contact layer 506 can be formed of, e.g. gallium arsenide (GaAs) doped with a p type dopant, e.g. Beryllium (Be), zinc (Zn) or carbon (C). Contact layer 506 can include a thickness in the range of from about 100nm to about 500nm.

[0068] Further details of laser stack 510 according to one embodiment are set forth in reference to Table A.

Table A

Structure	Material and Process Conditions
buffer material formation 502	GaAs can be deposited with multiple epitaxially growing and annealing cycles; thickness in a range of e.g. about 1000nm to about 4000nm
contact layer 505	GaAs can be doped with Si (n type contact layer); thickness in a range of e.g. about 100nm to about 500nm
aluminum tuning layer 511A	Al(x)Ga(1-x)As can be epitaxially grown where the Al mole fraction is increased from about 0.0 to about 0.4; thickness can be in a range of e.g. about 50nm to about 100nm.
cladding layer 512A	Al(0.4)Ga(0.6)As can be epitaxially grown with thickness in a range of e.g. about 500nm to about 2000nm.
aluminum tuning layer 513A	Al(x)Ga(1-x)As can be epitaxially grown where the Al mole fraction is decreased from about 0.4 to about 0.0; thickness can be in a range of e.g. about 50nm to about 100nm.

spacer layer 514	GaAs can be epitaxially grown with thickness in a range of e.g. about 50nm to about 100nm.
active region 515	{InGaAs/InAs QDs/InGaAs/GaAs}xN can be epitaxially grown where N range from about 3 to about 9; thickness of active region 515 can be in a range of e.g. about 150nm to about 450nm, with each sublayer in the range of from about 3nm to about 50nm.
patterned layer 516	Layer formed of e.g. GaAs be patterned for selection of the wavelength at with the laser operates; thickness in a range of e.g. about 50nm to about 100nm. Patterned layer 516 can be patterned e.g. as a waveguide and/or as a grating.
aluminum tuning layer 513B	Al(x)Ga(1-x)As can be epitaxially grown where the Al mole fraction is increased from about 0.0 to about 0.4; thickness can be in a range of e.g. about 50nm to about 100nm.
cladding layer 512B	Al(0.4)Ga(0.6)As can be epitaxially grown with thickness in a range of e.g. about 500nm to about 2000nm.
aluminum tuning layer 511B	Al(x)Ga(1-x)As can be epitaxially grown where the Al mole fraction is decreased from about 0.4 to about 0.0; thickness can be in a range of e.g. about 50nm to about 100nm.
contact layer 506	GaAs can be doped with e.g. Beryllium (Be), Zinc (Zn) or Carbon (C) (p-type contact), thickness can be in a range of e.g. from about 100nm to about 500nm.

[0069] Laser stack 510 according to one embodiment can include buffer material formation 502 epitaxially grown on defined surface of substrate 100 formed of silicon, contact layer 505 epitaxially grown on buffer material formation 502, aluminum tuning layer 511A epitaxially grown on buffer material formation 502, cladding layer 512A epitaxially grown on aluminum tuning layer 511A, aluminum tuning layer 513A epitaxially grown on cladding layer 512A, spacer layer 514 epitaxially grown on aluminum tuning layer 513B, active region 515 epitaxially grown on aluminum tuning layer 513B, patterned layer 516 epitaxially grown on active region 515, aluminum tuning layer 513B epitaxially grown on active region 515, cladding layer 512B epitaxially grown on aluminum tuning layer 513B, aluminum tuning layer 513B epitaxially grown on cladding layer 512B, and contact layer 506 epitaxially grown on aluminum tuning layer 511B.

[0070] Laser stacks 510 can have a diameter at the depicted lower elevations in a range of from about 2um to about 10um, and a diameter at the depicted upper elevations in a range of from about 1um to about 5um according to one embodiment. Laser stacks 510 can have a total height (bottom of structure 502 to top of structure 506) in a range of from about 2um to about 20um according to one embodiment, and from about 4um to about 12um according to one embodiment. Buffer material

formations 502 of laser stacks 510 can have a height in a range of from about 1um to about 5um according to one embodiment and from about 2um to about 4um according to one embodiment. The combination of structures from 505, 511A, 512A, 513A, 514, 515, 516, 513B, 512B, 511B, and 506 can have a height in a range of from about 1um to about 10um according to one embodiment, and from about 2um to 6um according to one embodiment.

[0071] As set forth herein voltage can be applied by associated contacts across contact layer 505 and contact layer 506 of each laser stack 510. Such an applied voltage can induce a flow of electrons through structures 511A, 512A, 513A, 514, 515, 516, 513B, 512B, and 511B of a laser stack 510. Each active region 515 can include a conduction band and a valance band. Applying a voltage between contact layer 505 and contact layer 506 can assure that an abundance of electrons reside in a conduction band of an active region 515 and can assure that an abundance of holes reside in a valance band of active region 515 to thus provide conditions suitable for the emission of light by active region 515. Active region 515 can include an associated horizontally extending longitudinal axis. Active region 515 can emit light in a direction parallel to the horizontally extending longitudinal axis.

[0072] Cladding layers 512A and 512B and aluminum tuning layers 511A, 513A, 513B, 511B of laser stack 510 can be configured to aid in the confinement of light within active region 515 and can inhibit light interacting with contact layer 505 and contact layer 506 respectively. For confinement of light within active region 515, each laser stack 510 can include a highest index of refraction within active region 515 and can include reduced indices of refraction at spacing distances within laser stack 510 increasing from active region 515. Aluminum tuning layers 511A, 513A, 513B, 511B can include continuously increasing concentrations of aluminum (Al) as distances increase from active region 515 and can include continuously decreasing indices of refraction as spacing distances increase from active region 515.

[0073] For the formation of aluminum tuning layers 511A, 513Aepitaxially grown on a preceding layer of laser stack 510, deposition parameters can be controlled so that the feedstock of aluminum (Al) is iteratively decreased as the aluminum tuning layer 511A, 513A is epitaxially grown. For the deposition of aluminum tuning layer 513B, 511B epitaxially grown on spacer layer 514, the deposition parameters can be controlled so that a feedstock of aluminum (Al) is iteratively increased as aluminum tuning layer 513B, 511B defining a second gradient layer is epitaxially grown.

[0074] Various deposition technologies can be utilized for the epitaxial growth of structures 502, 505, 513A, 512A, 511A, 514, 515, 516, 513B, 512B, 511B, and 506. According to one embodiment, structures 502, 505, 513A, 512A, 511A, 514, 515, 516, 513B, 512B, 511B, and 506 can be epitaxially grown using molecular beam epitaxy (MBE). The various structures 502, 505, 513A, 512A, 511A, 514, 515, 516, 513B, 512B, 511B, and 506 can be epitaxially grown at one or more temperature within a temperature range of from about 500°C to about 700°C according to one embodiment. According to one embodiment, a deposition temperature can be maintained at a sufficiently low temperature so as not to degrade previously fabricated photonics devices and components such as

structures 401-404, 406-408, 411-412, 421-422. According to one embodiment epitaxially grown structures 502, 505, 513A, 512A, 511A, 514, 515, 516, 513B, 512B, 511B, and 506 can be epitaxially grown using metal organic chemical vapor deposition (MOCVD). According to one embodiment, the various structures 502, 505, 513A, 512A, 511A, 514, 515, 516, 513B, 512B, 511B, and 506 can be epitaxially grown using MOCVD at one or more temperature within a temperature range of from about 550°C to about 750°C.

[0075] According to one embodiment a fabrication temperature for fabricating structures of laser stack 510 can be reduced for fabrication of active region 515 and subsequent structures. Embodiments herein recognize that active region 515 an be subject to performance degradation by subsequent processes at higher temperatures. Accordingly, conditions for fabrication of laser stack 510 can be controlled so that a temperature for fabrication of active region 515 and ensuing structures can be reduced. For example, according to one embodiment, the temperature for epitaxially growing (and annealing where applicable) of the structures of laser stack 510 may be reduced for the formation of active region 515 and ensuing structures so that structures 516, 513B, 512B, 511B, and 506 epitaxially grown subsequent to the formation of active region 515 are fabricated at temperatures of at least about 25°C less than a highest temperature used for fabricating structures preceding active region 515. The active region 515 can be epitaxially grown at about 500°C according to one embodiment and can be epitaxially grown using MOCVD or MBE with annealing temperatures in the temperature range of from about 550°C to about 580°C. According to one embodiment, MOCVD can be used for the formation of structures 502, 505, 511A, 512A, 513A, and MBE can be used for the epitaxially growing of structures 514, 515, 516, 513B, 512B, 511B and 506.

[0076] For growing of laser stack 810, temperature budgets can be applied. A lower stack temperature budget can be applied for the fabrication of structures below active region 515, namely structures 502, 505, 511A, 512A, 513A, and 514. The lower stack temperature budget can be applied for protection of previously fabricated photonics so as not to degrade previously fabricated photonics devices and components such as structures 401-404, 406-408, 411-412, 421-422. According to one embodiment the lower stack temperature budget limit can be established to be about 650°C so that deposition and annealing temperatures for the fabrication of structures below active region 515, namely, structures 502, 505, 511A, 512A, 513A, and 514 does not exceed about 650°C. According to one embodiment the lower stack temperature budget limit can be established to be about 625°C so that deposition and annealing temperatures for the fabrication of structures below active region 515, namely, structures 502, 505, 511A, 512A, 513A, and 514 does not exceed about 625°C. According to one embodiment the lower stack temperature budget limit can be established to be about 600°C so that deposition and annealing temperatures for the fabrication of structures below active region 515, namely, structures 502, 505, 511A, 512A, 513A, and 514 does not exceed about 600°C. According to one embodiment the lower stack temperature budget limit can be established to be about 580°C so that deposition and annealing temperatures for the fabrication of structures below active region 515, namely, structures 502, 505, 511A, 512A, 513A, and 514 does not exceed about 580°C.

[0077] An upper stack temperature budget can be applied for the fabrication of structures including and above active region 515, namely structures 515, 516, 513B, 512B, 511B, and 506. The upper stack temperature budget can be applied for protection of active region 515. According to one embodiment the upper stack temperature budget limit can be established to be about 650°C so that deposition and annealing temperatures for the fabrication of structures including and above active region 515, namely, structures 515, 516, 513B, 512B, 511B, and 506 does not exceed about 650°C. According to one embodiment the upper stack temperature budget limit can be established to be about 625°C so that deposition and annealing temperatures for the fabrication of structures including and above active region 515, namely, structures 515, 516, 513B, 512B, 511B, and 506 does not exceed about 625°C. According to one embodiment the upper stack temperature budget limit can be established to be about 600°C so that deposition and annealing temperatures for the fabrication of structures including and above active region 515, namely, structures 515, 516, 513B, 512B, 511B, and 506 does not exceed about 600°C. According to one embodiment the upper stack temperature budget limit can be established to be about 580°C so that deposition and annealing temperatures for the fabrication of structures including and above active region 515, namely, structures 515, 516, 513B, 512B, 511B, and 506 does not exceed about 580°C. According to one embodiment, the upper stack temperature budget limit can be established to be lower that the lower stack temperature budget limit. According to one embodiment, each of the upper stack temperature budget limit the lower stack temperature budget limit can be established to be lower than a temperature budget limit for fabrication of photonics devices and components such as structures 401-404, 406-408, 411-412, 421-422.

[0078] With the input of electrical energy, electrons can be injected into laser stack 510. Laser stack 510 of each laser light source 500 can be configured to facilitate a flow of electrons through the laser stack 510 with a high density of electrons formed in the active region 515. The flow of electrons can be facilitated with appropriate electrical energy inputs at bottom contact layer 505 and/or top contact layer 506 made through contacts fabricated as set forth herein. With electrons occupying active region 515 of a laser stack 510 the device can emit light.

[0079] Fig. 2H illustrates photonics structure 10 shown in Fig. 2G in an intermediary stage of fabrication after performing processes for the fabrication of contacts C1-C13. For the formation of contacts C1-C13 contact trenches having respective vertically extending center axes can be etched in photonics dielectric stack 200. Following the formation of the contact trenches, the contact trenches can be filled with contact conductive material, e.g. conductive metal. The conductive material can be deposited to overfill the conductive material trenches and then can be subject to CMP to define a horizontally extending planar surface at elevation 2026.

[0080] Fig. 2I illustrates the photonics structure 10 as shown in Fig. 2H in an intermediary stage of fabrication subsequent to further processing to define metallization layer 602, vias layer 702, and metallization layer 612. For the formation of metallization layer 602 trenches can be formed in photonics dielectric stack 200 to extend to a bottom elevation defined at elevation 2026 which is the

top elevation of contacts C1-C13. For the formation of metallization layer 602 metallization layer formation trenches can be formed to include center axes at the centers of metallization layer formations M1 shown in Fig. 2I. The metallization layer trenches can be overfilled with conductive metal material and then subject to CMP to define a planar horizontal surface at the depicted top elevation 2027 of metallization layer formations. A dielectric layer can then be deposited and then subject to CMP to increase the elevation of photonics dielectric stack 200 to elevation 2028 and vias trenches can be formed to include center axes at the vertical centers of respective vias V1 as shown in Fig. 2I.

[0081] The vias trenches can be overfilled and subject to CMP so that a top elevation of photonics dielectric stack 200 is defined at elevation 2028, the top of vias V1. Dielectric material, e.g. oxide can be deposited on the horizontal surface defined at elevation 2028 and then can be subject to CMP to define a horizontal planarized surface at elevation 2029. Metallization layer trenches can be formed in photonics dielectric stack 200 having metallization layer trench center axes at the center axes of respective metallization layer formations M2 as shown in Fig. 2I. The metallization layer trenches can be overfilled and subject to CMP to define a horizontally extending planar surface at elevation 2029, and then a further layer of dielectric material, e.g. oxide can be deposited on the horizontally extending surface at elevation 2024 which additional layer can be subject to CMP to define a top elevation in the intermediary stage view of photonics dielectric stack 200 at elevation 2030.

[0082] All of the components depicted within photonics dielectric stack 200 of Figs. 2A-2H can be integrally formed and fabricated within photonics dielectric stack 200 using semiconductor device processes characterized by photolithography semiconductor device fabrication stages and/or chemical semiconductor device fabrication stages.

[0083] In the fabrication stage of Fig. 2H, there is described a process wherein bottom contacts, e.g., contacts C5, C6, C8, C9, C11 and C12 for respective laser sources are fabricated with use of top side metallization. For example, for the formation of contact C5, a trench can be formed through a top surface of photonics structure 10 and filled with conductive material.

[0084] Contact layer 505 of the laser stack 510 at location “C” is shown as having a higher elevation than the laser stacks of locations “A” or “B”. Locating contact layer 505 at a higher elevation can reduce energy. On the deposition of aluminum tuning layer 513A the laser stack trenches at location A and B having associated center axes 7042 and 7052 can be covered with masking material and contact layer 505 formed of conductive material can be deposited on aluminum tuning layer 513A at location C. The laser stack trench at location C can then be filled with dielectric material and the laser stack trench can be re-formed to have a center centered again on center axis 7062 and a narrower diameter to define sidewalls intersecting vertically extending plane 7065 and vertically extending plane 7067 as indicated in Fig. 2G. Each of the laser stack trenches generally at “A” and “B” can then be reopened for further processing, including by laser stack layer growing. At laser stack trench 510 of location C, contact layer 505 can be etched to expose a top surface of aluminum tuning layer 513A.

Contact layer 505 and contact layer 506 can be in situ doped during a deposition stage specific for the formation of the layer. According to one embodiment, contact layer 505 and/or contact layer 506 at one or more of the locations A B and C can be formed by way of doping of a previously deposited layer. At laser stack 510 of location C, for example, contact layer 505 can be formed by ion implantation of layer 513A.

[0085] Fig. 3 is a cutaway side view of photonics structure 10 having bottom contacts alternatively formed reactive to photonics structure 10 depicted in Fig. 1. An alternative process for the formation of bottom contacts for laser sources 500 is illustrated with respect to the fabrication stage use of Figs. 4A and 4B.

[0086] Referring to Fig. 4A, the fabricating of structures within photonics dielectric stack 200 is performed in the manner of Fig. 2H except that the stages for the formation of laser source bottom contacts C5, C6, C8, C9, C11 and C12 are avoided and not performed and hence in the intermediary stage view depicted in Fig. 4A photonics structure 10 is absent of bottom contacts C5, C6, C8, C9, C11.Referring to the intermediary fabrication stage view of Fig. 4A, a handle wafer 1100 can be attached to a top side of photonics dielectric stack 200 with use of adhesive layer 1102. Handle wafer 1100 as shown in Fig. 4A, can be held by a wafer handler to facilitate backside processing of photonics structure 10.

[0087] With photonics structure 10 as shown in Fig. 4A placed in a wafer handler to facilitate backside processing, substrate 100, e.g., in a state substantially as depicted in Fig. 2H can be removed. With the removal of substrate 100 (Fig. 2H), laser stack buffer structures 502 can also be removed. For removal of substrate 100 and buffer structures 502, grinding process can be performed for the majority of the material removal with the last threshold percentage, e.g., 10% or less of material being removed with use of a reactive ion etching (RIE) process.

[0088] Fig. 4B illustrates photonics structure 10 in an intermediary stage of fabrication as shown in Fig. 4B after further fabrication to fabricate through via VX2, to extend photonics dielectric stack 200 and to fabricate additional structures within the extended photonics dielectric stack 200. After removal of material of substrate 100 to elevation 2012 to reveal contact layer 505 of laser stacks 510, dielectric material can be deposited and then subject to CMP to define a horizontally extending planar surface at elevation 2007. Trenches can then be formed for the fabrication of through via VX2 and bottom contacts C21, C22 and C23 of respective laser stacks 510. Conductive material can then be deposited in the respective trenches to define through via VX2, bottom contacts C21, C22 and C23 of respective laser stacks 510.

[0089] Dielectric material can be deposited and can be subject to CMP to define a horizontally extending planar surface at elevation 2006. Metallization trenches can then be formed. Metallization layer 1602 can be deposited in the metallization trenches and can be subject to CMP to define metallization formations M11 and to define a top surface of photonics structure 10 at elevation 2006.

Dielectric depositing and CMP can then be performed to define a horizontally extending planar surface at elevation 2005. With photonics structure 10 in a stage having a top elevation at elevation 2005 vias trenches to define vias V21 can be etched and conductive material forming vias layer 1702 can be deposited in the vias trenches to define vias V21.

[0090] Dielectric material can be deposited at elevation 2005 and then subject to CMP to define a horizontally extending planar surface at elevation 2004. Metallization trenches can then be formed and metallization layer 1612 can be deposited in the metallization trenches to define metallization formations M12.

[0091] Dielectric material can be deposited at elevation 2005 and then subject to CMP to define a horizontally extending planar surface at elevation 2004. Trenches can be formed as shown to expose metallization formations. Terminations 6002 can then be fabricated. A termination 6002 can include, e.g., one or more of (a) an opening formed in photonics dielectric stack 200 opening to metallization layer 612; (b) a pad formed on metallization layer 612 and an opening to the pad; (c) an under bump metallization (UBM) layer formed on the metallization layer 612 with an opening formed in photonics dielectric stack 200 to the UBM; (d) a UBM formed on metallization layer 612 and a solder bump formed on the UBM externally protruding from photonics dielectric stack 200.

[0092] Fabricating according to the stage views depicted in Figs. 4A and 4B culminating in the photonics structure 10 of Fig. 3 having terminations 6002 provided by backside terminations can reduce the height requirements of contacts connecting to contact layer 505. Tolerances and costs associated with the fabrication of such contacts accordingly can be reduced, and performance speed can be increased. Fabricating according to the stage views of Figs 2A-2l culminating in in the photonics structure 10 of Fig. 1 having terminations 6002 provided by frontside terminations can avoid additional processing stages e.g. for removal of material of substrate 100.

[0093] In the views of Figs. 1-2I, laser stack 510 is depicted as having a certain bottom elevation. Referring to Fig. 2F, laser stacks 510 are depicted as having a bottom elevation at elevation 2002 within an elevation of substrate 100, which is the bottom elevation of buffer material formation 502.

[0094] Embodiments herein recognize that laser stacks 510 can be fabricated to have different bottom elevations and that different elevations can be yielded by the selection of such different bottom elevations. Embodiments herein recognize that a bottom elevation of laser stack 510 can be selected for optimization of light coupling according to a targeted light coupling scheme. According to some embodiments, a bottom elevation of laser stack 510 can be selected based on a selected coupling method for coupling light from active region 515 of laser stack 510 into one or more waveguide.

[0095] Figs. 5A-5D depict differentiated coupling schemes coupling methods and structures for coupling light from active region 515 of laser stack 510 into a waveguide and also illustrate

differentiated fabrication schemes wherein a bottom elevation of laser stack 510 can be selected in dependence on a selected coupling scheme for coupling light from active region 515 of laser stack 510 into one or more waveguide.

[0096] For coupling light from active region 515 into a waveguide, photonics structure 10 can be fabricated so that horizontally extending longitudinal axis of a waveguide can be aligned and coincident with a horizontally extending longitudinal axis of active region 515. Fig 5A depicts laser source 500 as shown in Fig. 1, taken along the Z-Y plane rather than the ZX plane, as shown in Fig. 1 (Fig. 5A illustrates a view, extending into and out of the paper, as shown in Fig. 1).

[0097] Referring to Fig. 5A, photonics structure 10 can be fabricated and accordingly configured so that active region 515 and waveguide 451 are arranged so that horizontally extending longitudinal axis of active region 515 aligns with and coincides with a horizontally extending longitudinal axis of waveguide 451. The horizontally extending longitudinal axes of active region 515 and waveguide 451 can be coincident with axis 2515 as shown. Waveguide 451 can be fabricated by patterning of layer 302, which is silicon layer 302 as depicted in Fig. 1, which is the silicon layer of pre-fabricated silicon on insulator (SOI) wafer. Fig. 5A depicts direct coupling of active region 515 into waveguide 451 formed to silicon, wherein the silicon depicted is the silicon layer of an originally fabricated SOI wafer.

[0098] Fig. 5B depicts an alternative scheme for coupling light from active region 515 of laser stack 510 into waveguide 451. In the coupling scheme depicted in Fig. 5B, waveguide 452 fabricated from nitride layer 3002 and waveguide 453 fabricated from nitride layer 3004 can be fabricated to be disposed in proximity with waveguide 451, fabricated from layer. Waveguide 452 and waveguide 453 can be nitride e.g. SIN silicon nitride waveguides patterned in the manner described with reference to waveguide 411 and waveguide 421 set forth in reference to Fig. 1 and Figs. 2A-2D.

[0099] Waveguide 452 and waveguide 453 can be sized, shaped, and located, and perform an evanescent coupling function wherein light propagating through waveguide 451 about axis 2515 can evanescently couple onto waveguide 452 and/or waveguide 453 and can recouple by way of evanescent in coupling back into waveguide 451 to improve overall light transmission through waveguide 451.

[00100] Fig. 5C depicts an alternative coupling scheme for coupling light from active region 515 a laser stack 510 to one or more waveguide. In photonics structure 10 as depicted in Fig. 5C a horizontally extending longitudinal axis of active region 515 and a horizontally extending longitudinal axis of waveguide 467 can be aligned and can be coincident with each other on axis 2515. Waveguide 467 can be a waveguide patterned from layer 3014 formed of nitride.

[00101] Photonics structure 10, as depicted in Fig. 5C can include waveguide 461 patterned from layer 3002 waveguide 462 patterned from layer 3004 waveguide 463 patterned from layer 3006 waveguide 464 patterned from layer 3008 waveguide 465 patterned from layer 3010, waveguide 466 patterned

from 3012, and waveguide 467 patterned from layer 3014. Layers 3002, 3004, 3006, 3008, 3010, 3012,3014 can be nitride layers so that the fabricated respective waveguides 461-467 are nitride waveguides. Waveguides 461-467 as depicted in Fig. 5C can be fabricated to be in a step-wise pattern to encourage evanescent coupling between the waveguides 461-467, namely light propagating through waveguide 467 can evanescently couple into waveguide 466 which light can evanescently couple into waveguide 465 which light can evanescently couple into waveguide 464 which can evanescently couple into waveguide 463 which light can evanescently couple into waveguide 462 which light can evanescently couple into waveguide 461 which light can evanescently couple into waveguide 451 patterned from layer 3002 formed of silicon. Photonics structure 10 is depicted in Fig. 5C illustrates a coupling scheme wherein light emitted from active region 515 of laser stack 510 can directly couple into a waveguide 467 formed of nitride and thereafter can evanescently couple through a series of waveguides eventually into waveguide 451 formed of silicon, which waveguide 451 can be patterned from layer 302 formed of silicon which can be a silicon layer of a prefabricated silicon on insulator (SOI) wafer. For facilitation of the coupling scheme depicted in Fig. 5C of bottom elevation of laser stack 510 can be selected and fabricated to have a higher elevation than laser stack 510 depicted in Fig. 1.

[00102] Waveguides 4067-461 as depicted in Fig. 5C can be sized, shaped and located to facilitate evanescent coupling of light from waveguide 467 downwardly through waveguides 466-461 and eventually into waveguide 451 formed of silicon.

[00103] In the coupling scheme depicted in Fig. 5D a bottom elevation of laser stack 510 is at a higher elevation than as depicted in the arrangement of Fig. 5C.

[00104] Photonics structure 10 as shown in Fig. 5D can be fabricated so that buffer material formation 502 is a epitaxially grown on a top surface of layer 302, which can be the silicon layer of a pre-fabricated silicon on insulator (SOI) wafer. Layer 302 as shown throughout the views, according to one embodiment, can feature advantages associated with being prefabricated with use of high temperature treatments e.g. above 500 degrees C, in some cases above 700 degrees C and in some cases above 1000 degrees C. Layer 302, which can be prefabricated as part of an SOI wafer, can be subject to annealing processes for annihilation of defects with use of a thermal budget that can be limited after patterning of layer 302 for fabrication of devices.

[00105] The coupling scheme depicted in Fig. 5D can operate in the manner of the coupling scheme as described in connection with photonic structure 10 as shown in Fig. 5C. Horizontally extending longitudinal axes of active region 515 and horizontally extending longitudinal axis of waveguide 477 can be aligned and can be coincident on axis 2515. Light emitted from active region 515 can be directly coupled into waveguide 477 formed of nitride. Light coupling into waveguide 477 can evanescently couple successively though the series of waveguides 476, and 475, 474, 473, 472, and 471 and eventually into waveguide 451, which can be patterned from layer 302 which can be the

silicon layer of a prefabricated SOI wafer. Waveguides 477-471 as depicted in Fig. 5D can be sized, shaped, and located in relative positions to facilitate evanescent coupling downward through the series of waveguides 477 through waveguide 471, and ultimately into waveguide 451, patterned from layer 302 formed of silicon (Si).

[00106] Waveguide such as waveguide 451 (Figs. 5A-5B), waveguide 467 (Fig. 5C) and waveguide 477 (Fig. 5D) that are coupled to an active region 515 of a laser stack can be edge coupled to active region 515. For promotion of light coupling between active region 515 and a waveguide edge coupled to the active region, the active region and the waveguide can be configured to include compatible mode profiles, wherein the respective mode profiles define respective spatial area distributions of a traveling light signal. Mode profiles can be tuned using e.g. indices of refraction e.g. of the active region 515, the edge coupled waveguide, the respective geometries of active region 515 and the edge coupled waveguide and the index of refraction of dielectric material surrounding the edge coupled waveguide and laser stack 510. With the design parameters tuned for configuration of compatible mode profiles, light signal losses including by way of reflections returned to active region (recycling losses) can be reduced. According to some embodiments, for reduction of light losses, light entry ends of edge coupled waveguides that are edge coupled to active region 515 can be tapered.

[00107] For optimizing evanescent coupling between waveguides, size, shape, and location of evanescently coupled waveguides can be coordinated. For tuning of evanescent coupling, parameters that can be controlled can include: (a) Z direction spacing distance, d, as depicted in Figs. 5C-5D, (b) overlap length, l, as depicted in Fig. 5C-5D, and (c) taper geometry. Tapered evanescently coupled waveguides are depicted in Fig. 5E. To promote evanescent coupling between first and second waveguides, waveguides can have overlapping tapered ends.

[00108] As shown in Fig. 5E depicting a top Y-X plane view of first and second waveguides, first waveguide 491 can have a tapered end 4911 coordinated to a tapered end 4921 of second waveguide 492, wherein second waveguide has an elevation lower than that of waveguide 491 (and therefore is depicted in dashed form). First waveguide 491 and second waveguide 492 can represent any combination of any combination of upper and lower evanescently coupling waveguides as depicted in Figs. 5A-5D. Characteristics of evanescent coupling can be in dependence on various additional parameters e.g. the index of refraction of first waveguide 491, the index of refraction of second waveguide 492, the index of refraction of surrounding dielectric material of photonics dielectric stack 200 surrounding the waveguides, and the wavelength of traveling light.

[00109] In any of the described embodiments of a laser stack 510, a square groove trench for accommodation of the deposition of material defining buffer material formation 502 can be substituted by a V groove trench indicated by the dashed line 902 depicted in Fig. 5A. The presence of a V groove trench can according to some embodiments reduce the formation of defects during the deposition process.

[00110] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. The term “on” in one embodiment can refer to a relationship where an element is “directly on” a specified element without intervening elements between the element and the specified element. As used herein, the singular forms “a,” “an,” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprise” (and any form of comprise, such as “comprises” and “comprising”), “have” (and any form of have, such as “has” and “having”), “include” (and any form of include, such as “includes” and “including”), and “contain” (and any form contain, such as “contains” and “containing”) are open-ended linking verbs. As a result, a method or device that “comprises,” “has,” “includes,” or “contains” one or more steps or elements possesses those one or more steps or elements, but is not limited to possessing only those one or more steps or elements. Likewise, a step of a method or an element of a device that “comprises,” “has,” “includes,” or “contains” one or more features possesses those one or more features, but is not limited to possessing only those one or more features. Forms of the term "defined by" encompass relationships where an element is partially defined by as well relationships where an element is entirely defined by. Numerical identifiers herein, e.g. "first" and "second" are arbitrary terms to designate different elements without designating an ordering of elements. Furthermore, a system method or apparatus that is configured in a certain way is configured in at least that way, but may also be configured in ways that are not listed. Furthermore, a system method or apparatus set forth as having a certain number of elements can be practiced with less than or greater than the certain number of elements.

[00111] The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below, if any, are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of one or more aspects of the invention and the practical application, and to enable others of ordinary skill in the art to understand one or more aspects of the invention for various embodiments with various modifications as are suited to the particular use contemplated.

CLAIMS

What is claimed is:

1. A photonics structure comprising:

a substrate;

a dielectric stack disposed on the substrate;

one or more photonics device integrated in the dielectric stack; and

a laser light source having a laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are integrated in the dielectric stack, wherein the laser stack includes an active region configured to emit light in response to the application of electrical energy to the laser stack, wherein the laser light source includes a buffer material formation having a bottom elevation below a top elevation of the substrate.

2. The photonics structure of claim 1, wherein the laser light source includes a buffer material formation, a cladding layer, an aluminum tuning layer and an active region.

3. The photonics structure of claim 1, wherein the dielectric stack is defined by an insulator layer of a silicon on insulator (SOI) wafer, and wherein a photonics device of the one or more photonics device is defined by a silicon layer of the SOI wafer.

4. The photonics structure of claim 1, wherein the one or more photonics device integrally formed within the dielectric stack includes a waveguide, wherein the active region has an elevation in common with waveguide, and wherein the active region is configured to emit light into the waveguide.

5. The photonics structure of claim 1, wherein the one or more photonics device integrally formed within the dielectric stack includes a monocrystalline silicon waveguide having a horizontally extending longitudinal axis, wherein the horizontally extending longitudinal axis of the waveguide is aligned with a horizontally extending longitudinal axis of the active region, and wherein the active region is configured to emit light into the monocrystalline silicon waveguide.

6. The photonics structure of claim 1, wherein the one or more photonics device integrally formed within the dielectric stack includes a nitride waveguide having a horizontally extending longitudinal axis, wherein the horizontally extending longitudinal axis of the waveguide is aligned with a horizontally extending longitudinal axis of the active region, and wherein the active region is configured to emit light into the nitride waveguide.

7. The photonics structure of claim 1, wherein the one or more photonics device integrally formed within the dielectric stack includes a nitride waveguide having a horizontally extending longitudinal axis, wherein the horizontally extending longitudinal axis of the waveguide is aligned with a horizontally extending longitudinal axis of the active region, and wherein the active region is configured to emit light into the nitride waveguide, wherein the dielectric stack is defined by an insulator layer of a silicon on insulator (SOI) wafer, and wherein a photonics device of the one or more photonics device is monocrystalline waveguide defined by a silicon layer of the SOI wafer, wherein the photonics structure includes a plurality of waveguides arranged in an overlapping stepwise pattern configured to evanescently couple light emitted from the active region into the monocrystalline waveguide defined by a silicon layer of the SOI wafer.

8. The photonics structure of claim 1, wherein the laser light source includes a buffer material formation, a contact layer, an aluminum tuning layer and an active layer.

9. The photonics structure of claim 1, wherein the one or more photonics device disposed within the dielectric stack includes a monocrystalline silicon waveguide having a horizontally extending longitudinal axis, wherein the horizontally extending longitudinal axis of the waveguide coincides with a horizontally extending longitudinal axis of the active region, and wherein the active region is configured to emit light into the monocrystalline silicon waveguide.

10. The photonics structure of claim 1, wherein the substrate is a substrate of a silicon on insulator (SOI) wafer having a silicon layer formed on an insulator which is formed on the substrate, wherein the one or more photonics device includes a waveguide defined by the silicon layer, the waveguide being being aligned with the active region.

11. The photonics structure of claim 1, wherein the one or more photonics device includes each of a photodetector integrated in the dielectric stack, a modulator integrated in the dielectric stack and, and a waveguide integrated in the dielectric stack.

12. The photonics structure of claim 1, wherein the photonics structure includes a second laser light source having a second laser stack, wherein the laser stack and the second laser stack each include a bottom contact layer interfaced to a contact, wherein the bottom contact layer of the second laser stack is at a higher elevation than a bottom contact layer of the laser stack.

13. The photonics structure of claim 1, wherein the dielectric stack is defined by an insulator layer of an SOI wafer, and wherein the laser stack extends entirely through elevations of the insulator layer.

14. A method comprising:

patterning a waveguide in a silicon layer of a silicon on insulator (SOI) wafer of a photonics structure having a dielectric stack defined by an insulator of the SOI wafer;

forming in the photonics structure a trench extending through dielectric layers of the dielectric stack; and

epitaxially growing a laser stack within the trench, the laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are disposed within the dielectric stack and include an active region configured to emit light in response to the application of electrical energy to the laser stack, wherein the forming in the photonics structure a trench extending through dielectric layers of the dielectric stack includes forming in the photonics structure a trench extending through dielectric layers of the dielectric stack so that the trench has a bottom elevation lower than a top elevation of a substrate of the SOI wafer.

15. The method of claim 14, wherein the active region is aligned with the waveguide.

16. The method of claim 14, wherein the waveguide is horizontally extending and disposed at an elevation in common with an elevation of the active region which is aligned with the waveguide and wherein the active region emits light horizontally so that light emitted by the active region is coupled into the waveguide.

17. The method of claim 14, wherein the patterning the waveguide in the silicon layer includes using a first process temperature range, and wherein the epitaxially growing includes epitaxially growing a buffer material formation defining the laser stack using a second process temperature

range, wherein a highest temperature of the second process temperature range is lower than a highest temperature of the first process temperature range.

18. The method of claim 14, wherein the epitaxially growing the laser stack includes epitaxially growing a buffer material formation, epitaxially growing a contact layer on the buffer material formation, epitaxially growing a first aluminum tuning layer the buffer material formation, epitaxially growing a second cladding layer on the first aluminum tuning layer, epitaxially growing a second aluminum tuning layer on the first cladding layer, epitaxially growing a spacer layer on the second aluminum tuning layer and epitaxially growing the active region on the spacer layer.

19. The method of claim 14, wherein the active region comprises quantum dots.

20. The method of claim 14, wherein the epitaxially growing a laser stack within the trench includes epitaxially growing a buffer material formation on a silicon surface defined by the substrate, wherein the method includes removing the substrate and material of the buffer material formation to reveal a bottom side surface of the dielectric stack, and fabricating an extended dielectric stack region on the bottom side surface of the dielectric stack, wherein the method includes fabricating in the extended dielectric stack region an integrated electrical contact that contacts a contact layer of the laser stack, and fabricating a termination in electrical communication with the electrical contact.

21. The photonics structure of claim 1, wherein the laser stack includes a first tuning layer for confining light within the activation region at an elevation lower than the active region, and a second tuning layer for confining light within the activation region at an elevation higher than the active region.

22. The photonics structure of claim 1, wherein the laser stack includes a patterned layer pattern integrated in the dielectric stack for selection of a wavelength at which the active region operates.

23. A photonics structure comprising:

a substrate;

a dielectric stack disposed on the substrate;

one or more photonics device integrated in the dielectric stack; and

a laser light source having a laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are integrated in the dielectric stack, wherein the laser stack includes an active region configured to emit light in response to the application of electrical energy to the laser stack, wherein the dielectric stack is defined by an insulator layer of a silicon on insulator (SOI) wafer, and wherein a photonics device of the one or more photonics device is monocrystalline waveguide defined by a silicon layer of the SOI wafer, wherein the photonics structure includes a plurality of waveguides arranged in an overlapping stepwise pattern configured to evanescently couple light emitted from the active region into the monocrystalline waveguide defined by a silicon layer of the SOI wafer.

24. A photonics structure comprising:

a substrate;

a dielectric stack disposed on the substrate;

one or more photonics device integrated in the dielectric stack; and

a laser light source having a laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are integrated in the dielectric stack, wherein the laser stack includes an active region configured to emit light in response to the application of electrical energy to the laser stack, wherein the photonics structure includes a second laser light source having a second laser stack, wherein the laser stack and the second laser stack each include a bottom contact layer interfaced to a contact, wherein a bottom contact layer of second laser stack is at a higher elevation than a bottom contact layer of the laser stack.

25. A photonics structure comprising:

a substrate;

a dielectric stack disposed on the substrate;

one or more photonics device integrated in the dielectric stack; and

a laser light source having a laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are integrated in the dielectric stack, wherein the laser stack includes an active region configured to emit light in response to the application of electrical energy to the laser stack, wherein the dielectric stack is defined by an insulator layer of an SOI wafer, and wherein the laser stack extends entirely through elevations of the insulator layer.

26. A photonics structure comprising:

a substrate;

a dielectric stack disposed on the substrate;

one or more photonics device integrated in the dielectric stack; and

a laser light source having a laser stack including a plurality of structures arranged in a stack, wherein structures of the plurality of structures are integrated in the dielectric stack, wherein the laser stack includes an active region configured to emit light in response to the application of electrical energy to the laser stack, wherein the dielectric stack is defined by an insulator layer of an SOI wafer, wherein a bottom elevation of the laser stack is defined by a bottom elevation of a buffer material formation, the buffer material formation having a bottom elevation within an elevation of the insulator layer.

27. The photonics structure of claim 25, wherein the laser light source include a buffer material formation having a bottom elevation below a top elevation of the substrate.

28. The photonics structure of claim 24, wherein the bottom contact layer of the second laser stack is epitaxially grown on an aluminum tuning layer of the second laser stack, wherein the bottom contact layer of the laser stack is epitaxially grown on a buffer material formation of the laser light source.