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(71) Applicant *(for all designated States except US)*: **DOW GLOBAL TECHNOLOGY INC.** [US/US]; Washington Street, 1790 Building, Midland, MI 48674 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **TOWNSEND, Paul, H., III** [US/US]; 1102 Willard Street, Midland, MI 48642 (US). **MILLS, Lynne, K.** [US/US]; 1604 Avalon Street, Midland, MI 48642 (US). **WAETERLOOS, Joost, J., M.** [BE/BE]; Leeuwerikenstraat 53 B 503, Heverlee, B-3001 Vlaams Brabant (BE). **STRITTMATTER, Richard, J.** [US/US]; 5717 Stillwater Lane, Midland, MI 48642 (US).

(74) Agent: **ZERULL, Susan, Moeller**; The Dow Chemical Company, Intellectual Property, P.O. Box 1967, Midland, MI 48641-1967 (US).

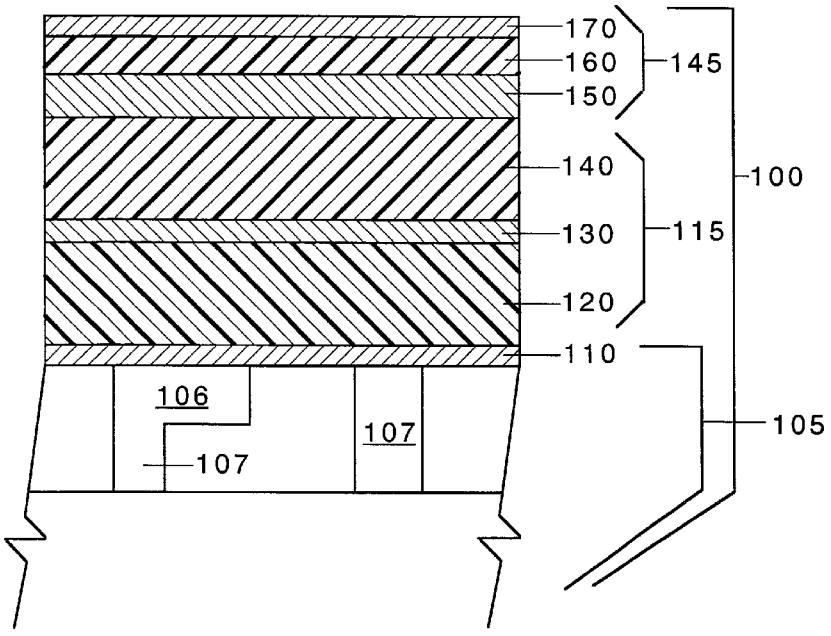
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(54) Title: TRI-LAYER MASKING ARCHITECTURE FOR PATTERNING DUAL DAMASCENE INTERCONNECTS



(57) Abstract: This invention relates to a method of dual damascene integration for copper based wiring in a low-k dielectric stack (120, 130, 140) using three top hard mask layers (150, 160, 170) having alternating etch selectivity characteristics, and being, for example, inorganic/organic/inorganic.

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