ABSTRACT

A NEW FLASH MEMORY ARRAY STRUCTURE WITH REDUCED BIT-LINE PITCH

A new method is provided for the creation of floating gates of a flash memory array. The floating gates of conventional flash memory devices are formed using a single polysilicon deposition followed by a single polysilicon etch. The invention provides a method that allows for the reduction in the spacing between adjacent floating gates by providing a double polysilicon deposition followed by a double polysilicon etch process. The process of the invention starts with the formation of FOX regions in a semiconductor surface; the channel regions of the devices are implanted. The first half of the floating gates of the device are formed followed by the formation of the second half of the floating gates of the device. The control gate of the device is formed as a last step of the processes of the invention.

(FIGURE 2a IS SUGGESTED FOR PUBLICATION)