

Description

Related U.S. patent applications

U.S. Patent applications directly or indirectly related to the subject application are the following:

Serial No. 457,176, filed January 11, 1983 by Fazil I. Osman and entitled "A Dynamic Re-programmable PLA", and

Serial No. 457,177, filed January 11, 1983 by David W. Page and entitled "A Dynamic Data Re-programmable PLA".

Background of the invention

This invention relates to programmable logic arrays (PLA's), and more particularly, to PLA's which are readily re-programmable.

In general, a PLA is a logic circuit which receives a plurality of digital input signals and generates a plurality of digital output signals wherein each of the digital output signals is a programmable sum-of-product combination of the input signals. In conventional PLA's, one circuit is provided for generating a plurality of terms which are the logical AND of selected input signals; and another circuit is provided to generate the output signals by selectively ORing the AND terms. A typical PLA may have a total of x input signals, generate a total of y AND terms from the input signals, and generate a total of z output signals by selectively ORing the y AND terms.

An article describing PLA's in more detail is "Field-PLA's Simplify Logic Designs", which was published in *Electronic Design* of September 1, 1975, at pages 84-90. Another series of articles describing PLA's are "Field-programmable Arrays: Powerful Alternatives to Random Logic", *Electronics*, July 5, 1979, pages 89-94; and "Field-programmable Logic, Part 2: Sequencers and Arrays Transform Truth Tables into Working Systems", *Electronics*, July 19, 1979, pages 95-102.

The general design of a PLA includes an AND array feeding into an OR array. The AND array accepts n inputs and divides them into data and data complement for each data line.

These data lines feed an array of terms m deep. Each term is the AND combination of data, data complement and don't care for each input (don't care is formed by ignoring data and data complement for a given input), hence a typical program may appear as:

term 1=AAB
term 2= $\bar{A}\bar{A}B$
term $m=\bar{B}$

The term lines then feed into an OR array where each term line may be selectively OR'd into an output (the array is $m \times k$ where k is the number of outputs).

The prior art PLA's are typically designed for use in systems requiring permanent or semipermanent nonvolatile logic arrays. PROM's (pro-

grammable read only memories) are frequently used to implement logic arrays, which PROM's are usable only once after programming (i.e., the program cannot be changed once made). EPROM's (erasable PROM's) can be changed by the use of an ultraviolet light, which erasure requires several hours to complete. Also, another problem with EPROM's is that they are expensive.

EEPROM's (electrically erasable PROM's), which are even more expensive than EPROM's, require special power supplies. Furthermore, PROM's are not configured as PLA's. In EP-A-00 038 947 a re-programmable logic array comprising an AND array and OR array is disclosed, in which series-connected storage elements associated with each cell enable or disable the associated cell, in accordance with the binary state stored. The storage elements are loaded by a number of input terminals.

Summary of the invention

An advantage of the present invention resides in the provision of a unique design that is readily adaptable to standard MOS (metal oxide semiconductor) fabrication techniques.

Another advantage of this invention is the provision of a PLA design that is readily programmable or re-programmable as required.

According to the invention a programmable logic array according to claim 1 is provided.

Brief description of the drawings

Fig. 1 is a logic-schematic diagram of the PLA of this invention;

Fig. 2 is a schematic diagram of a register element used in this invention; and,

Fig. 3 is a timing diagram illustrating operation of the invention.

Detailed description of the invention

Referring now to the drawings and in particular to Fig. 1, a programmable logic array (PLA) 10 in accordance with the present invention is illustrated in detail. A shift register including flip-flop register elements 12-1, 12-2, ... 12- m , 14-1, 14-2, ... 14- m , 17-1, 17-2, ... 17- m ... are coupled together in a serial fashion. The data input of the flip-flop 12-1 is coupled to an input terminal 20, which terminal is disposed for serially receiving program data referred to herein as "I". The output terminal "Q" of the flip-flop 12-1 is coupled to the data input terminal "D" of the flip-flop 12-2, and so forth, in a similar serial fashion for the remaining flip-flops of the shift register. A clock signal is supplied on a terminal 22, which clock signal is coupled in parallel to the clock "CK" input terminals of each of the flip-flops of the shift register. The operation of a serial shift register is well-known in the art, and will not be explained further hereafter.

The output of the flip-flop 12-1 is also coupled to the gate terminal of an MOS transistor 24. The drain terminal of the transistor 24 is coupled to ground potential and the source terminal thereof is coupled to the drain terminal of a second MOS

transistor 26. The source terminal of the transistor 26 is coupled to a term line 28 which is also coupled to a power supply V_{cc} through a resistor R10. This biases the term line to a high-level voltage.

The gate terminal of the transistor 26 is coupled to an address line A_1 . The flip-flop 12-1 and the transistors 24 and 26 form a single cell of the AND array of the PLA 10, which is made up of a multiplicity of such cells arranged in an array of $2n \times m$ cells. Block 34 represents numerous additional such cells as that described above organized in a similar fashion and having address lines A_2 through A_n including the complements of these address lines ($\bar{A}_2$ through $\bar{A}_n$).

The term line 28 is also coupled to the gate terminal of a transistor 36, and the source terminal of this transistor is coupled to output line O_1 . The output line O_1 is biased at a high-level voltage by means of the V_{cc} voltage supply through a resistor R20. The drain terminal of the transistor 36 is coupled to the source terminal of a transistor 38 and the drain terminal of this transistor is coupled to ground potential. The gate terminal of the transistor 38 is coupled to the output terminal of the flip-flop 17-1.

The flip-flop 17-1 and the transistors 36 and 38 form a single cell of the OR array of the PLA 10, which OR array is arranged in an array of $k \times m$ cells. Block 40 represents numerous additional such cells organized in a similar fashion, and having output lines O_2 through O_k .

The above-described PLA is programmed by serially loading data into the shift register on the terminal 20 ("I"). That is, the input data "I" is supplied (one bit at a time) on the terminal 20 while a clock signal ("CK") is supplied on the terminal 22.

Assume that the output of the flip-flop 12-1 is at a high level, and the transistor 24 is turned on. The terms high and low level are used in a conventional manner; and in one embodiment a high level is equal to approximately five volts while a low level is equal to approximately zero volts. When transistor 26 is turned on by a high level signal on the line A_1 , the term line 28 is pulled down to ground potential, which potential is impressed upon the gate terminal of the transistor 36 thereby rendering transistor 38 ineffective. Thus, assuming no other term lines are at a high level, the output on the line O_1 in response to this single example would be a high level signal.

Referring now to Fig. 2, a typical flip-flop element is illustrated in detail. The data ("D") input terminal 50 is coupled to the source terminal of an MOS transistor 52 and the drain terminal thereof is coupled to the input terminal of an inverter 54. The gate terminal of the transistor 52 is coupled to the CK input terminal and is disposed for receiving phase 1 (ϕ_1) of the clock signal. A second inverter 56, which is scaled smaller than the inverter 54, is coupled in a reverse parallel arrangement with the inverter 54 so as to form a latch. The output of the inverter

54 is also coupled to the drain terminal of a second MOS transistor 58, and the source terminal thereof is coupled to the input of yet another inverter 60. The gate terminal of the transistor 58 is coupled to phase 2 (ϕ_2) of the clock signal. The output terminal of the inverter 60 is coupled to the flip-flop output terminal Q.

Before describing further the operation of the flip-flop circuit shown in Fig. 2, reference is made to the timing diagram of Fig. 3 wherein the operation of loading the PLA shift register is shown. Waveforms 64 and 65 illustrate phases 1 and 2, respectively, of the clock signal. Note that ϕ_2 is the complement of ϕ_1 . Waveform 66 depicts the input data "I" which is to be stored in the PLA shift register. Waveform 67 illustrates the fact that all address lines are to be held at a low level during the programming operation, and waveform 68 shows the outputs at a low level during this operation. Time t_p represents the end of the program mode of operation. Note that ϕ_1 remains low and ϕ_2 remains high after t_p .

Referring again to the flip-flop shown in Fig. 2, a high-level signal appearing on terminal 50 is transferred by the transistor 52 in response to the ϕ_1 clock signal to the input of the inverter 54 where it is inverted to a low-level signal. This low-level signal is transferred by the transistor 58 in response to the ϕ_2 clock signal to the input of the inverter 60 where it is inverted to a high-level signal at the output terminal Q. When the ϕ_1 signal is held low and the ϕ_2 signal is held high, the flip-flop will retain the last state. In other words, the circuit will store a high or low-level signal programmed therein since the input terminal 50 is isolated by the transistor 52 being turned off, and the output of the inverter 54 is coupled to the input of the inverter 60 by the transistor 58 being turned on.

Referring now to Fig. 4, a timing diagram of the operation of the PLA is briefly summarized. Similar reference numerals with a prime are used in Fig. 4 to represent the same waveforms shown in Fig. 3 and described above. Note that ϕ_1 (waveform 64') and I (waveform 66') are held at a low level while ϕ_2 is held at a high level. Note also that the address signals A_x (waveform 67') and the output signals (waveform 68') will vary as a function of the address supplied to the PLA 10 and the outputs extracted from the PLA.

It may be appreciated from the description above that a re-programmable logic array has been described in detail. Thus, while the invention has been particularly shown and described with reference to only one embodiment, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made without departing from the scope of the appended claims.

Claims

1. A re-programmable logic array (10) comprising:
 - a. an AND array (34) disposed for receiving n

transistor 26. The source terminal of the transistor 26 is coupled to a term line 28 which is also coupled to a power supply V_{cc} through a resistor R10. This biases the term line to a high-level voltage.

The gate terminal of the transistor 26 is coupled to an address line A_1 . The flip-flop 12-1 and the transistors 24 and 26 form a single cell of the AND array of the PLA 10, which is made up of a multiplicity of such cells arranged in an array of $2n \times m$ cells. Block 34 represents numerous additional such cells as that described above organized in a similar fashion and having address lines A_2 through A_n including the complements of these address lines ($\bar{A}_2$ through $\bar{A}_n$).

The term line 28 is also coupled to the gate terminal of a transistor 36, and the source terminal of this transistor is coupled to output line O_1 . The output line O_1 is biased at a high-level voltage by means of the V_{cc} voltage supply through a resistor R20. The drain terminal of the transistor 36 is coupled to the source terminal of a transistor 38 and the drain terminal of this transistor is coupled to ground potential. The gate terminal of the transistor 38 is coupled to the output terminal of the flip-flop 17-1.

The flip-flop 17-1 and the transistors 36 and 38 form a single cell of the OR array of the PLA 10, which OR array is arranged in an array of $k \times m$ cells. Block 40 represents numerous additional such cells organized in a similar fashion, and having output lines O_2 through O_k .

The above-described PLA is programmed by serially loading data into the shift register on the terminal 20 ("I"). That is, the input data "I" is supplied (one bit at a time) on the terminal 20 while a clock signal ("CK") is supplied on the terminal 22.

Assume that the output of the flip-flop 12-1 is at a high level, and the transistor 24 is turned on. The terms high and low level are used in a conventional manner; and in one embodiment a high level is equal to approximately five volts while a low level is equal to approximately zero volts. When transistor 26 is turned on by a high level signal on the line A_1 , the term line 28 is pulled down to ground potential, which potential is impressed upon the gate terminal of the transistor 36 thereby rendering transistor 38 ineffective. Thus, assuming no other term lines are at a high level, the output on the line O_1 in response to this single example would be a high level signal.

Referring now to Fig. 2, a typical flip-flop element is illustrated in detail. The data ("D") input terminal 50 is coupled to the source terminal of an MOS transistor 52 and the drain terminal thereof is coupled to the input terminal of an inverter 54. The gate terminal of the transistor 52 is coupled to the CK input terminal and is disposed for receiving phase 1 (ϕ_1) of the clock signal. A second inverter 56, which is scaled smaller than the inverter 54, is coupled in a reverse parallel arrangement with the inverter 54 so as to form a latch. The output of the inverter

54 is also coupled to the drain terminal of a second MOS transistor 58, and the source terminal thereof is coupled to the input of yet another inverter 60. The gate terminal of the transistor 58 is coupled to phase 2 (ϕ_2) of the clock signal. The output terminal of the inverter 60 is coupled to the flip-flop output terminal Q.

Before describing further the operation of the flip-flop circuit shown in Fig. 2, reference is made to the timing diagram of Fig. 3 wherein the operation of loading the PLA shift register is shown. Waveforms 64 and 65 illustrate phases 1 and 2, respectively, of the clock signal. Note that ϕ_2 is the complement of ϕ_1 . Waveform 66 depicts the input data "I" which is to be stored in the PLA shift register. Waveform 67 illustrates the fact that all address lines are to be held at a low level during the programming operation, and waveform 68 shows the outputs at a low level during this operation. Time t_p represents the end of the program mode of operation. Note that ϕ_1 remains low and ϕ_2 remains high after t_p .

Referring again to the flip-flop shown in Fig. 2, a high-level signal appearing on terminal 50 is transferred by the transistor 52 in response to the ϕ_1 clock signal to the input of the inverter 54 where it is inverted to a low-level signal. This low-level signal is transferred by the transistor 58 in response to the ϕ_2 clock signal to the input of the inverter 60 where it is inverted to a high-level signal at the output terminal Q. When the ϕ_1 signal is held low and the ϕ_2 signal is held high, the flip-flop will retain the last state. In other words, the circuit will store a high or low-level signal programmed therein since the input terminal 50 is isolated by the transistor 52 being turned off, and the output of the inverter 54 is coupled to the input of the inverter 60 by the transistor 58 being turned on.

Referring now to Fig. 4, a timing diagram of the operation of the PLA is briefly summarized. Similar reference numerals with a prime are used in Fig. 4 to represent the same waveforms shown in Fig. 3 and described above. Note that ϕ_1 (waveform 64') and I (waveform 66') are held at a low level while ϕ_2 is held at a high level. Note also that the address signals A_n (waveform 67') and the output signals (waveform 68') will vary as a function of the address supplied to the PLA 10 and the outputs extracted from the PLA.

It may be appreciated from the description above that a re-programmable logic array has been described in detail. Thus, while the invention has been particularly shown and described with reference to only one embodiment, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made without departing from the scope of the appended claims.

Claims

1. A re-programmable logic array (10) comprising:
 - a. an AND array (34) disposed for receiving n



input signals $A_1 \dots A_n$ on n rows of m cells per row;

b. an OR array (40) providing k output lines ($O_1 \dots O_k$) on k rows of m cells per row; wherein n , m and k are integers greater than one;

c. m term lines (28) coupling said cells of said AND array (34) to said cells of said OR array (40);

d. each of said rows of cells of said AND and said OR arrays (34, 40) including shift register means of m data storage elements (12-1, 12-2, ... 12- m , 14-1, 14-2, ... 14- m , 17-1, 17-2, ... 17- m), each storage element enabling or disabling in accordance with the binary value stored, a corresponding cell of the logic array (10), characterized by:

an input terminal (20) for programming said data storage elements with said binary value coupled to the first of said m data storage elements (12-1) and output terminals (Q) coupled to the output of the m th ones of said data storage elements (12- m , 14- m , 17- m) of each shift register, the output terminals (Q) of the first and of each of the subsequent row shift registers being coupled to the input terminals (D) of the next immediately following row shift register so as to form one continuous shift register through both said AND and said OR arrays (34, 40).

2. A re-programmable logic array (10) as in Claim 1 further characterized by each of said $n \times m$ cells in said AND array (34) comprising first and second transistor means (24, 26) coupled in series between one of said term lines (28) and a reference potential, each of said transistor means (24, 26) having a control element, one of said n input terminals (D) being coupled to the control element of said first transistor means and the output terminal of each of said data storage elements (12-1, 12-2, ... 12- m , 14-1, 14-2, ... 14- m) associated with the AND array being coupled to the control element of a corresponding one of said second transistor means (26).

3. A re-programmable logic array (10) as in Claim 1 further characterized by each of said $k \times m$ cells in said OR array (40) comprising third and fourth transistor means (36, 38) coupled in series between one of said output lines ($O_1 \dots O_k$) and a reference potential (V_{cc}), each of said transistor means (36, 38) having a control element, each of said m term lines (28) being coupled to the control element of a corresponding one of said third transistor (36) means and an output terminal of each of said data storage elements (17-1, 17-2, ... 17- m) associated with the OR array being coupled to the control element of said fourth transistor means.

4. A re-programmable logic array as in Claim 1 further characterized by a clock signal (CK) being coupled in parallel to each other of said data storage elements (12-1, 12-2, ... 12- m , 14-1, 14-2, ... 14- m , 17-1, 17-2, ... 17- m).

5. A re-programmable logic array as in Claim 1 further characterized by each of said data storage elements (12-1, 12-2, ... 12- m , 14-1, 14-2, ... 14- m , 17-1, 17-2, ... 17- m) being a flip-flop circuit.

Patentansprüche

1. Ein reprogrammierbares logisches Glied (10) mit

a. einem UND-Glied (34), das zum Empfang von n Eingangssignalen ($A_1 \dots A_n$) an n Reihen von m Zellen per Reihe angeordnet ist;

b. einem ODER-Glied (40), das k s Ausgangsleitungen ($O_1 \dots O_k$) an k Reihen von m Zellen der Reihe vorsieht; wobei n , m und k ganze Zahlen größer als eins sind;

c. mit m Verbindungsleitungen (28), welche die Zellen des UND-Gliedes (34) mit den Zellen des ODER-Gliedes koppeln;

d. wobei jede der Reihen von Zellen der UND- und der ODER-Glieder (34, 40) eine Schieberegistereinrichtung mit m Datenspeicherelementen (12-1, 12-2, ... 12- m , 14-1, 14-2, 14- m , 17-1, 17-2, ... 17- m) umfaßt, und jedes Speicherelement in Abhängigkeit mit dem gespeicherten binären Wert eine entsprechende Zelle des logischen Gliedes (10) freigibt oder sperrt, gekennzeichnet, durch:

einen Eingangsterminal (20) zum Programmieren der Datenspeicherelemente mit dem mit den ersten der m Datenspeicherelemente (12-1) gekoppelten binären Wert, und

durch Ausgangsterminals (Q), die mit dem Ausgang des m -ten der Datenspeicherelemente (12- m , 14- m , 17- m) jedes Schieberegisters gekoppelt ist, wobei die Ausgangsterminals (Q) des ersten und jedes der folgenden Reihen-Schieberegister mit den Eingangsterminals (D) des nächsten, unmittelbar folgenden Reihen-Schieberegisters gekoppelt sind, um durch sowohl die UND- wie auch die ODER-Glieder, (34, 40) ein kontinuierliches Schieberegister zu bilden.

2. Ein reprogrammierbares logisches Glied (10) nach Anspruch 1, dadurch gekennzeichnet, daß jede der $n \times m$ Zellen in dem UND-Glied (34) erste und zweite Transistoreinrichtungen (24, 26) umfaßt, die in Serie zwischen der Verbindungsleitung (28) und einem Bezugspotential gekoppelt sind, wobei jeder der Transistoreinrichtungen (24, 26) ein Kontrollelement aufweist, das einer der n -Eingangsterminals (D) mit dem Kontrollelement der ersten Transistoreinrichtung gekoppelt ist, und daß der Ausgangsterminal jedes der Datenspeicherelement (12-1, 12-2, ... 12- m , 14-1, 14-2, ... 14- m), das mit dem UND-Glied verbunden ist, mit dem Kontrollelement einer der entsprechenden zweiten Transistoreinrichtungen (26) gekoppelt ist.

3. Ein reprogrammierbares logisches Glied (10) nach Anspruch 1, dadurch gekennzeichnet, daß jede der $k \times m$ Zellen in dem ODER-Glied (40) dritte und vierte Transistoreinrichtungen (36, 38) umfaßt, die in Serie zwischen einer der Ausgangsleitungen ($O_1 \dots O_k$) und einem Bezugspotential (V_{cc}) gekoppelt sind, wobei jede der Transistoreinrichtungen (36, 38) ein Kontrollelement aufweist, jede der m Verbindungsleitungen (28) mit dem Kontrollelement eines entsprechenden der dritten Transistoreinrichtungen (36) gekoppelt ist, und daß ein Ausgangsterminal jedes der



Datenspeicherelemente (17-1, 17-2, ... 17-m), die mit dem ODER-Glied verbunden sind, mit dem Kontrollelement der vierten Transistoreinrichtungen verbunden sind.

4. Ein reprogrammierbares logisches Glied nach Anspruch 1, gekennzeichnet durch einen Taktgeber (CK) der parallel zu den jeweiligen Datenspeicherelementen (12-1, 12-2, ... 12-m, 14-1, 14-2, ... 14-m, 17-1, 17-2, ... 17-m) gekoppelt ist.

5. Ein reprogrammierbares logisches Glied nach Anspruch 1, dadurch gekennzeichnet, daß jedes der Datenspeicherelemente (12-1, 12-2, ... 12-m, 14-1, 14-2, ... 14-m, 17-1, 17-2, ... 17-m) ein FLIP-FLOP-Kreis ist.

Revendications

1. Réseau logique reprogrammable (10) comprenant:

a) un réseau ET (34) disposé pour recevoir n signaux d'entrée (A_1 ... A_n) sur n rangées de m cellules par rangée;

b) un réseau OU (40) fournissant k lignes de sortie (O_1 ... O_k) sur k rangées de m cellules par rangée, n, m et k étant des entiers plus grands que 1;

c) m lignes de terme (28) reliant lesdites cellules dudit réseau ET (34) auxdites cellules dudit réseau OU (40);

d) chacune desdites rangées de cellules desdits réseaux ET et OU (34, 40) comprenant des registres à décalage de m éléments de stockage de données (12-1, 12-2, ... 12-m, 14-1, 14-2, ... 14-m, 17-1, 17-2, 17-m), chaque élément de stockage validant ou invalidant, en fonction de la valeur binaire stockée, une cellule correspondante du réseau logique (10), caractérisé par une borne d'entrée (20) pour programmer lesdits éléments de stockage de données avec ladite valeur binaire reliée au premier desdits m éléments de stockage de données (12-1) et des bornes de sortie Q reliées à la sortie des m^{èmes} desdits éléments de stockage de données (12-m, 14-m, 17-m) de chaque registre à décalage, les bornes de sortie (Q) du premier et de chacun des registres à décalage des rangées suivantes étant reliées aux bornes

d'entrée (D) du registre à décalage de la rangée immédiatement suivante, de manière à constituer un registre à décalage continu à travers à la fois ledit réseau ET et ledit réseau OU (34, 40).

2. Réseau logique reprogrammable (10) suivant la revendication 1, caractérisé en outre en ce que chacune desdites $n \times m$ cellules dans ledit réseau ET (34) comprend un premier et un deuxième transistors (24, 26) reliés en série entre l'une desdites lignes de terme (28) et un potentiel de référence, chacun desdits transistors (24, 26) comportant un élément de commande, l'une desdites bornes d'entrée (D) étant reliée à l'élément de commande dudit premier transistor et la borne de sortie de chacun desdits éléments de stockage de données (12-1, 12-2, ... 12-m, 14-1, 14-2, ... 14-m) associés au réseau ET étant reliée à l'élément de commande d'un transistor correspondant desdits deuxièmes transistors (26).

3. Réseau logique reprogrammable (10) suivant la revendication 1, caractérisé en outre en ce que chacune desdites $k \times m$ cellules dans ledit réseau OU (40) comprend un troisième et un quatrième transistors (36, 38) reliés en série entre l'une desdites lignes de sortie (O_1 ... O_k) et un potentiel de référence (V_{cc}), chacun desdits transistors (36, 38) ayant un élément de commande, chacune desdites m lignes de terme (28) étant reliées à l'élément de commande d'un transistor correspondant desdits troisièmes transistors (36), et une borne de sortie de chacun desdits éléments de stockage de données (17-1, 17-2, ... 17-m) associés au réseau OU étant reliée à l'élément de commande desdits quatrièmes transistors.

4. Réseau logique reprogrammable suivant la revendication 1, caractérisé en outre en ce qu'un signal d'horloge (CK) est relié en parallèle à chacun desdits éléments de stockage de données (12-1, 12-2, ... 12-m, 14-1, 14-2, ... 14-m, 17-1, 17-2, ... 17-m).

5. Réseau logique reprogrammable suivant la revendication 1, caractérisé en outre en ce que chacun desdits éléments de stockage de données (12-1, 12-2, ... 12-m, 14-1, 14-2, ... 14-m, 17-1, 17-2, ... 17-m) est un circuit de bascule bistable.

