

RECESSED AND EMBEDDED DIE CORELESS PACKAGE

BACK GROUND OF THE INVENTION

As semiconductor technology advances for higher processor performance,
5 advances in packaging architectures may include package-on-package (PoP) architecture
and other such assemblies. As the design of package structures becomes more complex,
there is often a resulting increase in assembly expense. Thus there is a need to
significantly lower package and assembly costs for advanced package structures.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and
distinctly claiming certain embodiments of the present invention, the advantages of this
invention can be more readily ascertained from the following description of the invention
when read in conjunction with the accompanying drawings in which:

15 FIGS. 1a-1m represent methods of forming structures according to an embodiment
of the present invention.

FIG. 2 represents a system according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

20 In the following detailed description, reference is made to the accompanying
drawings that show, by way of illustration, specific embodiments in which the invention
may be practiced. These embodiments are described in sufficient detail to enable those
skilled in the art to practice the invention. It is to be understood that the various
embodiments of the invention, although different, are not necessarily mutually exclusive.
25 For example, a particular feature, structure, or characteristic described herein, in
connection with one embodiment, may be implemented within other embodiments without
departing from the spirit and scope of the invention. In addition, it is to be understood that
the location or arrangement of individual elements within each disclosed embodiment may
be modified without departing from the spirit and scope of the invention. The following
30 detailed description is, therefore, not to be taken in a limiting sense, and the scope of the
present invention is defined only by the appended claims, appropriately interpreted, along
with the full range of equivalents to which the claims are entitled. In the drawings, like
numerals refer to the same or similar functionality throughout the several views.

Methods and associated structures of forming and utilizing a microelectronic structure, such as a package structure, are described. Those methods may comprise forming a cavity in a plating material to hold a die, attaching the die in the cavity, forming a dielectric material adjacent to the die, forming vias in the dielectric material adjacent the die, forming PoP lands in the vias, forming interconnects in the vias, and then removing the plating material to expose the PoP lands and die. Methods of the present invention enable the fabrication of package-on-package architectures such as PoP assemblies comprising partially recessed and/or fully embedded die or any other type of ball grid array (BGA) package.

FIGS. 1a-1m illustrate embodiments of a method of forming a microelectronic structure, such as a package structure, for example. FIG. 1a illustrates a material 100. In one embodiment, the material 100 may comprise a plating material, such as but not limited to a copper foil plating material, for example. In some embodiments, any suitable plating material may be utilized, depending upon the particular application. In FIG. 1b, a cavity 102 may be formed in the material 100. The cavity 102 may be formed utilizing any suitable etching process in some embodiments, such as are known in the art. In an embodiment, the cavity 102 may be formed such that the cavity 102 may hold a die, such as a microelectronic die, for example. The cavity 102 may comprise a bottom portion 101 an angled portion 103, and a top portion 105. In an embodiment, the bottom and top portions may be separated by a barrier layer to aid in the formation of the cavity structure, especially for an etching process. In an embodiment (not shown), PoP land structures (to be described further herein) can be formed on surface 101.

In an embodiment, a die 104 may be attached within the cavity 102 (FIG. 1c). In an embodiment, the die 104 may comprise a thin die 104, and may comprise a thickness of below about 150 microns. In an embodiment, the die 104 may be attached to the top portion 105 of the cavity 101. In an embodiment, the die 104 may comprise at least one sidewall 106, a top side 107 and a bottom/active side 108. In some cases, an adhesive film and/or an attach process may be used to attach the die 104 into the cavity 102 of the plating material 100. In an embodiment, the adhesive film (not shown), can be used as a permanent part of a final package to protect the die backside, to provide a surface for marking, and/or manage any warpage that may occur within the die 104, for example. A dielectric material 110 may be formed on the plating material 100 and adjacent the die 104 that is in the cavity 102 of the plating material 100 (FIG. 1d). In an embodiment, the

dielectric material 110 may be formed by a laminating process, for example. The dielectric material 110 may be formed on the bottom portion 101 of the cavity 102, on the angled portion 103 of the cavity 102, and on a portion of the top portion 105 of the cavity 102 of the plating material 100 that surrounds the die 104. Vias 112 may be formed in a region 114 of the dielectric material 110 adjacent the die 104 (FIG. 1e). In an embodiment, a package on package (PoP) land area 113 may be formed within the via 112, wherein a portion of the plating material 100 may be removed to form the PoP land area 113. In an embodiment, the plating material 100 and the dielectric material 110 may be removed using any suitable etching process.

In an embodiment, a PoP land structure 116 may be formed in the PoP land area 113 (FIG. 1f). The PoP land structure 116 may be formed in the PoP land area 113 by using an electrolytic plating process, for example, however any suitable process may be utilized to form the PoP land structure 116. In an embodiment, the plating material 100 within the PoP land area 113 may be used as a plating bus for the formation of the PoP land structure 116. In an embodiment, the plating material 100 may comprise a copper foil that may be used as a plating bus. In some cases, plating metallurgies may include gold, nickel, gold/nickel, gold/nickel/palladium, and the similar suitable materials, according to the particular application. In an embodiment, wire bond pads may be plated on the PoP land area 113, allowing for a mixed-technology stacking on a CPU die backside, for example.

In an embodiment, vias 118 may be formed in a die area 119, wherein die pads, for example copper die pads, maybe exposed on the active side 108 of the die 104 (FIG. 1g). The vias 112 adjacent the PoP land structures 116 (those located in the dielectric region 114) and the vias 118 in the die area 119 may be plated with a metallic material (FIG. 1h) to form PoP land structure 116 interconnect structures 117 and to form die pad interconnect structures 120. In an embodiment, the PoP land interconnect structure 117 may be electrically connected to the PoP land structure 116, and the die pad interconnect structure 120 may be electrically connected to die pads on the active side 108 of the die 104.

In an embodiment, a semi-additive process (SAP) may be used to form the die pad interconnect structures 120 and the PoP interconnect structures 118. In some embodiments, the die pad interconnect structures 120 and the PoP interconnect structures 118 may be formed in the same process step, or in other embodiments, the die pad

interconnect structures 120 and the PoP interconnect structures 118 may be formed in separate formation steps. A second dielectric layer 110' may be formed on the die pad interconnect structures 120 and the PoP interconnect structures 118 (FIG. 1i). A first metallization layer 121 may be formed in the second dielectric layer 110'.

5 Subsequent layers may then be formed using standard substrate SAP build-up processing, for example, wherein further dielectric layers 120'' and metallization layers 121' may be formed upon each other to form a coreless substrate 125 by utilizing a buildup process (FIG. 1j). The plating material 100 may then be removed from the die 104 and the PoP land structures 116 of the coreless substrate 125, exposing the PoP lands and
10 the die, to form a coreless package structure 126 (FIG. 1k). The coreless package structure 126 may comprise a fillet structure 127 of dielectric material 110 around the die 104, wherein the dielectric material 110 may surround the sidewall 106 and the bottom 108 of the die 104, but wherein the dielectric material 110 is absent on the top side 107 of the die 104.

15 The fillet structure 127 may comprise a portion of the dielectric 110 that may be angled/raised in relation to a planar top portion 111 of the dielectric 110 of the coreless substrate 125. The geometry of this fillet structure 127 can be optimized to provide maximum reliability of the die/package, wherein an angle 128 of the fillet structure 127 may be varied to optimize reliability. In an embodiment, the angle of the fillet structure
20 may comprise about 70 degrees or less, but may be varied according to the application.

 In an embodiment, the coreless package structure 126 may comprise the die 104 being at least partially embedded in the coreless substrate 125. In other embodiments, the coreless package structure 126 may comprise the die 104 being substantially entirely embedded in the coreless substrate 125. In some embodiments, the top side 107 of the die
25 104 may be substantially coplanar with the top portion 111 of the dielectric 110. In another embodiment, there may be a distance 129 between the top side 107 of the die 104 and a top side 131 of the PoP land 116.

 The coreless package structure 126 may comprise package interconnect structures areas 122, wherein interconnect structures 124, such as ball grid array (BGA) balls, may
30 be attached (FIG. 1l). The PoP land structures 116 of the coreless package structure 126 may comprise raised, electrolytically plated lands 116 disposed on top of the coreless substrate 125, thus enabling the attachment of another package on top of the coreless package structure 126 (e.g. Package-on-Package structure).

FIG. 1m depicts a PoP structure 130, wherein a second package 132 is connected to the coreless package structure 126 by attachment to the PoP land structures 116. In an embodiment, the second package 132 may comprise a die 104' that is directly above the die 104 of the coreless package structure 126. Interconnect balls 124' of the second package 132 may be attached to the PoP land structures 116 of the coreless package structure 126.

FIG. 2 is a diagram illustrating an exemplary system 200 capable of being operated with methods for fabricating a microelectronic structure, such as the coreless package structure 126 of FIG. 11, for example. It will be understood that the present embodiment is but one of many possible systems in which the coreless package structures of the present invention may be used.

FIG. 2 shows a computer system according to an embodiment of the invention. System 200 includes a processor 210, a memory device 220, a memory controller 230, a graphics controller 240, an input and output (I/O) controller 250, a display 252, a keyboard 254, a pointing device 256, a peripheral device 258, and a bus 260. Processor 210 may be a general purpose processor or an application specific integrated circuit (ASIC). I/O controller 250 may include a communication module for wired or wireless communication. Memory device 220 may be a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a flash memory device, or a combination of these memory devices. Thus, in some embodiments, memory device 220 in system 200 does not have to include a DRAM device.

One or more of the components shown in system 200 may be included in one or more integrated circuit packages, such as the coreless package structure 126 of FIG. 11 for example. For example, processor 210, or memory device 220, or at least a portion of I/O controller 250, or a combination of these components may be included in an integrated circuit package that includes at least one embodiment of a structure described in FIGS. 1a-1m.

System 200 may include computers (e.g., desktops, laptops, hand-helds, servers, Web appliances, routers, etc.), wireless communication devices (e.g., cellular phones, cordless phones, pagers, personal digital assistants, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, camcorders, digital cameras, MP3 (Motion Picture Experts Group, Audio Layer 3) players, video games,

watches, etc.), and the like.

Benefits of the present invention enable a new packaging architecture that can meet design requirements for future mobile/handheld system on a chip (SoC) processors at roughly half the cost of current package architectures. Embodiments provide a method of
5 embedding a die in a substrate, which enables the elimination of many assembly processes. Embodiments enable thin die assembly, PoP compatibility, substrate design rule scalability, package thickness reduction, and package/assembly cost reduction. In addition, the substrate is no longer confined to strip manufacturing capability, which enables full panel processing, which also reduces costs.

10 Although the foregoing description has specified certain steps and materials that may be used in the method of the present invention, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the invention as defined by the appended claims. In addition, it is
15 appreciated that various microelectronic structures, such as package structures, are well known in the art. Therefore, the Figures provided herein illustrate only portions of an exemplary microelectronic device that pertains to the practice of the present invention. Thus the present invention is not limited to the structures described herein.

IN THE CLAIMS

What is claimed is:

1. A method comprising;
 - 5 forming a cavity in a plating material;
 - attaching a die in the cavity;
 - forming a dielectric material adjacent the die;
 - forming vias in a region of the dielectric material adjacent the die;
 - forming PoP land areas within the vias;
 - 10 forming PoP land structures in the PoP land areas;
 - forming vias in the die area to expose die pads on the die;
 - forming die pad interconnect structures in the die area vias and
 - forming PoP interconnect structures in the dielectric region vias; and
 - removing the plating material to expose the die and the PoP land
 - 15 structures.
2. The method of claim 1 further comprising forming subsequent metal layers on the die pad interconnect structures and on the PoP interconnect structures to form a coreless substrate.
3. The method of claim 2 further comprising wherein the die is partially
- 20 embedded into the coreless substrate, and wherein the dielectric material is formed along a portion of a sidewall of the die.
4. The method of claim 2 further comprising wherein the die is substantially fully embedded into the coreless substrate, and wherein the dielectric material is formed along a portion of a sidewall of the die.
- 25 5. The method of claim 1 further comprising wherein a portion of the dielectric material comprises a fillet structure surrounding a portion of the sidewall of the die.
6. The method of claim 5 further comprising wherein an angle is between a raised portion of the fillet structure and a planar top portion of the dielectric
- 30 material.
7. The method of claim 2 further comprising wherein the PoP land structures comprise raised, electrolytically plated lands on top of the coreless package.
8. The method of claim 1 further comprising wherein interconnect structures

of a second package are attached to the PoP land structures.

9. A method comprising:

forming a cavity in a plating material to hold a die;
attaching the die in the cavity;
5 forming a dielectric material adjacent the die;
forming vias in the dielectric material adjacent the die;
forming PoP lands in the vias;
forming interconnects in the vias; and
removing the plating material to expose the PoP lands and die,

10 wherein the die is disposed above the PoP lands.

10. The method of claim 9 further comprising wherein the die is attached using an adhesive film.

11. The method of claim 9 further comprising wherein the plating material comprises an electroplating metal.

15 12. The method of claim 11 wherein forming the PoP lands in the vias further comprises forming wire bond pads in the vias.

13. The method of claim 9 further comprising wherein forming the PoP lands in the vias comprises using the plating material as the plating bus to form the PoP lands.

20 14. The method of claim 9 further comprising:
forming vias in a die area, exposing pads on the die; and
plating the vias in the die area.

15. The method of claim 14 further comprising wherein a coreless substrate is built up on the PoP lands and on the plated die vias.

25 16. A structure comprising:

a partially embedded die disposed in a coreless substrate; and
raised PoP lands adjacent the die on top of the coreless substrate,
wherein the PoP lands are capable of receiving a second substrate.

30 17. The structure of claim 16 further comprising an adhesive film disposed on a top surface of the die, and wherein the coreless substrate comprises a portion of a POP package structure.

18. The structure of claim 16 wherein the coreless substrate comprises a portion of a PoP package structure, and further wherein interconnect structures of a

second package are disposed on the the PoP lands of the coreless substrate.

19. The structure of claim 16 wherein the die comprises a dielectric fillet structure surrounding the sidewall of the die.

5 20. The structure of claim 19 wherein there is an angle between a planar top portion of the dielectric material of the coreless substrate and the dielectric fillet structure.

21. The structure of claim 18 wherein a die of the second package is directly above the die of the coreless substrate

10 22. The structure of claim 16 wherein there is a distance between a top side of the die and a top side of the PoP land.

23. A structure comprising:

a die disposed in a coreless substrate, wherein at least a portion of the die is embedded in the coreless substrate;

15 raised PoP lands adjacent the die, wherein the PoP lands and the die are capable of receiving a second substrate;

a dielectric film adjacent the die, wherein die interconnect structures are disposed in the dielectric film and are connected to pads of the die;

20 PoP interconnect structures that are connected to the PoP lands; and a first metal layer disposed on the PoP interconnect structures and on the die interconnect structures.

24. The structure of claim 23 wherein a portion of the dielectric material is adjacent a sidewall of the die and raised above a top side of the PoP lands.

25. The structure of claim 23 wherein the PoP lands comprise plated metal.

25 26. The structure of claim 23 wherein the structure comprises a portion of coreless package structure, wherein a second package is connected to the coreless package structure.

27. The structure of claim 26 wherein interconnect structures of the second package are connected to the PoP lands of the coreless package structure.

30 28. The structure of claim 24 wherein there is an angle between a top planar portion of the dielectric material of the coreless package and the dielectric material adjacent the sidewall of the die.

29. The structure of claim 23 wherein the die comprises a thickness of less than

about 150 microns.

30. The structure of claim 23 further comprising a system comprising:
a bus communicatively coupled to the structure; and
a DRAM communicatively coupled to the bus.

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