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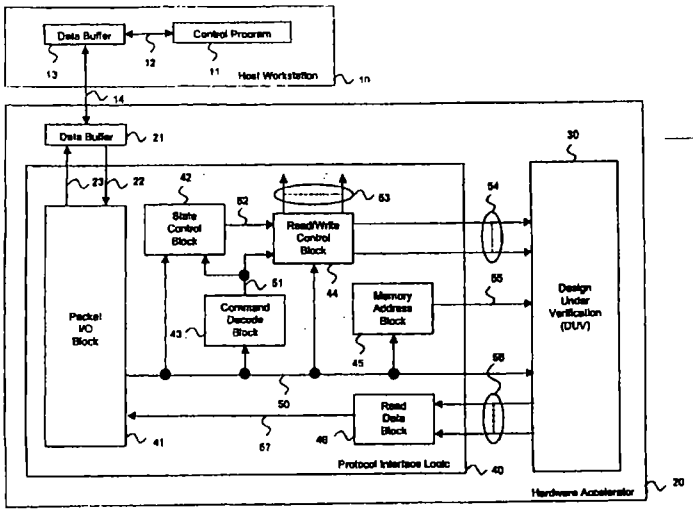
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(54) Title: HARDWARE-ASSISTED DESIGN VERIFICATION SYSTEM USING A PACKET-BASED PROTOCOL LOGIC SYNTHESIZED FOR EFFICIENT DATA LOADING AND UNLOADING



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ACTION

(57) Abstract: A system is prvided to increase the accessibility of registers and memories in a user's design undergoing functional verificationin a hardware-assisted design verification system. A packet-based protocol is used to perform data transfer operations between a host workstation and ahardware accelerator for loading data to and unloading data from the registers and memories in a target design under verification (DUV) during logic simulation. The method and apparatus synthesizes interface logic into the DUV to provide for greater access to the registers and memories in the target DUV which is simulated with the assistance of the hardware accelerator.

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