

Description

The invention relates to an amplifier arrangement comprising an input terminal for receiving an input voltage, an output terminal for supplying an output voltage which is an amplified version of the input voltage, a first amplifier having a first transistor coupled to the output terminal for producing at the output terminal a first output voltage up to a maximum first voltage value, the first amplifier being coupled between a first and a second supply voltage terminal.

Such an amplifier arrangement can be used for amplifying a signal in electronic circuits, such as integrated audio amplifier circuits.

An amplifier arrangement of this type is known inter alia from the second edition of the book "Analysis and design of analog integrated circuits" by P. Gray and R. Meyer. In Figure 3.8a on page 175 this book shows a transistor having a base, emitter and collector, an input signal being applied to the base and the supply voltage terminals being coupled to the emitter and collector. The output voltage is taken from the collector, which is therefore coupled to the associated supply-voltage terminal by means of a resistor. A drawback of such an amplifier arrangement is that in the case of integration the maximum output voltage of the transistor is dictated by the fabrication process. If this maximum voltage value is exceeded this will be disastrous to the amplifier. Therefore, the output voltage of the amplifier is limited to the maximum voltage value. Generally, the voltage difference between the two supply-voltage terminals is selected to be smaller than said maximum voltage value, so that the output voltage cannot cause damage to the amplifier. However, if the voltage difference is selected to be larger than the maximum voltage value the fabrication process will impose limitations on the output voltage of the amplifier arrangement.

It is an object of the invention to provide an amplifier arrangement which is capable of supplying an output voltage larger than the maximum voltage value imposed on the output voltage of the amplifier by the fabrication process, the voltage difference between the two supply-voltage terminals being chosen so as to enable a larger output voltage to be obtained.

An amplifier arrangement in accordance with the invention is characterized in that the amplifier arrangement further comprises a second amplifier having a series arrangement of a second and a third transistor, the series arrangement being coupled to the output terminal for producing at the output terminal a second output voltage up to a maximum second voltage value, the second amplifier also being coupled between the first and the second supply voltage terminal, and means for driving the first and the second amplifier with a first and second drive signal respectively, the sum of the first and second drive signal being proportional to the input signal and the ratio between the first and second drive signal being dependent on the difference between the actual output voltage

value at the output terminal and the first voltage value.

The invention, as defined by the appended claims, is based on the recognition of the fact that the amplification of the input signal is taken over by the second amplifier when the resulting output voltage tends to exceed the maximum voltage value of the first amplifier. The means ensure a gradual cross-over between the first and the second amplifier. The first amplifier is adapted to supply comparatively small output voltages at large currents and the second amplifier is adapted to supply comparatively small output currents at large voltages. For this purpose, the second amplifier comprises two serially coupled transistors, which together can generate the comparatively large output voltages at small currents. The amplifier arrangement can therefore supply a maximum output voltage which is related to the voltage difference between the two supply-voltage terminals.

An embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the means comprise a differential pair comprising a fourth and a fifth transistor each having a base for receiving a first portion of the output voltage and a first reference voltage respectively, having mutually coupled emitters for receiving a portion of the input signal, and each having a collector for driving the first amplifier and the second amplifier respectively. The differential pair compares a fraction of the output voltages with the first reference voltage, which comparison results in two complementary representations of the input signal, i.e. the first and the second signal respectively. The first reference voltage then dictates the instant of take-over.

A further embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the means further comprise a current regulator. The current regulator serves to minimize the cross-over distortion of the signals. This is achieved by maintaining the bias currents of the first and the second amplifier constant when these amplifiers are operative. For this purpose the current regulator will extract currents from the first main electrodes of the first and the second transistor, which currents are inversely proportional to the degree of conduction of said transistors.

Yet another embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the second and the third transistor each have a base coupled respectively to the means and to a terminal for receiving a third measure of the output voltages. One transistor receives its drive via the means and the other transistor receives its drive from the output voltages. Cascoding allows a higher voltage to be obtained across the two transistors, so that a larger output signal is possible. In this case the single transistor in the first amplifier, as is illustrated in the above example, will supply low voltages at large currents and the cascoded transistors in the second amplifier will supply high voltages at small currents.

The invention will now be described in more detail, by way of example, with reference to the accompanying

drawings in which

Fig. 1 is a basic diagram of an amplifier arrangement in accordance with the invention,

Fig. 2 shows a first embodiment of an amplifier arrangement in accordance with the invention,

Fig. 3 shows a second embodiment of an amplifier arrangement in accordance with the invention,

Fig. 4 shows an extension of the above embodiments of an amplifier arrangement in accordance with the invention, and

Fig. 5 shows an example of a current regulator for an amplifier arrangement in accordance to the invention.

In the Figures like parts bear the same reference numerals.

Fig. 1 is a basic diagram of an amplifier arrangement in accordance with the invention. The arrangement has an input terminal I for receiving an input signal V_{in} and an output terminal U for supplying an output signal V_{uit} , a first amplifier A1 having an input terminal i1 and an output terminal u1, a second amplifier A2 having an input terminal i2 and an output terminal u2, and means M having an output terminal u3 and an output terminal u4. The amplifier A1 is constructed to amplify the input signal V_{in} up to a maximum first voltage value and the amplifier A2 up to a maximum second voltage value. The means M are coupled to the input terminal I and to the output terminal U, to which in addition the output terminals u1 and u2 are connected. The output terminals u3 and u4 are coupled to the input terminals i1 and i2 respectively. The means M generate a first signal on the output terminal u3 and a second signal on the output terminal u4, which signals are complementary to one another and serve to drive the amplifier A1 and the amplifier A2 respectively. The signals are measures of the input signal V_{in} and, in addition, they depend upon the output signal V_{uit} in relation to the maximum voltage values of the output signals of amplifiers A1 and A2. These output signals together constitute the output signal V_{uit} . The means M apply an input signal V_{in} which results in an output signal V_{uit} smaller than the first maximum voltage value to the amplifier A1 as the first signal. The amplifier A2 then receives no drive, so that the second signal is zero. Consequently, the output signal is constituted by the output signal of the amplifier A1. As the input signal V_{in} increases and the output signal V_{uit} consequently tends to exceed the first maximum voltage value the drive to the amplifier A1 will decrease and that to the amplifier A2 will increase. The output signals of the two amplifiers A1 and A2 now form the output signal V_{uit} . As the input signal V_{in} increases further the drive to the amplifier A1, i.e. the first signal, will have become zero before the output signal V_{uit} exceeds the first maximum voltage value. The means M then generate only the second signal, which drives the amplifier A2. Consequently, the output signal V_{uit} is formed by the output signal of the amplifier A2.

When the second maximum voltage value associated with the amplifier A2 is larger than the supply voltage difference this will ensure that the amplifier cannot be damaged.

Fig. 2 shows a first embodiment of an amplifier arrangement in accordance with the invention. The first amplifier A1 comprises a transistor N1 having its control electrode coupled to the input terminal i1, having its first main electrode coupled to a supply-voltage terminal V_{ss} , and having its second main electrode coupled to the output terminal u1. The second amplifier A2 comprises a transistor N2 having its control electrode coupled to the input terminal i2 and having its first main electrode coupled to the supply-voltage terminal V_{ss} , and a transistor N3 having its control electrode coupled to a terminal 3 to receive a measure V_{uit2} of the output voltage V_{uit} , having its first main electrode coupled to the main electrode of the transistor N2 and having its second main electrode coupled to the output terminal u2. The other elements constitute the means M, which are coupled to the two amplifiers A1 and A2 in a way similar to that shown in Fig. 1. A transistor P1 and a transistor P2, which form part of the means M, constitute a degenerated differential pair, for which purpose they have their first main electrodes coupled to a terminal 4 and a terminal 5 respectively, which terminals are coupled to each other by a parallel arrangement of a diode D1 and a resistor R1 in series with another parallel arrangement of a diode D2 and a resistor R2. The node common to the two parallel arrangements is coupled to the second main electrode of a transistor P3, whose first main electrode is coupled to a supply-voltage terminal V_{dd} and whose control electrode is coupled to the input terminal I. Moreover, the transistor P1 has its control electrode coupled to a terminal 1 to receive a measure V_{uit1} of the output voltage V_{uit} and has its second main electrode coupled to the output terminal u3, which is also connected to the supply-voltage terminal V_{ss} by a resistor R3. The transistor P2 further has its control electrode coupled to a terminal 2 to receive a reference voltage V_{ref1} and has its second main electrode coupled to the output terminal u4, which is also connected to the supply-voltage terminal V_{ss} by a resistor R4. The means M further comprise a current regulator S, which is coupled to the terminals 4 and 5 and to the output terminals u3 and u4. The function of this regulator S is to maintain the bias currents and hence the transconductances of the amplifiers A1 and A2 constant when these are operative. This precludes unnecessary cross-over distortion. The resistors R1 and R2 provide a gradual cross-over between the transistors P1 and P2, the diodes D1 and D2 limiting the voltage drops across these resistors. The resistors R3 and R4 limit the control electrode currents of the transistors N1 and N2. The circuit is driven by the input signal V_{in} applied to the input terminal I. This input signal V_{in} is transferred to the differential pair P1 and P2 via the transistor P3. The magnitude of the measure V_{uit1} of the output signal V_{uit} in relation to the reference voltage V_{ref1} dictates the de-

gree of conduction of the transistors P1 and P2. In the case of an input signal V_{in} resulting in a measure V_{uit1} of the output signal V_{uit} , which relative to the supply-voltage terminal V_{ss} is smaller than the reference voltage V_{ref1} , the transistor P1 will conduct and the transistor P2 will be cut off. How the measure V_{uit1} can be obtained will be described with reference to Fig. 4. On the basis of the fabrication process the reference voltage V_{ref1} is selected in such a way that the output signal of the first amplifier does not exceed the first voltage value and the output signal of the second amplifier does not exceed the second voltage value. The input signal V_{in} will then produce the first signal on the output terminal $u3$ via the transistor P3, the diode D1, the resistor R1 and the transistor P1. This signal drives the amplifier A1 via the control electrode of the transistor N1. The second amplifier A2 does not receive any drive via the control electrode of the transistor N2, so that this transistor is not conductive. Consequently, the transistor N3 will neither be conductive, although this transistor is driven by the measure V_{uit2} of the output signal V_{uit} via its control electrode, which measure is obtained, for example, by means of a voltage divider. As the input signal V_{in} increases and the measure V_{uit1} tends to become equal to the reference voltage V_{ref1} , the transistor P2 will be driven into conduction and the transistor P1 will become less conductive. The second signal on the output terminal $u4$ will then also increase, causing the second amplifier to be driven via the control electrode of the transistor N2. In this situation the current regulator S ensures that both amplifiers have equal bias currents. As the input signal V_{in} increases further the transistor P1 will be cut off, while the transistor P2 will be fully conductive. Consequently, the transistor N1 will no longer receive any drive, so that the currents in this transistor will be zero. In contrast, the transistors N2 and N3 are now both conductive. The transistor N2 is then driven by the second signal, which is derived from the input signal V_{in} via the transistor P2, the diode D2, the resistor R2 and the transistor P3. The transistor N3 is still driven by the measure V_{uit2} of the output signal V_{uit} and is now turned on because the transistor N2 conducts. The operation of this arrangement will become apparent from the description of the following versions of the two amplifiers. The amplifier A1 comprises a transistor N1, which is capable of supplying comparatively large output currents at low voltages and which has a maximum voltage value dictated by the selected fabrication process. The amplifier A2 comprises a cascode pair comprising a transistor N2 and a transistor N3, which together are capable of supplying comparatively high output voltages at small currents. The two amplifiers supplement one another in such a way that the entire amplifier arrangement has a larger output swing than the individual amplifiers.

Fig. 3 shows a second embodiment of an amplifier arrangement in accordance with the invention. This arrangement is largely identical to the arrangement shown in Fig. 2, i.e. the diodes D1 and D2, the resistors R1 and

R2 and the transistor P3 have been replaced. The terminals 4 and 5 are now coupled to one another by a parallel arrangement of a diode D3, a diode D4 and a resistor R5. Moreover, two transistors P4 and P5 have been added whose control electrodes are coupled to the input terminal 1, whose first main electrodes are coupled to the supply-voltage terminal V_{dd} and whose second main electrodes are coupled to the terminals 4 and 5 respectively. This embodiment, which enables an integrable resistor to be dispensed with, operates in a way equivalent to that of the arrangement described with reference to Fig. 2. The input signal V_{in} drives the transistors P4 and P5, which activate the degenerate differential pair P1 and P2 by means of the resistor R5. The diodes D3 and D4 again serve to limit the voltage across the resistor R5.

Fig. 4 shows an extension of the above embodiments of an amplifier arrangement in accordance with the invention. A transistor N4 and a transistor N5 are arranged in parallel, their first main electrodes being coupled both to the supply-voltage terminal V_{ss} by a resistor R6 and to the terminal 1 and their second main electrodes being connected to the supply-voltage terminal V_{dd} . The control electrode of the transistor N4 is coupled both to a terminal 6 for receiving a measure V_{uit3} of the output voltage V_{uit} and to the supply voltage V_{ss} by means of a zener diode D_z . The measure V_{uit3} can be obtained by means of a voltage divider. The control electrode of the transistor N5 is connected to a terminal 7 for a reference voltage V_{ref2} . This arrangement limits the measure V_{uit1} of the output signal V_{uit} to substantially the reference voltage V_{ref2} in order to keep the transistor P1 out of saturation for the purpose of driving the amplifier A1. Moreover, the measure V_{uit3} of the output voltage V_{uit} is limited by the zener diode D_z in order to prevent the occurrence of excessively large signals.

Fig. 5 shows an example of a current regulator for an amplifier arrangement in accordance with the invention. A transistor N6 and a transistor N7 are coupled to each other via their first main electrodes and their control electrodes, which control electrodes are also coupled to a reference-voltage circuit. The second main electrodes of the transistors N6 and N7 are coupled to the terminals 4 and 5 respectively. A transistor P6 and a transistor P7 constitute a differential pair, the first main electrodes being coupled to each other and being connected to the first main electrodes of the transistors N6 and N7 by a resistor R7, the second main electrodes being coupled to the supply-voltage terminal V_{ss} , and the control electrodes being coupled to the output terminals $u3$ and $u4$ respectively. The reference-voltage circuit is coupled between the supply voltages V_{dd} and V_{ss} and comprises a series arrangement of a current source J1 and three diode-connected transistors N8, N9 and P8 respectively. The transistor N8 has its control electrode and its second main electrode coupled to both the current source J1 and the control electrodes of the transistors N6 and N7, and has its first main electrode coupled to the control electrode and the second main electrode of the transistor N9,

whose first main electrode is connected to the first main electrode of the transistor P8. The reference-voltage circuit provides the bias voltage for the transistors N6 and N7, the differential pair P6 and P7 dictating the magnitude of the currents depending on the voltages on the output terminals u3 and u4. These currents ensure that the bias currents applied to the active amplifier of the amplifiers A1 and A2 constantly have substantially constant values to stabilize the corresponding transconductances. This minimizes the cross-over distortion. Equal voltages on the output terminals u3 and u4 will give rise to equal currents through the transistors N6 and P6 and through the transistors N7 and P7. Unequal voltages on the output terminals u3 and u4, however, will give rise to unequal currents through the transistors P6 and P7, while the currents through the transistors N6 and N7 remain equal to each other. The magnitudes of the currents are dictated by the voltage difference between the control electrodes of the transistors N6 and N7 on the one hand and the output terminals u3 and u4 on the other hand.

In the embodiments disclosed herein, it is also possible to use unipolar transistors.

Claims

1. An amplifier arrangement comprising an input terminal (I) for receiving an input voltage, an output terminal (U) for supplying an output voltage which is an amplified version of the input voltage, a first amplifier (A1) having a first transistor (N1) coupled to the output terminal (U) for producing at the output terminal (U) a first output voltage up to a maximum first voltage value, the first amplifier being coupled between a first (V_{dd}) and a second (V_{ss}) supply voltage terminal, characterized in that the amplifier arrangement further comprises a second amplifier (A2) having a series arrangement of a second (N2) and a third (N3) transistor, the series arrangement being coupled to the output terminal (U) for producing at the output terminal (U) a second output voltage up to a maximum second voltage value, the second amplifier (A2) also being coupled between the first (V_{dd}) and the second (V_{ss}) supply voltage terminal, and means (M) for driving the first (A1) and the second (A2) amplifier with a first and second drive signal respectively, the sum of the first and second drive signal being proportional to the input signal and the ratio between the first and second drive signal being dependent on the difference between the actual output voltage value at the output terminal (U) and the first voltage value.
2. An amplifier arrangement as claimed in Claim 1, characterized in that the means (M) comprise a differential pair comprising a fourth (P1) and a fifth (P2) transistor, each having a base (1, 2) for receiving a first portion (V_{uit1}) of the output voltage and a first reference voltage (V_{ref1}) respectively, having mutually coupled emitters for receiving a portion of the input signal, and each having a collector (u3, u4) for driving the first amplifier (A1) and the second amplifier (A2) respectively.
3. An amplifier arrangement as claimed in Claim 2, characterized in that the means (M) comprise a further differential pair comprising a sixth (N4) and a seventh (N5) transistor, each having a base (6, 7) for receiving a second portion (V_{uit3}) of the output voltage and a second reference voltage (V_{ref2}) respectively, and having their emitters coupled to one another to supply the first portion (V_{uit1}) of the output voltage.
4. An amplifier arrangement as claimed in Claim 1 or 2, characterized in that the means (M) further comprise a current regulator (S).
5. An amplifier arrangement as claimed in Claim 4, characterized in that the current regulator (S) is at least coupled to the emitter and collector of both the fourth (P1) and the fifth (P2) transistor.
6. An amplifier arrangement as claimed in Claim 4 or 5, characterized in that the current regulator (S) comprises two transistors (P6, P7) connected as a differential pair having their emitters coupled to each other and to a reference-voltage circuit (J1, N6-N9, P8).
7. An amplifier arrangement as claimed in any one of the preceding Claims, characterized in that the second (N2) and the third (N3) transistor each have a base coupled respectively to the means (M) and to a terminal (3) for receiving a third portion (V_{uit2}) of the output voltage.
8. An amplifier arrangement as claimed in any one of the preceding Claims wherein the said transistors having a base, emitter and collector are replaced by transistors having a gate, source and drain.

Patentansprüche

1. Verstärkeranordnung mit einem Eingangsanschluß (I) zum Empfangen einer Eingangsspannung, einem Ausgangsanschluß (U) zum Abgeben einer Ausgangsspannung, die eine verstärkte Version der Eingangsspannung ist, einem ersten Verstärker (A1), der einen mit dem Ausgangsanschluß (U) gekoppelten ersten Transistor (N1) hat, zum Erzeugen einer ersten Ausgangsspannung bis zum maximalen ersten Spannungswert am Ausgangsanschluß (U), wobei der erste Verstärker zwischen

whose first main electrode is connected to the first main electrode of the transistor P8. The reference-voltage circuit provides the bias voltage for the transistors N6 and N7, the differential pair P6 and P7 dictating the magnitude of the currents depending on the voltages on the output terminals u3 and u4. These currents ensure that the bias currents applied to the active amplifier of the amplifiers A1 and A2 constantly have substantially constant values to stabilize the corresponding transconductances. This minimizes the cross-over distortion. Equal voltages on the output terminals u3 and u4 will give rise to equal currents through the transistors N6 and P6 and through the transistors N7 and P7. Unequal voltages on the output terminals u3 and u4, however, will give rise to unequal currents through the transistors P6 and P7, while the currents through the transistors N6 and N7 remain equal to each other. The magnitudes of the currents are dictated by the voltage difference between the control electrodes of the transistors N6 and N7 on the one hand and the output terminals u3 and u4 on the other hand.

In the embodiments disclosed herein, it is also possible to use unipolar transistors.

Claims

1. An amplifier arrangement comprising an input terminal (I) for receiving an input voltage, an output terminal (U) for supplying an output voltage which is an amplified version of the input voltage, a first amplifier (A1) having a first transistor (N1) coupled to the output terminal (U) for producing at the output terminal (U) a first output voltage up to a maximum first voltage value, the first amplifier being coupled between a first (V_{dd}) and a second (V_{ss}) supply voltage terminal, characterized in that the amplifier arrangement further comprises a second amplifier (A2) having a series arrangement of a second (N2) and a third (N3) transistor, the series arrangement being coupled to the output terminal (U) for producing at the output terminal (U) a second output voltage up to a maximum second voltage value, the second amplifier (A2) also being coupled between the first (V_{dd}) and the second (V_{ss}) supply voltage terminal, and means (M) for driving the first (A1) and the second (A2) amplifier with a first and second drive signal respectively, the sum of the first and second drive signal being proportional to the input signal and the ratio between the first and second drive signal being dependent on the difference between the actual output voltage value at the output terminal (U) and the first voltage value.
2. An amplifier arrangement as claimed in Claim 1, characterized in that the means (M) comprise a differential pair comprising a fourth (P1) and a fifth (P2) transistor, each having a base (1, 2) for receiving a

first portion (V_{uit1}) of the output voltage and a first reference voltage (V_{ref1}) respectively, having mutually coupled emitters for receiving a portion of the input signal, and each having a collector (u3, u4) for driving the first amplifier (A1) and the second amplifier (A2) respectively.

3. An amplifier arrangement as claimed in Claim 2, characterized in that the means (M) comprise a further differential pair comprising a sixth (N4) and a seventh (N5) transistor, each having a base (6, 7) for receiving a second portion (V_{uit3}) of the output voltage and a second reference voltage (V_{ref2}) respectively, and having their emitters coupled to one another to supply the first portion (V_{uit1}) of the output voltage.
4. An amplifier arrangement as claimed in Claim 1 or 2, characterized in that the means (M) further comprise a current regulator (S).
5. An amplifier arrangement as claimed in Claim 4, characterized in that the current regulator (S) is at least coupled to the emitter and collector of both the fourth (P1) and the fifth (P2) transistor.
6. An amplifier arrangement as claimed in Claim 4 or 5, characterized in that the current regulator (S) comprises two transistors (P6, P7) connected as a differential pair having their emitters coupled to each other and to a reference-voltage circuit (J1, N6-N9, P8).
7. An amplifier arrangement as claimed in any one of the preceding Claims, characterized in that the second (N2) and the third (N3) transistor each have a base coupled respectively to the means (M) and to a terminal (3) for receiving a third portion (V_{uit2}) of the output voltage.
8. An amplifier arrangement as claimed in any one of the preceding Claims wherein the said transistors having a base, emitter and collector are replaced by transistors having a gate, source and drain.

Patentansprüche

1. Verstärkeranordnung mit einem Eingangsanschluß (I) zum Empfangen einer Eingangsspannung, einem Ausgangsanschluß (U) zum Abgeben einer Ausgangsspannung, die eine verstärkte Version der Eingangsspannung ist, einem ersten Verstärker (A1), der einen mit dem Ausgangsanschluß (U) gekoppelten ersten Transistor (N1) hat, zum Erzeugen einer ersten Ausgangsspannung bis zum maximalen ersten Spannungswert am Ausgangsanschluß (U), wobei der erste Verstärker zwischen



- einen ersten (V_{dd}) und einen zweiten (V_{ss}) Versorgungsanschluß gekoppelt ist, dadurch gekennzeichnet ist, daß die Verstärkeranordnung weiterhin einen zweiten Verstärker (A2) mit einer Reihenschaltung aus einem zweiten (N2) und einem dritten (N3) Transistor umfaßt, wobei die Reihenschaltung mit dem Ausgangsanschluß (U) gekoppelt ist, um am Ausgangsanschluß (U) eine zweite Ausgangsspannung bis zum maximalen zweiten Spannungswert zu erzeugen, wobei der zweite Verstärker (A2) auch zwischen den ersten (V_{dd}) und den zweiten (V_{ss}) Versorgungsspannungsanschluß gekoppelt ist, und Mittel (M) zum Ansteuern des ersten (A1) und des zweiten (A2) Verstärkers mit einem ersten bzw. zweiten Ansteuerungssignal, wobei die Summe aus dem ersten und dem zweiten Ansteuerungssignal proportional zum Eingangssignal ist und das Verhältnis zwischen dem ersten und dem zweiten Ansteuerungssignal von der Differenz zwischen dem tatsächlichen Ausgangsspannungswert am Ausgangsanschluß (U) und dem ersten Spannungswert abhängt.
2. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel (M) ein Differenzpaar mit einem vierten (P1) und einem fünften (P2) Transistor umfassen, von denen jeder eine Basis (1, 2) zum Empfangen eines ersten Anteils (V_{uit1}) der Ausgangsspannung bzw. einer ersten Bezugsspannung (V_{ref1}) hat, sie miteinander gekoppelte Emitter zum Empfangen eines Anteils des Eingangssignals haben, und jeder einen Kollektor (u3, u4) zum Ansteuern des ersten Verstärkers (A1) bzw. des zweiten Verstärkers (A2) hat.
 3. Verstärkeranordnung nach Anspruch 2, dadurch gekennzeichnet, daß die Mittel (M) ein weiteres Differenzpaar mit einem sechsten (N4) und einem siebten (N5) Transistor umfassen, von denen jeder eine Basis (6, 7) zum Empfangen eines zweiten Anteils (V_{uit2}) der Ausgangsspannung bzw. einer zweiten Bezugsspannung (V_{ref2}) hat, und deren Emitter miteinander gekoppelt sind, um den ersten Anteil (V_{uit1}) der Ausgangsspannung zu liefern.
 4. Verstärkeranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Mittel (M) weiterhin einen Stromregler (S) umfassen.
 5. Verstärkeranordnung nach Anspruch 4, dadurch gekennzeichnet, daß der Stromregler (S) mindestens mit dem Emitter und dem Kollektor sowohl des vierten (P1) als auch des fünften (P2) Transistors gekoppelt ist.
 6. Verstärkeranordnung nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß der Stromregler (S) zwei als Differenzpaar geschaltete Transistoren (P6, P7) umfaßt, deren Emitter miteinander und mit einer Bezugsspannungsschaltung (J1, N6-N9, P8) gekoppelt sind.
 7. Verstärkeranordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß der zweite (N2) und der dritte (N3) Transistor je eine Basis haben, die mit den Mitteln (M) bzw. einem Anschluß (3) zum Empfangen eines dritten Anteils (V_{uit2}) der Ausgangsspannung gekoppelt ist.
 8. Verstärkeranordnung nach einem der vorhergehenden Ansprüche, wobei die genannten Transistoren, die eine Basis, einen Emitter und einen Kollektor haben, durch Transistoren mit einem Gate, einer Source und einem Drain ersetzt worden sind.

Revendications

1. Circuit d'amplification comprenant une borne d'entrée (I) destinée à recevoir une tension d'entrée, une borne de sortie (U) destinée à fournir une tension de sortie qui soit une version amplifiée de la tension d'entrée, un premier amplificateur (A1) comportant un premier transistor (N1) couplé à la borne de sortie (U) afin de produire à la borne de sortie (U) une première tension de sortie supérieure à une première valeur de tension maximale, le premier amplificateur étant couplé entre une première (V_{dd}) et une deuxième (V_{ss}) bornes de tension d'alimentation, caractérisé en ce que le circuit d'amplification comprend en plus un deuxième amplificateur (A2) comportant un montage en série d'un deuxième (N2) et d'un troisième (N3) transistors, le montage en série étant couplé à la borne de sortie (U) afin de produire à la borne de sortie (U) une deuxième tension de sortie supérieure à une deuxième valeur de tension maximale, le deuxième amplificateur (A2) étant également couplé entre la première (V_{dd}) et la deuxième (V_{ss}) bornes de tension d'alimentation, et des moyens (M) destinés à commander le premier (A1) et le deuxième (A2) amplificateurs avec un premier signal et un deuxième signal d'attaque, respectivement, la somme du premier signal et du deuxième signal d'attaque étant proportionnelle au signal d'entrée et le rapport entre le premier signal et le deuxième signal d'attaque étant fonction de la différence entre la valeur effective de la tension de sortie à la borne de sortie (U) et la première valeur de tension.
2. Circuit d'amplification suivant la revendication 1, caractérisé en ce que les moyens (M) comprennent une paire différentielle comprenant un quatrième (P1) et un cinquième (P2) transistors ayant chacun une base (1, 2) destinée à recevoir une première partie (V_{uit1}) de la tension de sortie et une première



tension de référence (V_{ref1}), respectivement, comportant des émetteurs couplés l'un à l'autre pour recevoir une première partie du signal d'entrée, et ayant chacun un collecteur ($u3$, $u4$) destiné à attaquer le premier amplificateur (A1) et le deuxième amplificateur (A2), respectivement. 5

3. Circuit d'amplification suivant la revendication 2, caractérisé en ce que les moyens (M) comprennent une autre paire différentielle comprenant un sixième (N4) et un septième (N5) transistors, chacun ayant une base (6, 7) destinée à recevoir une deuxième partie (V_{uit3}) de la tension de sortie et une deuxième tension de référence (V_{ref2}), respectivement, et leurs émetteurs étant couplés l'un à l'autre afin de fournir la première partie (V_{uit1}) de la tension de sortie. 10 15
4. Circuit d'amplification suivant la revendication 1 ou 2, caractérisé en ce que les moyens (M) comprennent en plus un régulateur de courant (S). 20
5. Circuit d'amplification suivant la revendication 4, caractérisé en ce que le régulateur de courant (S) est couplé au moins à l'émetteur et au collecteur des quatrième (P1) et cinquième (P2) transistors. 25
6. Circuit d'amplification suivant la revendication 4 ou 5, caractérisé en ce que le régulateur de courant (S) comprend deux transistors (P6, P7) connectés en paire différentielle, leurs émetteurs étant couplés l'un à l'autre et à un circuit de tension de référence (J1, N6-N9, P8). 30
7. Circuit d'amplification suivant l'une quelconque des revendications précédentes, caractérisé en ce que le deuxième (N2) et le troisième (N3) transistors ont chacun une base couplée respectivement aux moyens (M) et à une borne (3) pour recevoir une troisième partie (V_{uit2}) de la tension de sortie. 35 40
8. Circuit d'amplification suivant l'une quelconque des revendications précédentes, dans lequel lesdits transistors qui ont une base, un émetteur et un collecteur sont remplacés par des transistors ayant une grille, une source et un drain. 45

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