Claims

What is claimed:

1. ~~A method of making a semiconductor package, comprising:~~

~~providing a substrate having an active surface containing a plurality of active circuits;~~

~~forming an adhesive layer over the active surface of the substrate;~~

~~mounting a known good unit (KGU) to the adhesive layer; and~~

~~forming an interconnect structure to electrically connect the KGU and active circuits on the substrate by,~~

~~(a) providing a wire bond between a contact pad on the substrate and a contact pad on the KGU,~~

~~(b) forming a redistribution layer on a back surface of the substrate, opposite the active surface,~~

~~(c) forming a through hole via (THV) through the substrate to electrically connect the redistribution layer and wire bond, and~~

~~(d) forming solder bumps in electrical contact with the redistribution layer.~~ A method of making a semiconductor device, comprising:

providing a semiconductor wafer containing a plurality of first semiconductor die each having an active surface;

forming an adhesive layer on the active surface of the first semiconductor die;

providing a plurality of semiconductor packages by,

(a) providing a leadframe for each semiconductor package,

(b) mounting a second semiconductor die to a die pad on the leadframe,

(c) forming a dam around the die pad,

(d) forming a first bond wire between the second semiconductor die and a first contact pad on the leadframe, and

(e) depositing a first encapsulant in contact with the second semiconductor die and leadframe;

leading with the first encapsulant, mounting the semiconductor packages to the adhesive layer over the active surface of the first semiconductor die;

forming a second bond wire between the first contact pad on the leadframe and a contact pad on the first semiconductor die;

depositing a second encapsulant in contact with the semiconductor packages and semiconductor wafer, the dam preventing the second encapsulant from covering the die pad of the leadframe;

forming a redistribution layer over a back surface of the first semiconductor die, opposite the active surface;

forming a conductive via through the first semiconductor die to electrically connect the redistribution layer and contact pad of the first semiconductor die;

forming a first bump on the redistribution layer; and

singulating the semiconductor wafer into the individual first semiconductor die after mounting the semiconductor package, each semiconductor package being a known good unit which performs electrical functions in support of the first semiconductor die so that the

active circuits in the first semiconductor die can be formed without the electrical functions performed by the semiconductor package.

2. ~~The method of claim 1, further including forming the KGU by the steps of providing a KGU substrate for supporting the KGU, disposing a semiconductor die over the KGU substrate, and forming an encapsulant over the semiconductor die.~~ The method of claim 1, wherein the semiconductor package includes a quad-flat non-leaded package or ball grid array package.

3. The method of claim 1, further including ~~forming an encapsulant over the KGU.~~ mounting a discrete semiconductor component to the first semiconductor die.

4. The method of claim 1, ~~wherein forming the THV includes depositing an organic epoxy material into the THV.~~ further including mounting the back surface of the first semiconductor die to a printed circuit board.

5. The method of claim 1, ~~wherein the KCU includes a quad-flat non-leaded package.~~ further including forming a second bump over a second contact pad on the leadframe.

6. The method of claim 1, further including mounting ~~a discrete component to the substrate.~~ the semiconductor package to a printed circuit board.

7. ~~The method of claim 1, further including mounting the semiconductor package to a printed circuit board.~~ A method of making a semiconductor device, comprising:

providing a semiconductor wafer containing a plurality of first semiconductor die each having an active surface;

providing a plurality of semiconductor packages by,

(a) providing a leadframe for each semiconductor package,

(b) mounting a second semiconductor die to a die pad on the leadframe,

(c) forming a first electrical interconnection between the second semiconductor die and leadframe, and

(d) depositing a first encapsulant in contact with the second semiconductor die and leadframe;

mounting the semiconductor packages to the active

surface of the first semiconductor die;

forming a second electrical interconnection between the leadframe and first semiconductor die;

depositing a second encapsulant in contact with the semiconductor packages and first semiconductor die; and

singulating the semiconductor wafer into the individual first semiconductor die after mounting the semiconductor package, each semiconductor package being a known good unit which performs electrical functions in support of the first semiconductor die so that the active circuits in the first semiconductor die can be formed without the electrical functions performed by the semiconductor package.

8. The method of claim ~~1, further including forming solder bumps on the KGU.~~ 7, further including:

forming a redistribution layer over a back surface of the first semiconductor die, opposite the active surface;

forming a conductive via through the first semiconductor die to electrically connect the redistribution layer and active surface of the first semiconductor die; and

forming a third electrical interconnection over the redistribution layer.

9. ~~A method of making a semiconductor package, comprising:~~

~~providing a substrate having an active surface containing a plurality of active circuits;~~

~~forming an adhesive layer over the active surface of the substrate;~~

~~mounting a known good unit (KGU) to the adhesive layer; and~~

~~forming an interconnect structure to electrically connect the KGU and active circuits on the substrate.~~ The method of claim 7, further including forming a dam around the die pad to prevent the second encapsulant from covering the die pad of the leadframe.

10. ~~The method of claim 9, wherein forming the interconnect structure includes:~~

~~providing a wire bond between a contact pad on the substrate and a contact pad on the KGU;~~

~~forming a redistribution layer on a back surface of the substrate, opposite the active surface;~~

~~forming a through hole via (THV) through the~~

~~substrate to electrically connect the redistribution layer and wire bond; and~~

~~forming solder bumps in electrical contact with the redistribution layer.~~ The method of claim 7, further including mounting a third semiconductor die to the first semiconductor die.

11. ~~The method of claim 9, further including forming the KGU by the steps of providing a KGU substrate for supporting the KGU, disposing a semiconductor die over the KGU substrate, and forming an encapsulant over the semiconductor die.~~ The method of claim 7, further including mounting the first semiconductor die to a printed circuit board.

12. ~~The method of claim 9, further including forming an encapsulant over the KGU.~~ The method of claim 7, further including mounting the semiconductor package to a printed circuit board.

13. ~~The method of claim 9, wherein forming the THV includes depositing an organic epoxy material into the THV.~~ A method of making a semiconductor device, comprising:

providing a first semiconductor die having an active surface;

providing a semiconductor package by,

(a) providing a substrate,

(b) mounting a second semiconductor die to the substrate,

(c) forming a first electrical connection between the second semiconductor die and substrate, and

(d) depositing a first encapsulant covering the second semiconductor die and substrate;

mounting the semiconductor package to the active surface of the first semiconductor die;

forming a second electrical interconnection between the substrate and first semiconductor die; and

depositing a second encapsulant covering the semiconductor package and first semiconductor die;

wherein the semiconductor package is a known good unit which performs electrical functions in support of the first semiconductor die so that the active circuits in the first semiconductor die can be formed without the electrical functions performed by the semiconductor package.

14. The method of claim ~~9, wherein the KGU includes a quad-flat non-leaded package.~~ 13, further including:

forming a redistribution layer over a back surface of the first semiconductor die, opposite the active surface;

forming a conductive via through the first semiconductor die to electrically connect the redistribution layer and first semiconductor die; and

forming a third electrical interconnection over the redistribution layer.

15. The method of claim ~~9, further including mounting a discrete component to the substrate.~~ 13, further including forming a dam around a portion of the substrate to which

the second semiconductor die is mounted to prevent the second encapsulant from covering the portion of the substrate to which the second semiconductor die is mounted.

16. ~~A method of making a semiconductor package, comprising:~~

~~providing a substrate;~~

~~mounting a first surface of a known good unit (KGU) to a first surface of the substrate;~~

~~forming a first interconnect structure to electrically connect the KGU and substrate;~~

~~forming a second interconnect structure on a second surface of the substrate, opposite the first surface of the substrate; and~~

~~forming a third interconnect structure on a second surface of the KGU, opposite the first surface of the KGU.~~ The method of claim 13, further including mounting the first semiconductor die to a printed circuit board.

17. ~~The method of claim 16, wherein forming the first interconnect structure includes:~~

~~providing a wire bond between a contact pad on the substrate and a contact pad on the KGU;~~

~~forming a redistribution layer on a back surface of the substrate, opposite the active surface;~~

~~forming a through hole via (THV) through the substrate to electrically connect the redistribution layer and wire bond; and~~

~~forming solder bumps in electrical contact with the redistribution layer.~~ The method of claim 13, further including mounting the semiconductor package to a printed circuit board.

18. The method of claim ~~16, further including forming the KGU by the steps of providing a KGU substrate for supporting the KGU, disposing a semiconductor die over the KGU substrate, and forming an encapsulant over the semiconductor die.~~ 13, further including mounting a third semiconductor die to the first semiconductor die.

19. The method of claim ~~16, wherein the KGU includes a quad flat non-leaded package.~~ 13, further including mounting a third semiconductor die to the semiconductor package.

20. ~~The method of claim 16, further including mounting a semiconductor device to the second interconnect structure.~~

A method of making a semiconductor device, comprising:

providing a first semiconductor die having an active surface;

providing a semiconductor package by,

(a) providing a second semiconductor die,

(b) forming a first electrical interconnection to the second semiconductor die, and

(c) depositing a first encapsulant covering the second semiconductor die;

mounting the semiconductor package to the first semiconductor die;

forming a second electrical interconnection with the first electrical interconnection between the first semiconductor die and second semiconductor die; and

depositing a second encapsulant covering the semiconductor package and first semiconductor die;

wherein the semiconductor package is a known good unit which performs electrical functions in support of the first semiconductor die so that the active circuits in the first semiconductor die can be formed without the electrical functions performed by the semiconductor package.

21. ~~A semiconductor package, comprising:~~

~~a substrate having an active surface containing a plurality of active circuits;~~

~~an adhesive layer formed over the active surface of the substrate;~~

~~a known good unit (KGU) mounted to the adhesive~~

~~layer; and~~

~~an interconnect structure electrically connecting the KCU and active circuits on the substrate.~~ The method of claim 20, further including:

forming a redistribution layer over a back surface of the first semiconductor die, opposite the active surface; and

forming a conductive via through the first semiconductor die to electrically connect the redistribution layer and first semiconductor die.

22. ~~The semiconductor package of claim 21, wherein the interconnect structure includes:~~

~~a wire bond coupled between a contact pad on the substrate and a contact pad on the KCU;~~

~~a redistribution layer formed on a back surface of the substrate, opposite the active surface;~~

~~a through hole via (THV) formed through the substrate to electrically connect the redistribution layer and wire bond; and~~

~~a plurality of solder bumps in electrical contact with the redistribution layer.~~ The method of claim 20, further including forming a dam around a portion of the substrate to which the second semiconductor die is mounted to prevent the second encapsulant from covering the portion of the substrate to which the second semiconductor die is mounted.

23. ~~The semiconductor package of claim 21, wherein the KCU further includes:~~

~~a KGU substrate for supporting the KGU;~~

~~a semiconductor die disposed over the KGU substrate;~~ ~~and an encapsulant formed over the semiconductor die.~~ The method of claim 20, further including mounting a third semiconductor die to the first semiconductor die.

24. ~~The semiconductor package of claim 21, further including an encapsulant formed over the KGU.~~ The method of claim 23, further including depositing a third encapsulant covering the third semiconductor die and first semiconductor die.

25. ~~The semiconductor package of claim 21, wherein the KGU includes a quad flat non-leaded package.~~ The method of claim 20, further including mounting a third semiconductor die to the semiconductor package.