(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 March 2002 (07.03.2002)

PCT

(10) International Publication Number
WO 02/019431 A3

(51) International Patent Classification[7]: H01L 21/336, 29/51, 21/28, 29/423

(21) International Application Number: PCT/US01/26342

(22) International Filing Date: 23 August 2001 (23.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/648,044 25 August 2000 (25.08.2000) US

(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Boise, ID 83706-9632 (US).

(72) Inventors: MOULI, Chandra, V.; 727 S. Granite Way, Boise, ID 83712 (US). ROBERTS, Ceredig; 1066 Hearthstone Drive, Boise, ID 83702 (US).

(74) Agents: JIVIDEN, William, A. et al.; Kilworth, Gottman, Hagan & Schaeff, L.L.P., Suite 500, One Dayton Centre, One South Main Street, Dayton, OH 45402-2023 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

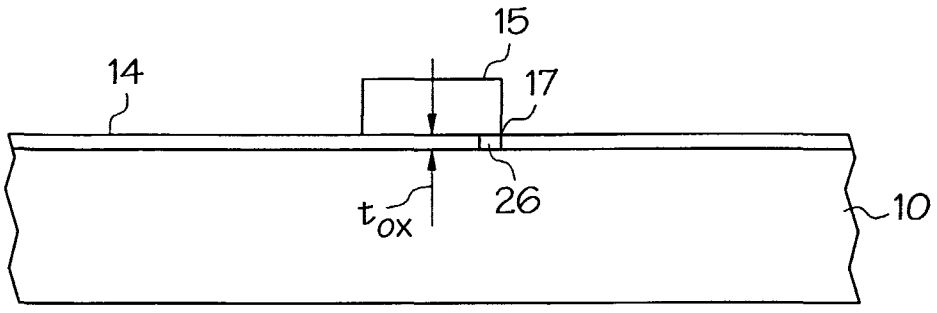
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
17 October 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND DEVICE TO REDUCE GATE-INDUCED DRAIN LEAKAGE (GIDL) CURRENT IN THIN GATE OXIDE MOSFETS



(57) Abstract: A process for the fabrication of an integrated circuit which provides a FET device having reduced GIDL current is described. A semiconductor substrate is provided wherein active regions are separated by an isolation region, and a gate oxide layer is formed on the active regions. Gate electrodes are formed upon the gate oxide layer in the active regions. An angled, high dose, ion implant is performed to selectively dope the gate oxide layer beneath an edge of each gate electrode in a gate-drain overlap region, and the fabrication of the integrated circuit is completed.

WO 02/019431 A3