

DESCRIPTION

TITLE: Basic structure of quantum devices and process for manufacturing same

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TECHNICAL FIELD OF THE INVENTION

The invention relates to materials and structures that are capable of forming a basis for electronic devices whose operating principle is based on the manipulation of quantum objects, in particular qubits.

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TECHNOLOGICAL BACKGROUND

Silicon is recognized as a promising material for electronic devices based on the manipulation of the spin of electrons, which represents their magnetic moment. In particular, information can be stored and manipulated by altering the spin of electrons, rather than by using their electrical charge as in conventional electronics. The spin of electrons can also be used as a support for qubits, for the purpose of putting quantum information theory into practice, by making use of superposition of spin states with a well-defined phase. The documents EP 3 975 072 A1 and US 2023/0026518 may be consulted.

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The period of maintenance of the phase, and therefore of the information, is defined by the coherence time. Long coherence times are necessary to ensure that operations on qubits can be performed, or that quantum information can be stored, before a read operation in which the qubit loses its coherence and the information is lost.

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US 2004/0169225 A1 and US 2006/0091393 A1 propose wafers of semiconductor material comprising layers of isotopically enriched silicon with a higher thermal conductivity than that of natural silicon.

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The paper by Mazzocchi V *et al.* entitled "99.992% ^{28}Si CVD-grown epilayer on 300 mm substrates for large scale integration of silicon spin qubits", ARXIV.ORG, Cornell University Library, 201 Olin Library Cornell University Ithaca, NY 14853, 13 July 2018 XP081248026 and the paper by Mazzocchi V *et al.* entitled "99.992% ^{28}Si CVD-grown epilayer on 300 mm substrates for large scale integration of silicon spin qubits", Journal of Crystal Growth, vol. 509, pages 1-7, XP085581554, ISSN: 022-0248, DOI: 10.1016/J.CRYSGRO.2018.12.010 describe the epitaxial growth of silicon-28 isotope layers with a purity of over 99.992% on 300 mm natural silicon substrates for use in quantum applications.

The document from CC LO *et al.* entitled "Device fabrication and transport measurements of FinFETs built with ^{28}Si SOI wafers towards donor qubits in silicon" describes an example of application of ^{28}Si with the manufacture of FinFETS transistors.

Silicon has three stable isotopes, namely the isotopes ^{28}Si , ^{29}Si and ^{30}Si , which constitute about 92.2%, 4.7% and 3.1% of natural silicon, respectively. One of the mechanisms that promotes the decoherence of spin states is the presence of the ^{29}Si silicon isotope, whose nuclear magnetic moment is not zero. It is therefore preferable to eliminate, as much as possible, the proportion of ^{29}Si in silicon used as the basis of qubit manipulation devices. The ^{30}Si isotope should also be eliminated: although the ^{30}Si isotope has no spin, it causes variations in the lengths of bonds between atoms, and therefore in the local environment of qubits. The homogeneity of the local environment should be maximized, so that the characteristics of the qubits are as similar as possible to each other.

One solution consists in using silicon enriched in ^{28}Si isotope. Schneider *et al.* (E. Schneider and J. England, "Isotopically Enriched Layers for Quantum Computers Formed by

²⁸Si Implantation and Layer Exchange", ACS Appl. Mater. Interfaces 2023, 15, 21609-21617) propose a technique for enriching a ²⁸Si silicon isotope layer based on the ion implantation of ²⁸Si ions into a layer of aluminium formed on a substrate of silicon without native oxide, followed by layer exchange crystallization: this produces a high-purity ²⁸Si layer in contact with the silicon substrate. Schneider also explains that defects at the interfaces of the layers of the devices make it necessary to use high-quality dielectrics and/or techniques for keeping the qubits away from the interfaces and the noise that they create, depending on the qubit placement geometry and whether the qubits are close to or distant from the interfaces.

Devices for manipulating spin qubits can be produced by using silicon as a base, with standard CMOS (Complementary Metal Oxide Semiconductor) or FD-SOI (Fully Depleted Silicon On Insulator) manufacturing processes, as used in the semiconductor industry. In particular, the FD-SOI technique may be used to control the placement of the qubits, at a distance from the interfaces between the silicon and the gate dielectric or the buried oxide (BOX) layer.

However, there are no commercially available substrates of the SOI (silicon on insulator) type that have a thin layer of the ²⁸Si silicon isotope of quantum quality. Here, "quantum quality" is taken to mean ²⁸Si layers that are pure enough, with a ²⁸Si purity of more than 99.92%, for the spin coherence of the electrons to have a sufficient duration to permit operations on the qubits.

Thus there is a need for silicon wafers that can be used as substrates for the manufacture of electron spin qubit manipulation devices that are capable of maintaining the isotopic purity of ²⁸Si layers and enabling qubits to be manipulated at chosen locations compatible with the type of device envisaged.

There is also a need for SOI (Silicon On Insulator) substrates having a thin layer of ^{28}Si on a substrate, with an electrically insulating layer interposed between the ^{28}Si layer and the substrate. It is advantageous for the thin layer and the electrically insulating layer (the buried oxide "BOX" layer) to be thin enough to be able to form FD-SOI (Fully Depleted SOI) transistors.

Furthermore, given that quantum applications require operations to be performed at very low temperatures, of less than 3 K or of the order of 10 mK for example, while using control electronics that are physically as close as possible to the supports of the quantum magnitudes manipulated, the integration of FD-SOI transistors and devices for manipulating quantum magnitudes on the same substrate is advantageous: FD-SOI transistors can have a low threshold voltage and can operate while limiting the dissipation of energy into their support, and therefore while limiting the problems of heating of these quantum magnitude manipulation devices.

SUMMARY OF THE INVENTION

The Applicant's aim is to provide a structure and a process for manufacturing a semiconductor support that is capable of forming a base for obtaining devices for manipulating quantum objects, particularly qubits formed by electron spins.

In order to achieve this aim, one aspect of the invention is a structure that is capable of forming a quantum device, comprising: a silicon carrier substrate; a first layer of ^{28}Si silicon isotope; a layer of silicon oxide; a second layer of ^{28}Si silicon isotope, the structure being formed by the carrier substrate, the first layer of ^{28}Si silicon isotope, the layer of silicon oxide, and the second layer of ^{28}Si silicon isotope, stacked in this order, in which the first layer (Si-L1) and

the second layer (Si-L2) of ^{28}Si silicon isotope are each formed from at least 99.92% ^{28}Si silicon isotope.

A first advantage of the structure is that it provides a suitable basis for the development of quantum devices using technologies that are already well mastered in the semiconductor field.

A second advantage of the structure is that it ensures the reliability of the devices obtained by virtue of the presence of a bilayer of ^{28}Si and $^{28}\text{SiO}_2$ acting as a barrier to undesirable elements contained in the support substrate, such as the silicon isotopes ^{29}Si and ^{30}Si , or even carbon, oxygen or nitrogen atoms. Specifically, it would be difficult and extremely costly to produce silicon substrates formed purely from the ^{28}Si silicon isotope. The substrates available are thus formed from natural silicon, containing at least the three silicon isotopes ^{28}Si , ^{29}Si and ^{30}Si , and also impurities such as carbon, oxygen and nitrogen.

A third advantage of the structure is that it may be obtained via known methods, suited to the needs of quantum devices, which accelerates the technological maturity of the manufacturing process involved and reduces the necessary investment in time and equipment.

According to additional non-limiting features of the support according to the invention, considered individually or in any technically feasible combination:

- the second layer of ^{28}Si silicon isotope may comprise less than 800 ppm of ^{29}Si silicon isotope;
- the first layer of ^{28}Si silicon isotope may comprise less than 800 ppm of ^{29}Si silicon isotope;
- the second layer of ^{28}Si silicon isotope may have a thickness of between 10 and 60 nm, the layer of silicon oxide may have a thickness of between 10 and 50 nm, preferentially between 15 and 30 nm, and the first layer of ^{28}Si silicon

isotope may have a thickness greater than 30 nm, preferentially between 30 nm and 250 nm; and

- the second layer of ^{28}Si silicon isotope may have a thickness of between 120 and 200 Å, preferentially between 140 and 180 Å, the layer of silicon oxide may have a thickness of between 120 and 280 Å, preferentially between 160 and 240 Å, and the first layer of ^{28}Si silicon isotope may have a thickness greater than 200 nm, preferentially between 200 nm and 420 nm.

The invention extends to a process for manufacturing a structure according to the invention, comprising the steps of: forming a first layer of ^{28}Si silicon isotope on a first substrate; forming a second layer of ^{28}Si silicon isotope on a second substrate; oxidizing the second silicon layer over part of its thickness to form a layer of oxide; assembling the first substrate and the second substrate by placing the first silicon layer in contact with the oxide layer, the first substrate, the first silicon layer, the oxide layer and the second silicon layer being stacked in that order, in which the first layer (Si-L1) and the second layer (Si-L2) of ^{28}Si silicon isotope are each formed from at least 99.92% ^{28}Si silicon isotope.

According to additional non-limiting features of the structure according to the invention, considered individually or in any technically feasible combination:

- the process according to the invention may also comprise a step of forming an embrittlement plane in the second layer by implanting ions of a light species in a non-oxidized part of the second layer after the oxidation step over part of its thickness; and a step of fracturing the second layer at the embrittlement plane and removing the donor substrate after the assembly step; and

- the second layer of ^{28}Si silicon isotope may have a thickness of between 300 nm and 600 nm prior to the oxidation step.

5 **BRIEF DESCRIPTION OF THE FIGURES**

Other characteristics and advantages of the invention will become apparent from the detailed description of the invention which will follow, with reference to the appended figures, in
10 which:

[Fig. 1] Figure 1 illustrates a fabrication process according to the invention;

[Fig. 2] Figure 2 illustrates a structure obtained by means of the process of figure 1; et

15 [Fig. 3] Figure 3 is a diagram summarizing the manufacturing process of Figures 1 and 2.

DETAILED DESCRIPTION OF THE INVENTION

20 Embodiment

One particular embodiment of the present invention is described by means of Figures 1 to 3 and of the associated description below.

Figure 2 illustrates a structure Strc consisting of a
25 carrier substrate Car, a barrier layer Si-L1, a dielectric layer Ox, and a device layer Si-L2, stacked in this order, each of these elements preferably being in direct contact with the immediately adjacent element or elements.

The barrier layer Si-L1, the oxide layer Ox and the device
30 layer Si-L2 are layers formed from the ^{28}Si silicon isotope. In particular, the Si-L1 and Si-L2 layers have a ^{28}Si purity of at least 99.92%, for example between 99.92% and 99.995%. Thus, the silicon layers Si-L1 and Si-L2 comprise less than 800 ppm of the ^{29}Si silicon isotope.

Such a structure may be used to form quantum devices on its surface, by virtue of the features of the device layer Si-L2: by virtue of its purity in ^{28}Si , the spin coherence time of the electrons of this layer is sufficient to perform operations on qubits associated with these electrons. When incorporated into a quantum device, the Si-L2 layer represents a good support for qubits.

In addition, the barrier layer Si-L1 and the oxide layer Ox prevent, or at least limit, the migration of impurities, and in particular atoms of the ^{29}Si silicon isotope, from the support substrate Car to the device layer Si-L2. Without a barrier layer, the phenomenon of impurity diffusion would increase the concentrations of ^{29}Si , ^{30}Si or other dopants to levels incompatible with the quantum quality required for the correct functioning of quantum devices. This would thus lead to a reduction in coherence times and cause these devices to operate in a manner similar to that of devices formed within conventional substrates for FD-SOI transistors.

Figure 1 illustrates in (A) the formation of the layer Si-L1 on the carrier substrate Car, in a step 310_{Car} . In this example, the carrier substrate Car consists of a single-crystal silicon wafer, but any other support conventionally used in the semiconductor industry could be employed. The barrier layer Si-L1 is grown, for example epitaxially, on one face of the carrier substrate Car.

Figure 1 illustrates in (B) the formation of the layer Si-L2 on the donor substrate Don, in a step 310_{Don} . In this example, the donor substrate Don consists of a single-crystal silicon wafer, but any other support conventionally used in the semiconductor industry could be employed. The device layer Si-L2 is grown, for example epitaxially, on one face of the donor substrate Don.

The layers Si-L1 and Si-L2 are grown in such a manner that they have silicon-28 isotope purities of between 99.920% and 99.995%. Thus, the maximum concentrations of silicon-29 isotope in these layers are, initially at least, between 800 and 50 ppm, these concentrations being low enough to allow the manufacture of quantum devices based on the spin of the electrons on the device layer Si-L2. Such compositions of the layers Si-L1 and Si-L2 can be obtained by using, in a conventional epitaxial growth process, silane gas, having a purity corresponding to that of the ^{28}Si layers, as the precursor gas of the silicon of the layers.

Figure 1 illustrates in (C) a partial oxidation, over a certain depth, of the layer Si-L2 to form a layer Ox of silicon oxide SiO_2 , in an oxidation step 320_{Don}. This operation may be performed in a conventional manner by applying a heat treatment in an oxygen atmosphere, during an oxidation step 320_{Don}. The layer Ox is preferentially formed by thermal oxidation so as to ensure a good quality of interface between the layer of oxide formed and the layer Si-L2 on the one hand and the layer Si-L1 on the other hand, after bonding. Evidently, this is a silicon oxide formed of oxygen and the ^{28}Si silicon isotope of the layer Si-L2. The layer Si-L2 is oxidized only to a certain thickness, which is strictly less than its thickness and is dependent on the intended thickness of the layer Ox. Moreover, the layer Ox may also be formed by deposition of the HDP-CVD (High Density Plasma CVD) type, which is performed at relatively low temperature in comparison with thermal oxidation, thus making it possible, advantageously, to limit the thermal budget imposed on the layer Si-L2, and thereby to limit the diffusion of the other Si isotopes in the layer intended to include the devices for manipulating quantum objects.

Figure 1 also illustrates at (C) an implantation of light species such as hydrogen, helium, or a combination of such

species into the non-oxidized part of the layer Si-L2 through the oxide layer Ox, so as to form an embrittlement plane Frg in the thickness of the non-oxidized part of the layer Si-L2, during a step 330_{Don}.

5 Following the formation of the embrittlement plane Frg, the donor substrate Don is flipped and the oxide layer Ox is brought into close contact with the layer Si-L1 of the carrier substrate Car and is assembled therewith, for example by molecular bonding or any other assembly technique in which
10 surfaces of elements to be assembled are placed in direct contact, so as to obtain the structure illustrated in (D) of Figure 1, in a step 340.

 Figure 1 illustrates in (E) the fracturing of the device layer Si-L2 at the embrittlement plane Frg obtained by ion
15 implantation, so that the donor substrate Don and a part Si-L2_{E1} is removed from the structure illustrated in (C) while a part of the device layer Si-L2 remains attached thereto, in a fracturing and removal step 350. This fracturing may be obtained by heat treatment, assisted if necessary by
20 mechanical stress to initiate breaking, according to conventional layer transfer techniques that are well known in the field of microelectronics, such as the process known as "Smart Cut". Following the assembly and fracturing of the donor substrate, heat treatment can be applied in order to
25 consolidate the assembly and to repair the assembled layers.

 An alternative to the formation of an embrittlement plane and fracturing of the layer Si-L2 in this plane may consist in thinning the donor substrate Don after it has been assembled, for example by etching, grinding and/or chemical-mechanical
30 polishing (CMP). This thinning may be used to completely remove the second substrate Don, and optionally a part of the layer Si-L2 to achieve the desired thickness for this layer.

 A step 360 of finishing the surface of the layer Si-L2 follows step 350, by one or more mechanical and/or chemical

attacks to thin the layer Si-L2 to a desired thickness and polish its accessible face. On conclusion of this step, the structure Strct illustrated in figure 2 is obtained.

5 The thicknesses of the layers Ox and Si-L1 may be chosen so as to ensure an adequate level of barrier effect to avoid contamination of the device layer Si-L2 with, in particular, ^{29}Si , while at the same time limiting the thickness of the oxide layer Ox, for example with a view to applications based on FD-SOI technology which require a thin Ox layer. Thus, by
10 computer simulation, the inventors were able to determine sets of thicknesses for the layers Si-L1, Ox and Si-L2, allowing a certain level of purity of the layer Si-L2 to be ensured while at the same time advantageously minimizing the thickness of the layer Si-L1 for a given thickness of the layer Ox, chosen
15 for its compatibility with conventional FD-SOI technology processes.

The table Tab. 1 indicates such thickness sets for two purity levels, at 99.9% and 99.99% ^{28}Si for the layer Si-L2. The numerical simulations were calculated considering that the
20 layer Si-L1 has a ^{28}Si purity level of 99.99%. These calculations notably take into account a thermal budget corresponding to that for the manufacture of Strc substrates and the conventional manufacture of an FD-SOI transistor, which is the highest thermal budget undergone by the layers,
25 including the steps for manufacturing CMOS transistors and qubit devices formed in the Si-L2 layer.

Thickness of Si-L2 (after transfer)	Thickness of Ox	Thickness of Si-L1 for an Si-L2 layer at 99.9%	Thickness of Si-L1 for an Si-L2 layer at 99.99%
16 nm	50 nm	30 nm	250 nm
16 nm	20 nm	200 nm	420 nm

Tab. 1

It will be noted that prior to steps 320, 350 and 360 for oxidizing, fracturing and finishing the layer Si-L2, the latter may have a thickness of about 400 nm, preferentially between 300 nm and 600 nm, so as to ensure that after these steps a layer Si-L2 of about 16 nm with the desired ^{28}Si purity can be obtained.

The thicknesses typically used in FD-SOI type technologies are between 10 and 60 nm for the active layer, which here corresponds to the device layer Si-L2, and between 10 and 50 nm for the oxide layer Ox, often about 20 nm thick.

The invention is not limited to the embodiment described above, and variants may be applied thereto without departing from the scope of the invention as defined by the claims.

CLAIMS

1. Structure (Strc) that is capable of forming a quantum device, comprising:

- 5 - a silicon carrier substrate (Car);
 - a first layer (Si-L1) of ^{28}Si silicon isotope;
 - a silicon oxide layer (Ox);
 - a second layer (Si-L2) of ^{28}Si silicon isotope;

10 the structure being formed by the carrier substrate (Car),
the first layer (Si-L1) of ^{28}Si silicon isotope, the layer (Ox)
of silicon oxide, and the second layer (Si-L2) of ^{28}Si silicon
isotope, stacked in this order,

 in which the first layer (Si-L1) and the second layer (Si-
L2) of ^{28}Si silicon isotope are each formed of at least 99.92%
15 ^{28}Si silicon isotope.

2. Structure (Strc) for forming a quantum device according to
Claim 1, in which the second layer (Si-L2) of ^{28}Si silicon
isotope comprises less than 800 ppm of ^{29}Si silicon isotope.

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3. Structure (Strc) for forming a quantum device according to
either of Claims 1 and 2, in which the first layer (Si-L1) of
 ^{28}Si silicon isotope comprises less than 800 ppm of ^{29}Si silicon
isotope.

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4. Structure (Strc) for forming a quantum device according to
any one of Claims 1 to 3, in which the second layer (Si-L2) of
 ^{28}Si silicon isotope has a thickness of between 10 and 60 nm,
the layer (Ox) of silicon oxide has a thickness of between 10
30 and 50 nm, preferentially between 15 and 30 nm, and the first
layer (Si-L1) of ^{28}Si silicon isotope has a thickness greater
than 30 nm, preferentially between 30 nm and 250 nm.

5. Structure (Strc) for forming a quantum device according to any one of Claims 1 to 4, in which the second layer (Si-L2) of ^{28}Si silicon isotope has a thickness of between 120 and 200 Å, preferentially between 140 and 180 Å, the layer (Ox) of silicon oxide has a thickness of between 120 and 280 Å, preferentially between 160 and 240 Å, and the first layer (Si-L1) of ^{28}Si silicon isotope has a thickness greater than 200 nm, preferentially between 200 nm and 420 nm.

6. Process (300) for manufacturing a structure according to any one of Claims 1 to 5, comprising the steps of:

- forming (310_{Car}) a first layer of ^{28}Si silicon isotope on a first substrate (Car);

- forming (310_{Don}) a second layer of ^{28}Si silicon isotope on a second substrate (Don);

- oxidizing (320_{Don}) the second layer of silicon over part of its thickness to form a layer of oxide (Ox);

- assembling (340) the first substrate (Car) and the second substrate (Don) by placing the first silicon layer (Si-L1) in contact with the oxide layer (Ox), the first substrate (Car), the first silicon layer (Si-L1), the oxide layer (Ox) and the second silicon layer (Si-L2) being stacked in this order,

in which the first layer (Si-L1) and the second layer (Si-L2) of the ^{28}Si silicon isotope are each formed from at least 99.92% of the ^{28}Si silicon isotope.

7. Process according to Claim 6, also comprising:

- a step (330_{Don}) of forming an embrittlement plane in the second layer (Si-L2) by implanting ions of a light species into a non-oxidized part of the second layer (Si-L2) after the oxidation step (320_{Don}) over part of its thickness; and

- a step (350) of fracturing the second layer (Si-L2) at the embrittlement and removal plane of the donor substrate (Don) after the assembly step (340).

- 5 8. Process according to Claim 6 or 7, in which the second layer of ^{28}Si silicon isotope has a thickness of between 300 nm and 600 nm before the oxidation step (320_{Don}).