Therefore, embodiments~~the object~~ of the present invention seek~~is~~ to propose improvements directed against the occurrence of such deficiencies.

According to an aspect of the invention, there is provided~~The object is achieved by means of~~ a method for depositing a layer on a semiconductor wafer by vapor deposition in a process chamber having an upper and a lower cover, comprising measuring the temperature on the front side of the semiconductor wafer; heating the semiconductor wafer to a deposition temperature; controlling the temperature of the upper cover of the process chamber to a target temperature, wherein the temperature of the upper cover is measured in the center of the outer surface of the upper cover and is used as an actual value of the controlled variable of a control loop for controlling the temperature of the upper cover; setting a gas flow rate with which a process gas for depositing the layer is conducted through the process chamber; and depositing the layer on the front side of the semiconductor wafer heated to the deposition temperature during the control of the temperature of the upper cover of the process chamber to the target temperature, wherein the target temperature is chosen in such a way that it correlates with the set gas flow rate of the process gas.

The invention provides for measuring the temperature of the upper cover in the center of the outer surface of the upper cover and making this temperature available as an actual value of a controlled variable in a control loop by means of which the temperature of the upper cover is controlled to a target temperature. Said target temperature is preferably chosen to lie within an optimum temperature range. The optimum temperature range is a temperature range within which the rate at which products of the process gas deposit on the inner surface of the upper cover is lower than in temperature ranges which adjoin the optimum temperature range. The actual temperature of the upper cover is measured in the center of the outer surface of the cover and hence at a location that

Preferably, at least one further layer is deposited on at least one further semiconductor wafer before the process chamber is cleaned. The cleaning of the process chamber is preferably effected by means of vapor phase etching.

~~In accordance with one preferred configuration of the method,~~ The target temperature of the upper cover is chosen in such a way that it correlates with the gas flow rate of the process gas that is set for depositing the layer.

This is because the process gas has a cooling effect on the inner surface of the upper cover. As a result and owing to the low thermal conductivity of the material of the cover, considerable temperature differences between the temperature on the inner and outer surfaces of the upper cover can occur. The temperature measured on the outer surface of the upper cover is then higher than it would be if the thermal conductivity of the material of the upper cover permitted a rapid temperature equalization. If the cooling effect of the process gas were disregarded in the choice of the target temperature, the temperature on the inner surface of the cover, despite the measures for controlling the temperature of the upper cover, could fall out of the optimum temperature range, and the process chamber would have to be cleaned more frequently as a result.

In accordance with a further preferred configuration of the method, after a cleaning of the process chamber, the amount of material deposited on semiconductor wafers is registered in the form of a total thickness, and the process chamber is cleaned again only when a defined total thickness of material has been deposited. The defined total thickness of deposited material corresponds to the sum of the thicknesses of the layers which

registered. The process chamber is cleaned again after the last cleaning only when the total thickness of epitaxially deposited silicon, that is to say the defined total thickness of deposited material, is not less than 50 μm, preferably not less than 80 μm.

According to another aspect of the invention, there is provided~~The abovementioned object is equally achieved by means of~~ an apparatus for depositing a layer on a semiconductor wafer by vapor deposition, comprising a process chamber having an upper and a lower cover and a first sensor for measuring the temperature of the upper cover in the center of the outer surface of the upper cover, and a controller for controlling the temperature of the upper cover to a predetermined target temperature using the temperature measured by the first sensor as an actual temperature, and further comprising a data memory, in which a plurality of temperature values are stored which are respectively assigned a gas flow rate of the process gas during the deposition of the layer on the semiconductor wafer, wherein the data memory predetermines that temperature value as target temperature which is assigned to the gas flow rate set for depositing the layer.

Details of a preferred embodiment of the process chamber are explained more specifically below with reference to the figure. The figure shows crucial elements of the invention in a simplified manner.

The process chamber 1 is constructed substantially symmetrically and comprises an upper cover 2, a lower cover 3 and a sidewall 4, which enclose a reactor space, in which a semiconductor wafer is coated by means of vapor deposition. The semiconductor wafer 5 to be coated is held by a susceptor 6 arranged in the reactor space. Radiant heating systems 7 and 8 for heating the semiconductor wafer to a specific deposition

temperature are situated above the upper cover 2 and below the lower cover 3. Furthermore, connections 9 and 10 for introducing process gas into the process chamber and for discharging process gas and gaseous products of the process gas from the process chamber through the sidewall 4 of the process chamber are present. The process chamber furthermore comprises a cooling system for cooling the upper cover 2 and the lower

Patent Claims

1. A method for depositing a layer on a semiconductor wafer by vapor deposition in a process chamber having an upper and a lower cover, comprising measuring the temperature on the front side of the semiconductor wafer; heating the semiconductor wafer to a deposition temperature; controlling the temperature of the upper cover of the process chamber to a target temperature, wherein the temperature of the upper cover is measured in the center of the outer surface of the upper cover and is used as an actual value of the controlled variable of a control loop for controlling the temperature of the upper cover; setting a gas flow rate with which a process gas for depositing the layer is conducted through the process chamber; and
depositing the layer on the front side of the semiconductor wafer heated to the deposition temperature during the control of the temperature of the upper cover of the process chamber to the target temperature.

2. The method as claimed in claim 1, wherein the target temperature is chosen in such a way that it correlates with the set gas flow rate of the process gas.

3. The method as claimed in claim 1 or claim 2, wherein at least one further layer is deposited on at least one further semiconductor wafer, and the amount of material that has been deposited on semiconductor wafers since a last cleaning of the process chamber is registered, and the process chamber is cleaned again after the last cleaning only when a defined total thickness of deposited material has been deposited.

4. The method as claimed in claim 3, wherein the temperature is measured on the rear side of a susceptor holding the semiconductor wafer, and wherein at least one further layer is

deposited on at least one further semiconductor wafer, and a next cleaning of the process chamber is initiated, regardless of the defined total thickness of deposited material, if the temperature difference between the temperature on the front side of the semiconductor wafer and the temperature on the rear side of the susceptor has changed by more than 5°C in comparison with an initial temperature difference that exists during the first deposition after the cleaning of the process chamber which directly precedes the next cleaning of the process chamber.

5. The method as claimed in claim 3 or claim 4, wherein the defined total thickness of deposited material is not less than 50 μm, if the semiconductor wafer consists of monocrystalline silicon and the deposited material is epitaxially deposited silicon.

6. The method as claimed in any of claims 1 to 5, wherein an epitaxial layer composed of silicon is deposited on a semiconductor wafer composed of monocrystalline silicon and the target temperature is chosen to lie in a range of 510 to 530°C, if the set gas flow rate of the process gas lies in the range of 45 to 55 slm, wherein the target temperature is chosen to lie in a range of 525 to 545°C, if the set gas flow rate of the process gas lies in the range of 56 to 65 slm, and wherein the target temperature is chosen to lie in a range of 540 to 560°C, if the set gas flow rate of the process gas lies in the range of 66 to 80 slm.

7. An apparatus for depositing a layer on a semiconductor wafer by vapor deposition, comprising a process chamber having an upper and a lower cover and a first sensor for measuring the temperature of the upper cover in the center of the outer surface of the upper cover, and a controller for controlling the temperature of the upper cover to a predetermined target

temperature using the temperature measured by the first sensor as an actual temperature.

8. The apparatus as claimed in claim 7, comprising a data memory, in which a plurality of temperature values are stored which are respectively assigned a gas flow rate of the process gas during the deposition of the layer on the semiconductor wafer, wherein the data memory predetermines that temperature value as target temperature which is assigned to the gas flow rate set for depositing the layer.

9. The apparatus as claimed in claim 7 or claim 8, comprising a measuring unit, which registers how much material has been deposited on semiconductor wafers since a last cleaning of the process chamber, and which, after registering a defined total thickness of deposited material, generates a signal for initiating a next cleaning of the process chamber that follows the last cleaning.

10. The apparatus as claimed in any of claims 7 to 9, comprising a second sensor, which measures the temperature of the semiconductor wafer on the front side of the semiconductor wafer, and a third sensor, which measures the temperature on the rear side of a susceptor holding the semiconductor wafer, and a comparison unit, which generates a signal for initiating a next cleaning of the process chamber, if the temperature difference between the temperature measured by the second sensor and the temperature measured by the third sensor deviates by more than 5°C from an initial temperature difference that exists during the first deposition after the cleaning of the process chamber which directly precedes the next cleaning of the process chamber.

Patent Claims

1. A method for depositing a layer on a semiconductor wafer by vapor deposition in a process chamber having an upper and a lower cover, comprising measuring the temperature on the front side of the semiconductor wafer; heating the semiconductor wafer to a deposition temperature; controlling the temperature of the upper cover of the process chamber to a target temperature, wherein the temperature of the upper cover is measured in the center of the outer surface of the upper cover and is used as an actual value of the controlled variable of a control loop for controlling the temperature of the upper cover; setting a gas flow rate with which a process gas for depositing the layer is conducted through the process chamber; and
depositing the layer on the front side of the semiconductor wafer heated to the deposition temperature during the control of the temperature of the upper cover of the process chamber to the target temperature, wherein the target temperature is chosen in such a way that it correlates with the set gas flow rate of the process gas.

2. The method as claimed in claim 1, wherein one or more further layer is deposited on one or more further semiconductor wafer, and the amount of material that has been deposited on semiconductor wafers since a last cleaning of the process chamber is registered, and the process chamber is cleaned again after the last cleaning only when a defined total thickness of deposited material has been deposited.

3. The method as claimed in claim 2, wherein the temperature is measured on the rear side of a susceptor holding the semiconductor wafer, and wherein one or more further layer is deposited on at least one further semiconductor wafer, and a next cleaning of the process chamber is initiated, regardless of the defined total thickness of deposited material, if the

temperature difference between the temperature on the front side of the semiconductor wafer and the temperature on the rear side of the susceptor has changed by more than 5°C in comparison with an initial temperature difference that exists during the first deposition after the cleaning of the process chamber which directly precedes the next cleaning of the process chamber.

4. The method as claimed in claim 2, wherein the defined total thickness of deposited material is not less than 50 µm, if the semiconductor wafer consists of monocrystalline silicon and the deposited material is epitaxially deposited silicon.

5. The method as claimed in claim 1, wherein an epitaxial layer composed of silicon is deposited on a semiconductor wafer composed of monocrystalline silicon and the target temperature is chosen to lie in a range of 510 to 530°C, if the set gas flow rate of the process gas lies in the range of 45 to 55 slm, wherein the target temperature is chosen to lie in a range of 525 to 545°C, if the set gas flow rate of the process gas lies in the range of 56 to 65 slm, and wherein the target temperature is chosen to lie in a range of 540 to 560°C, if the set gas flow rate of the process gas lies in the range of 66 to 80 slm.

6. An apparatus for depositing a layer on a semiconductor wafer by vapor deposition, comprising a process chamber having an upper and a lower cover and a first sensor for measuring the temperature of the upper cover in the center of the outer surface of the upper cover, and a controller for controlling the temperature of the upper cover to a predetermined target temperature using the temperature measured by the first sensor as an actual temperature, and further comprising a data memory, in which a plurality of temperature values are stored which are respectively assigned a gas flow rate of the process gas during the deposition of the layer on the

semiconductor wafer, wherein the data memory predetermines that temperature value as target temperature which is assigned to the gas flow rate set for depositing the layer.

7. The apparatus as claimed in claim 6, comprising a measuring unit, which registers the amount of material deposited on semiconductor wafers since a last cleaning of the process chamber, and which, after registering a defined total thickness of deposited material, generates a signal for initiating a next cleaning of the process chamber that follows the last cleaning.

8. The apparatus as claimed in claim 6 or claim 7, comprising a second sensor, which measures the temperature of the semiconductor wafer on the front side of the semiconductor wafer, and a third sensor, which measures the temperature on the rear side of a susceptor holding the semiconductor wafer, and a comparison unit, which generates a signal for initiating a next cleaning of the process chamber, if the temperature difference between the temperature measured by the second sensor and the temperature measured by the third sensor deviates by more than 5°C from an initial temperature difference that exists during the first deposition after the cleaning of the process chamber which directly precedes the next cleaning of the process chamber.