FIG. 1

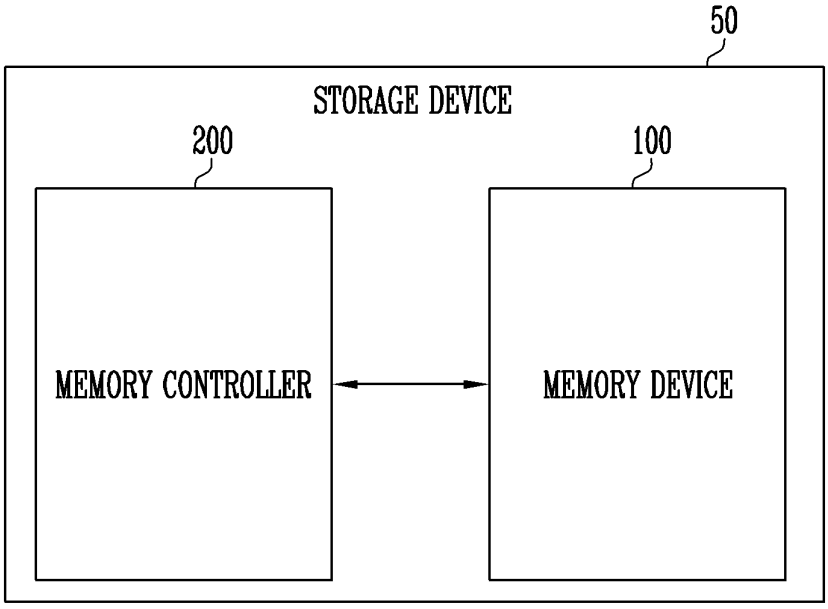


FIG. 2

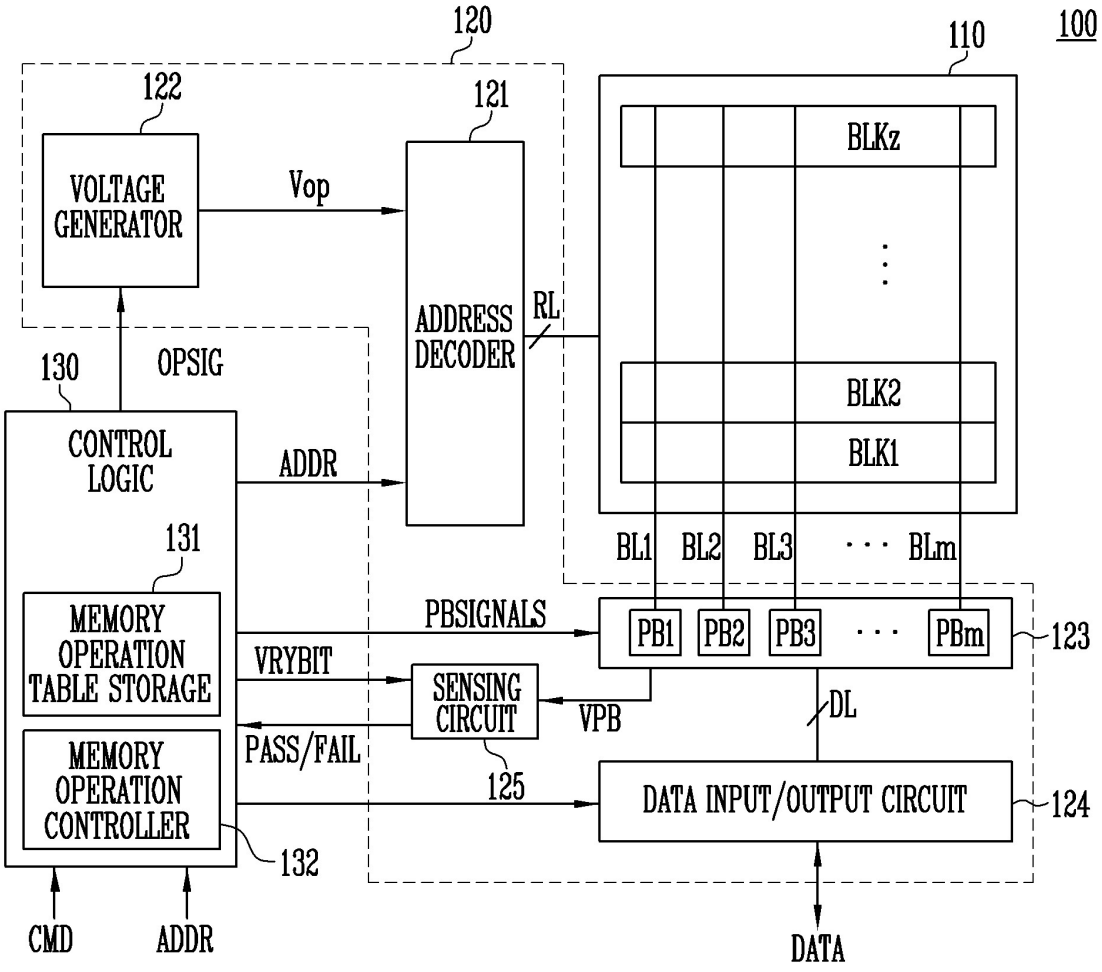

120
110
100
122
121
VOLTAGE GENERATOR
Vop
ADDRESS DECODER
RL
BLKz
BLK2
BLK1
130
OPSIG
CONTROL LOGIC
ADDR
131
BL1
BL2
BL3
BLm
MEMORY OPERATION TABLE STORAGE
PBSIGNALS
PB1
PB2
PB3
PBm
123
VRYBIT
SENSING CIRCUIT
VPB
DL
PASS/FAIL
MEMORY OPERATION CONTROLLER
125
DATA INPUT/OUTPUT CIRCUIT
124
132
CMD
ADDR
DATA

FIG. 3

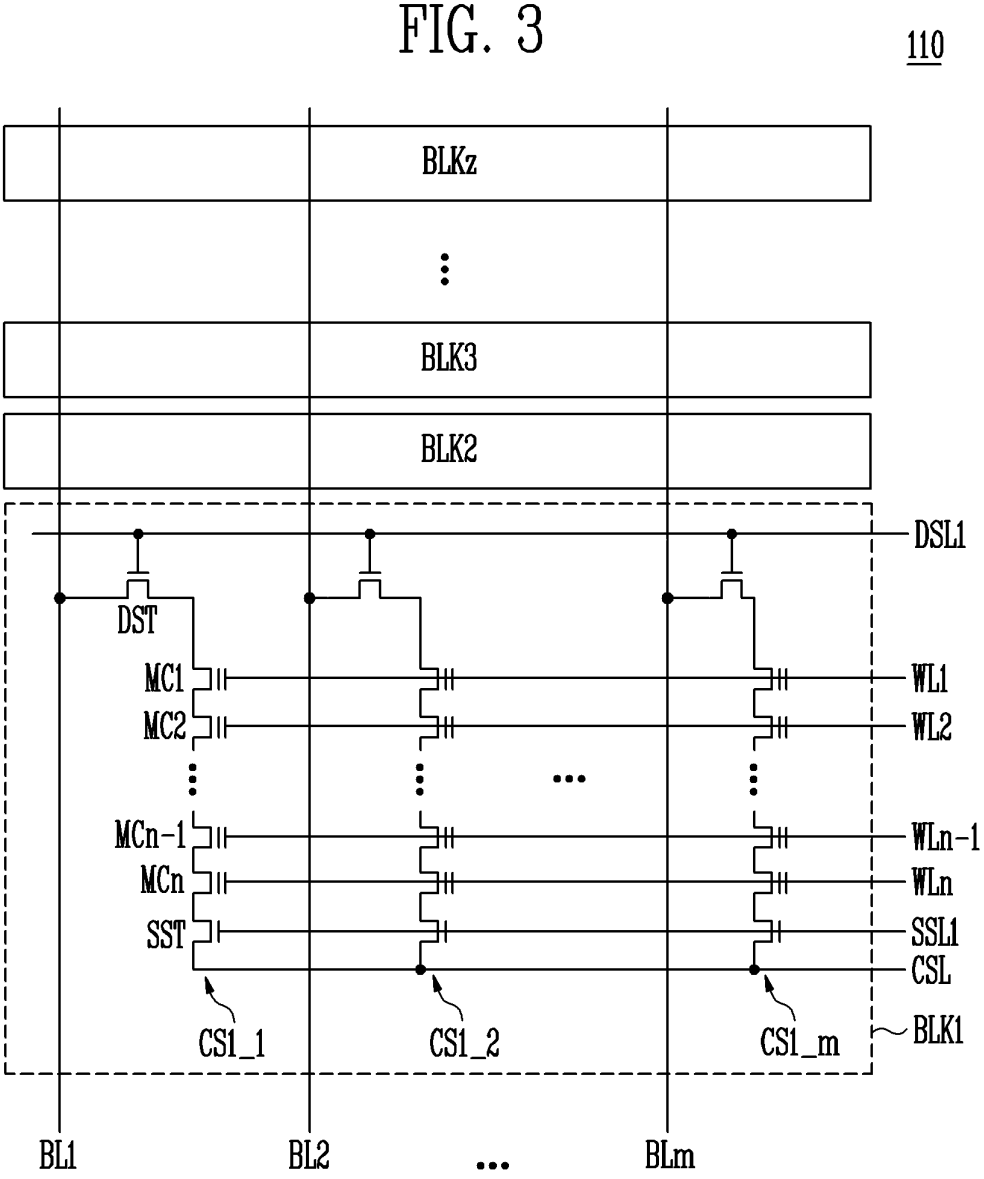

110
BLKz
BLK3
BLK2
DSL1
DST
MC1
MC2
MCn-1
MCn
SST
WL1
WL2
WLn-1
WLn
SSL1
CSL
CS1_1
CS1_2
CS1_m
BLK1
BL1
BL2
BLm

FIG. 4

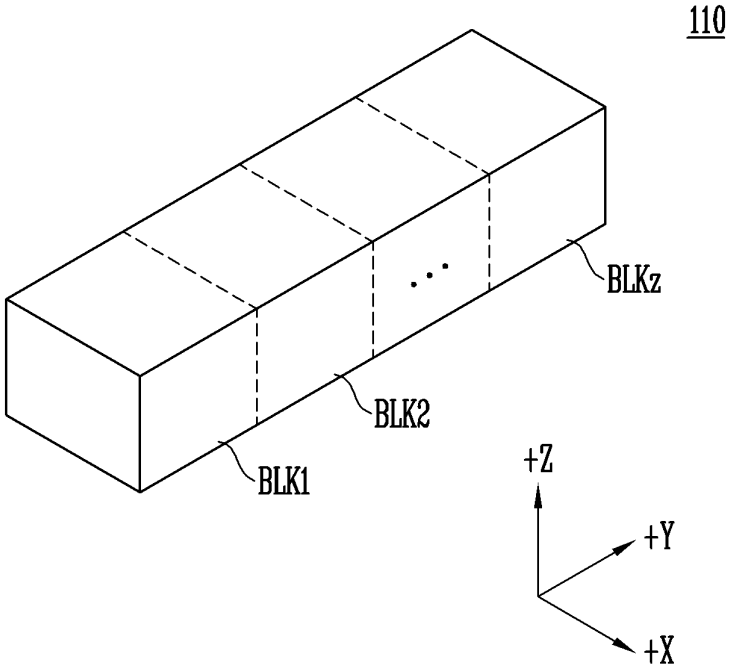


FIG. 5

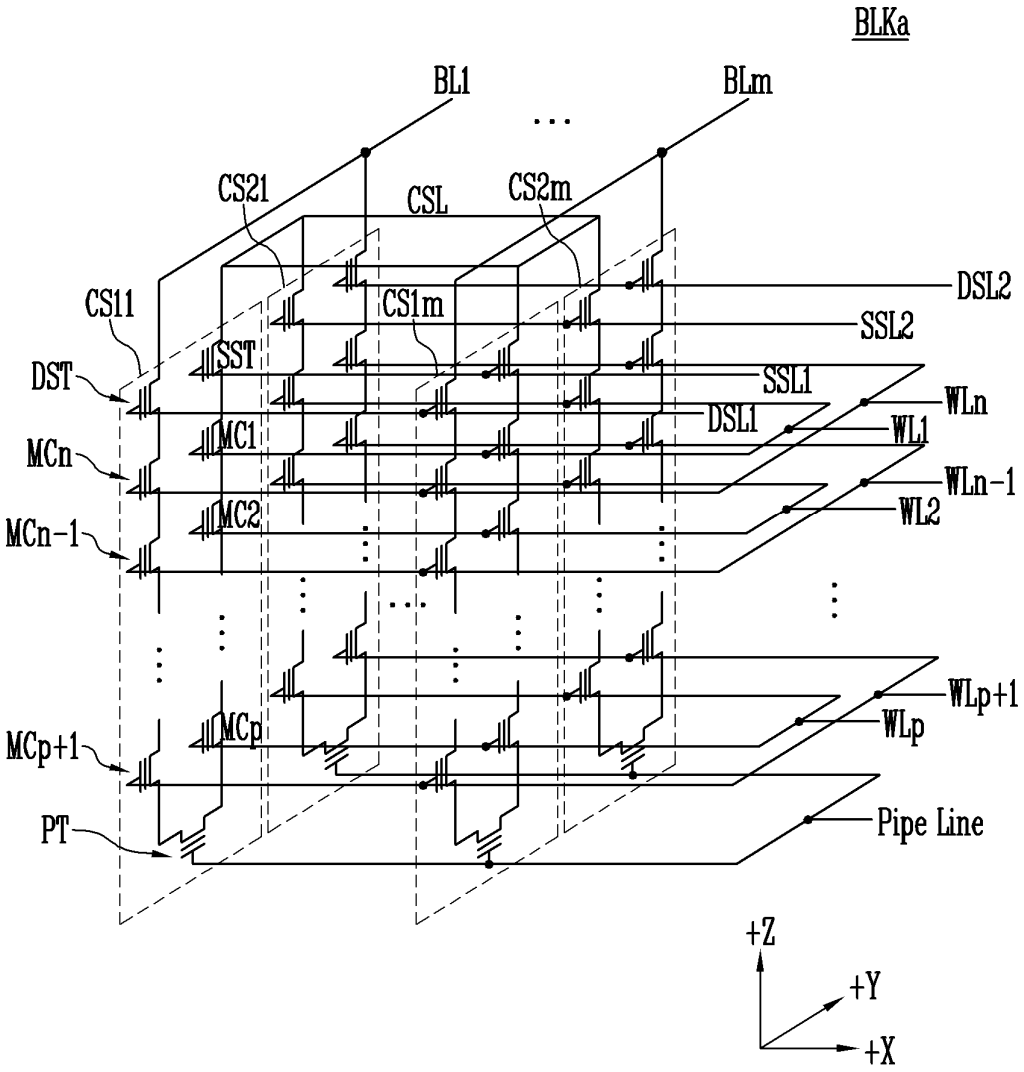

BLKa
BL1
BLm
CS21
CSL
CS2m
CS11
CS1m
DSL2
SSL2
SST
SSL1
DST
DSL1
WLn
MC1
WL1
MCn
WLn-1
MC2
WL2
MCn-1
WLp+1
MCp
WLp
MCp+1
PT
Pipe Line
+Z
+Y
+X

FIG. 6

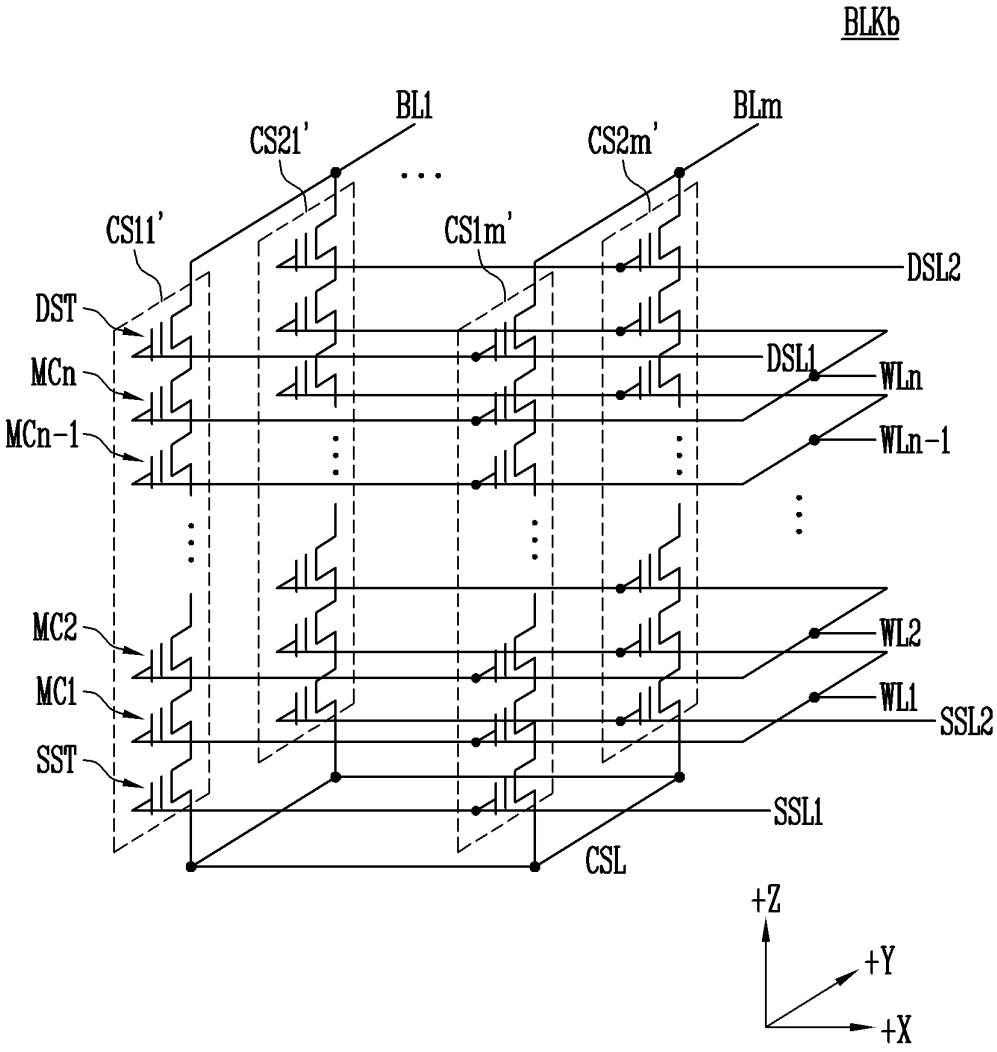

BLKb
BL1
BLm
CS21'
CS2m'
CS11'
CS1m'
DSL2
DST
DSL1
MCn
WLn
MCn-1
WLn-1
MC2
WL2
MC1
WL1
SSL2
SST
SSL1
CSL
+Z
+Y
+X

FIG. 7

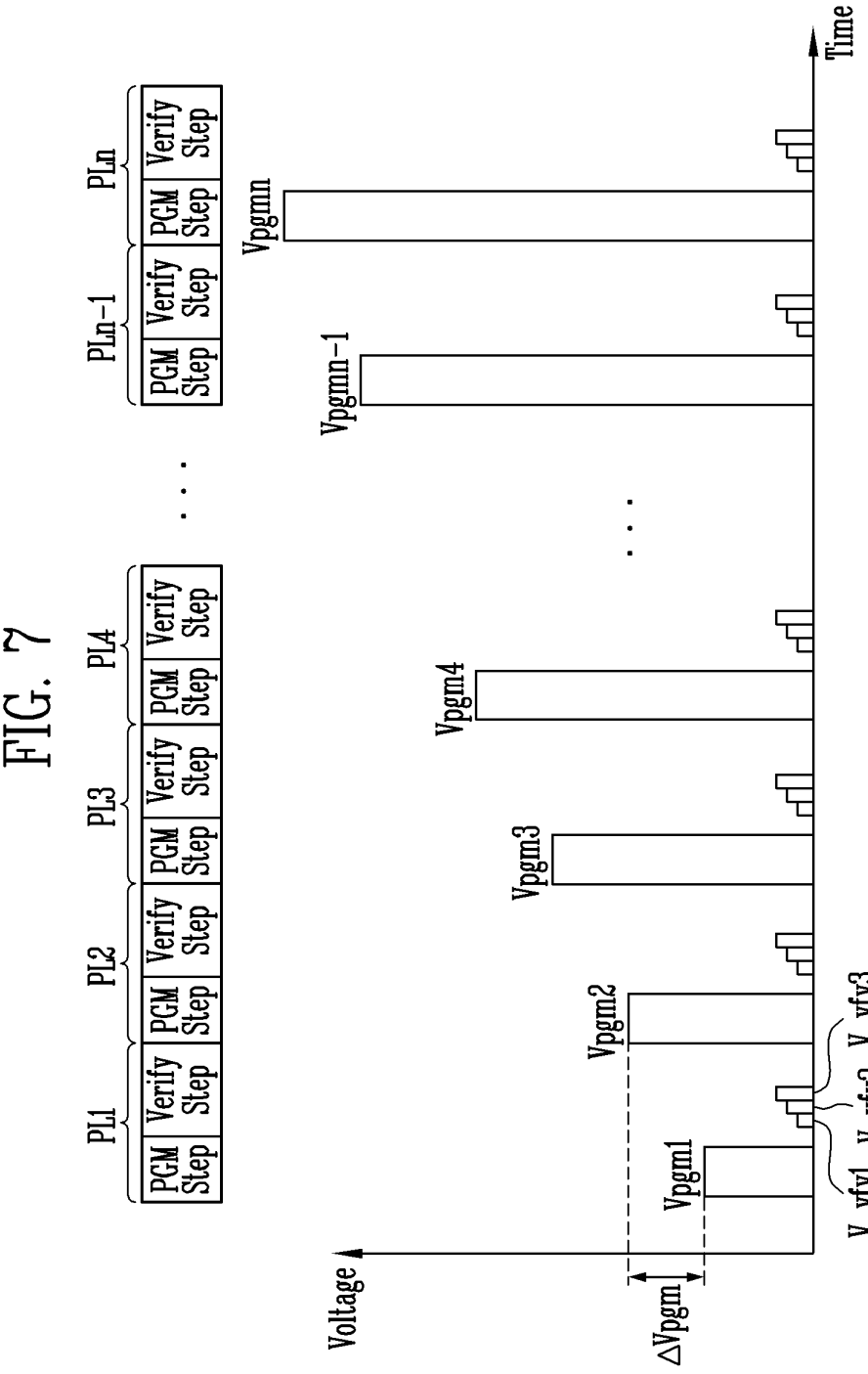

PL1
PL2
PL3
PL4
PLn-1
PLn
PGM Step
Verify Step
Vpgm1
Vpgm2
Vpgm3
Vpgm4
Vpgmn-1
Vpgmn
ΔVpgm
V_vfy1
V_vfy2
V_vfy3
Voltage
Time

FIG. 8

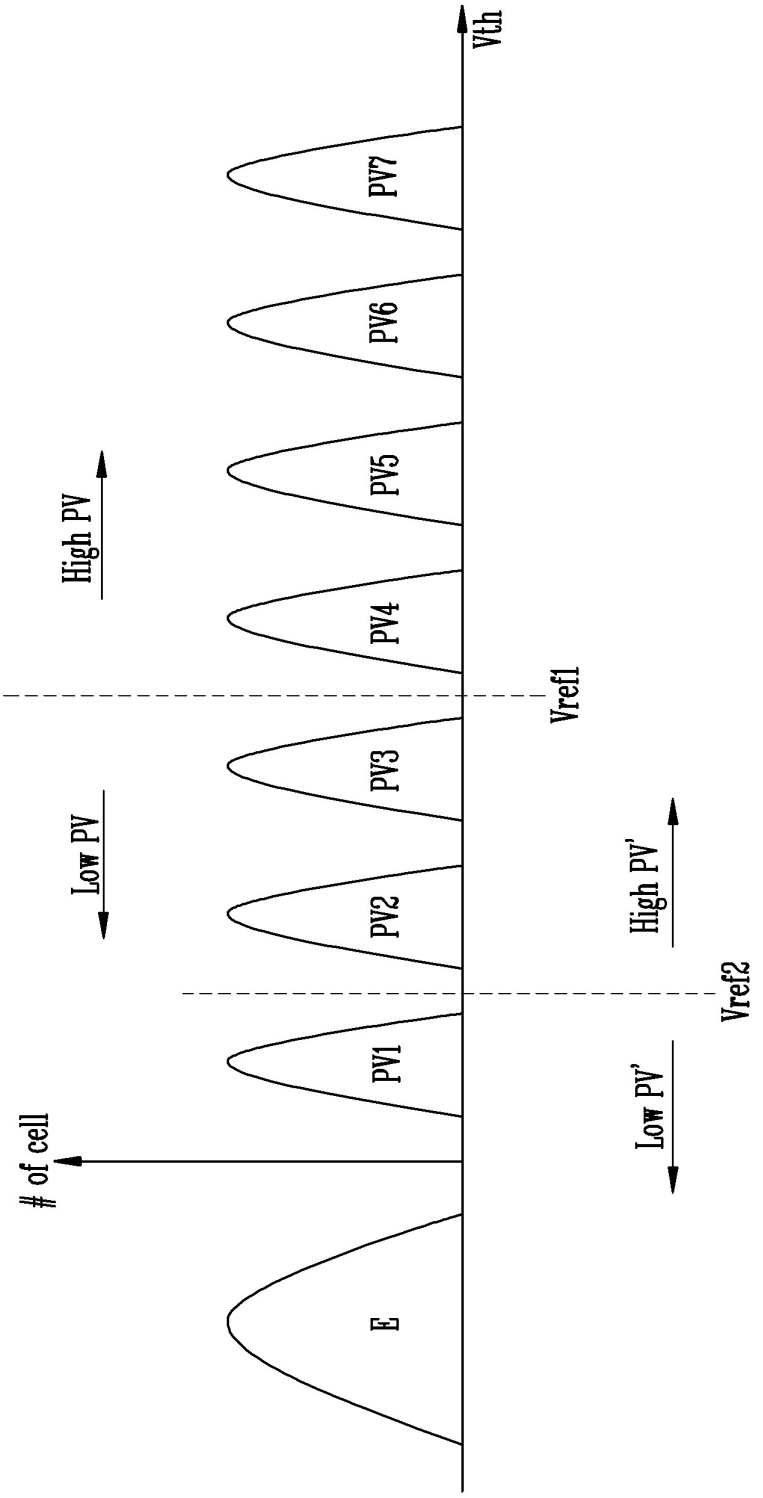

Vth
# of cell
E
PV1
PV2
PV3
PV4
PV5
PV6
PV7
Vref1
Vref2
High PV
Low PV
High PV'
Low PV'

FIG. 9

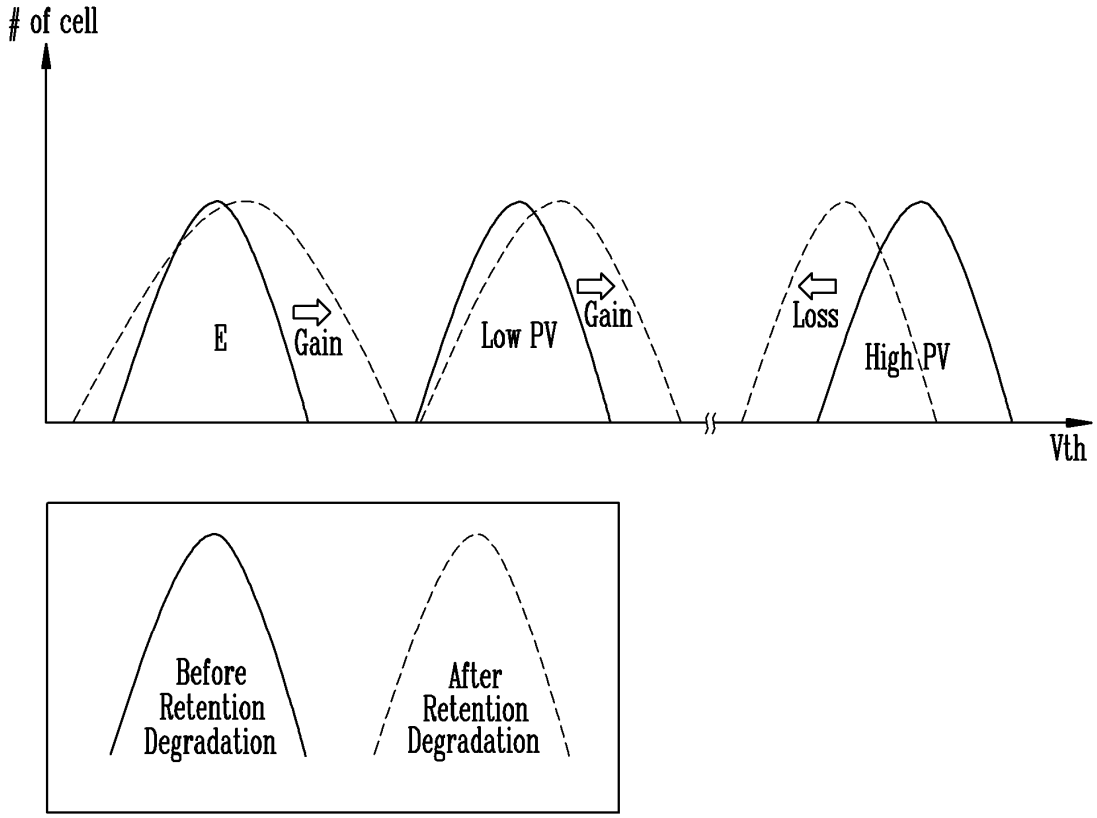

# of cell
E
Gain
Low PV
Gain
Loss
High PV
Vth
Before Retention Degradation
After Retention Degradation

FIG. 10

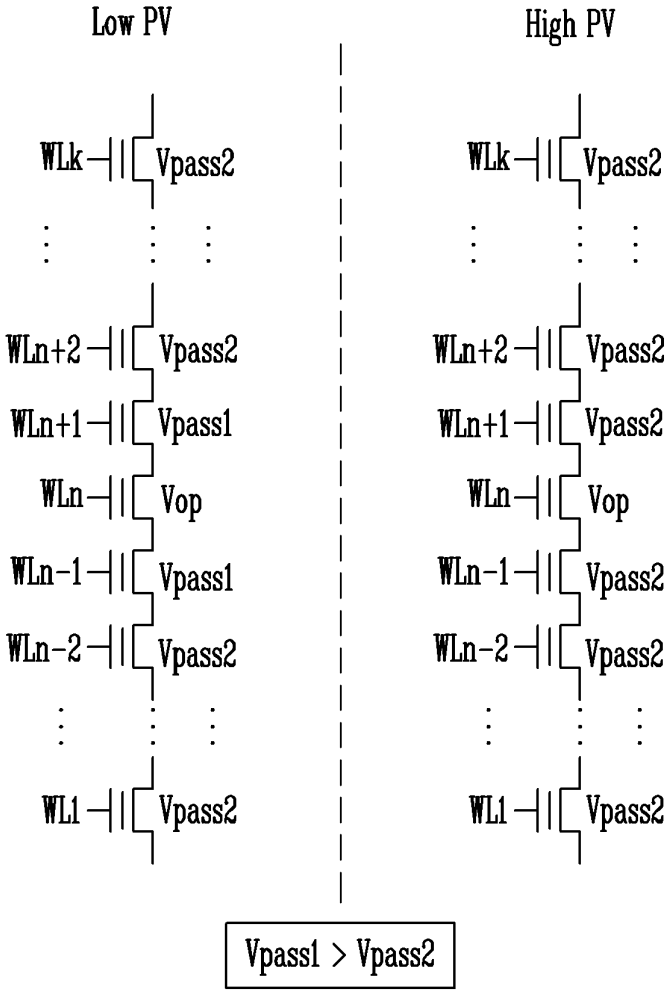

Low PV
High PV
WLk
Vpass2
WLn+2
Vpass2
WLn+1
Vpass1
WLn
Vop
WLn-1
Vpass1
WLn-2
Vpass2
WL1
Vpass2
WLk
Vpass2
WLn+2
Vpass2
WLn+1
Vpass2
WLn
Vop
WLn-1
Vpass2
WLn-2
Vpass2
WL1
Vpass2
Vpass1 > Vpass2

FIG. 11

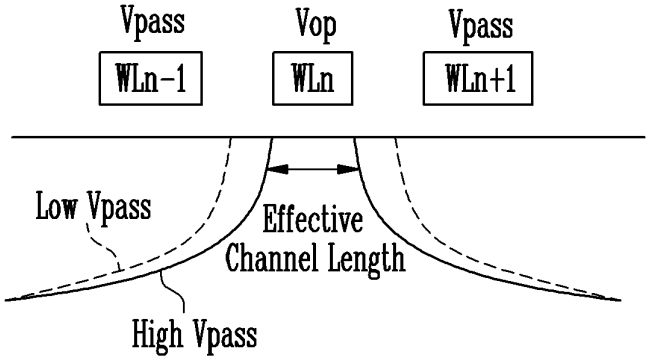

Vpass
Vop
Vpass
WLn-1
WLn
WLn+1
Low Vpass
Effective
Channel Length
High Vpass

FIG. 12

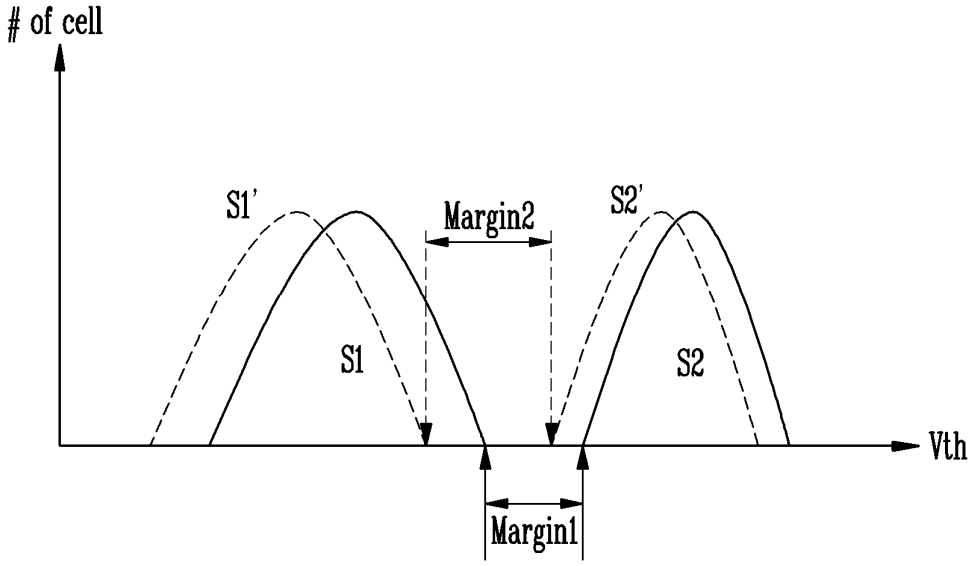

# of cell
S1'
Margin2
S2'
S1
S2
Vth
Margin1

FIG. 13A

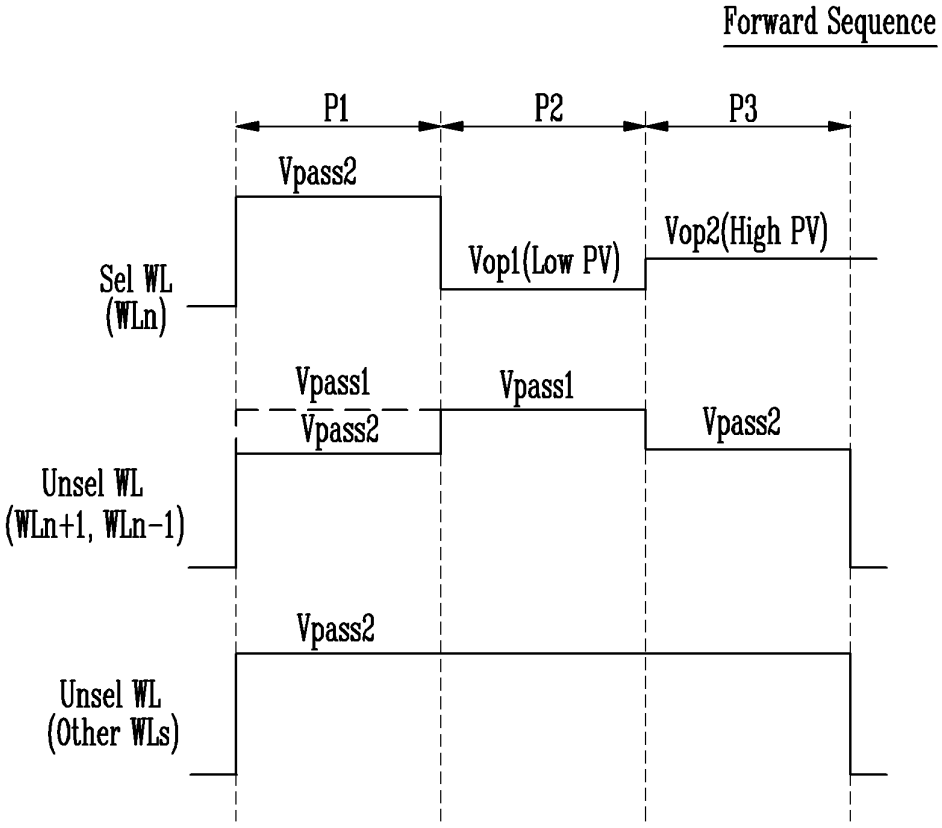

Forward Sequence
P1
P2
P3
Vpass2
Vop2(High PV)
Vop1(Low PV)
Sel WL
(WLn)
Vpass1
Vpass1
Vpass2
Vpass2
Unsel WL
(WLn+1, WLn-1)
Vpass2
Unsel WL
(Other WLs)

FIG. 13B

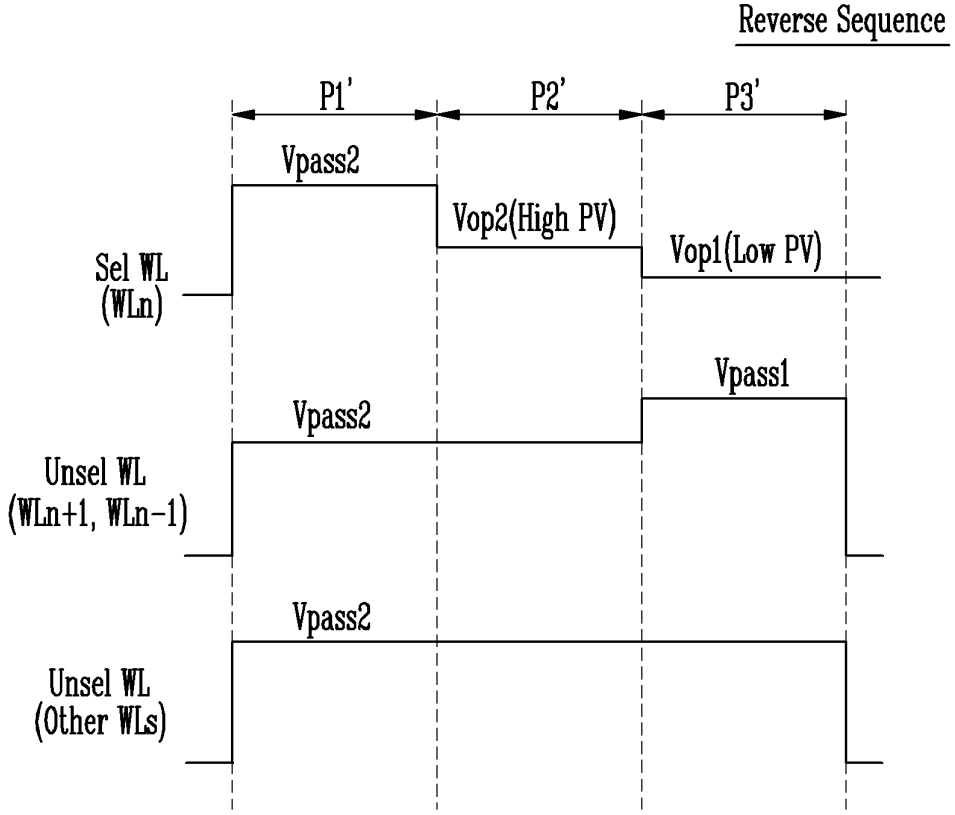

Reverse Sequence
P1'
P2'
P3'
Vpass2
Vop2(High PV)
Vop1(Low PV)
Sel WL
(WLn)
Vpass1
Vpass2
Unsel WL
(WLn+1, WLn-1)
Vpass2
Unsel WL
(Other WLs)

FIG. 14

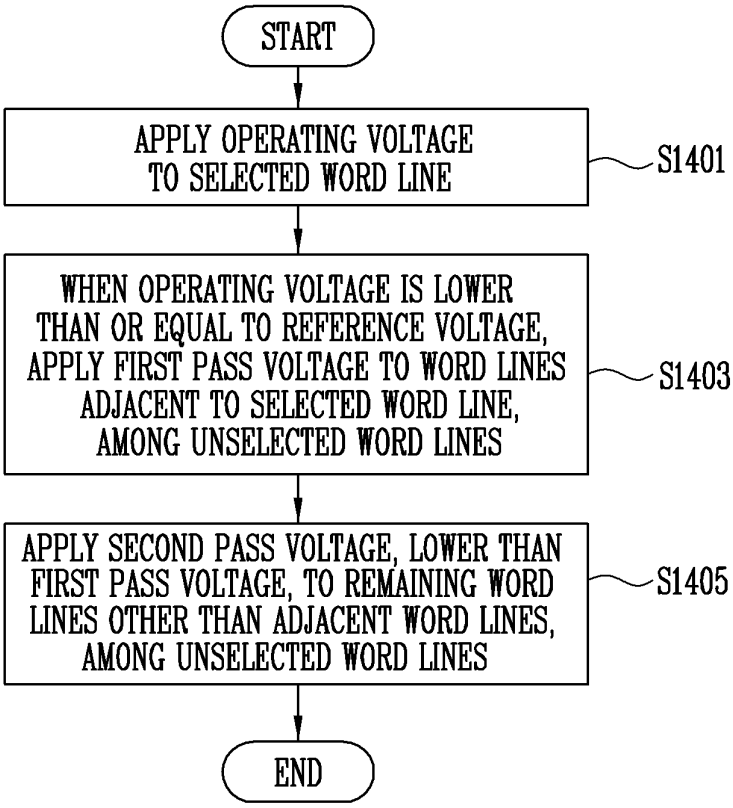
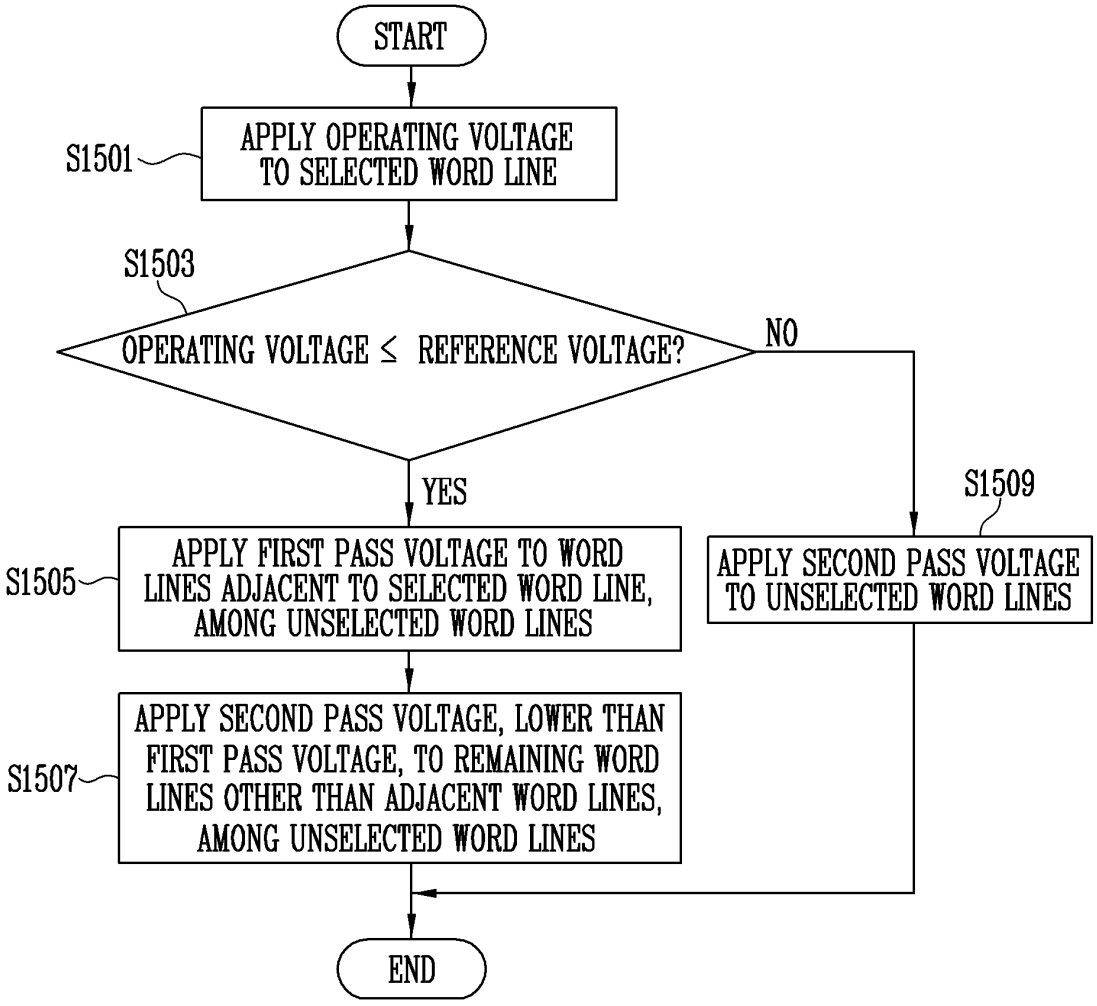

START
APPLY OPERATING VOLTAGE TO SELECTED WORD LINE
S1401
WHEN OPERATING VOLTAGE IS LOWER THAN OR EQUAL TO REFERENCE VOLTAGE, APPLY FIRST PASS VOLTAGE TO WORD LINES ADJACENT TO SELECTED WORD LINE, AMONG UNSELECTED WORD LINES
S1403
APPLY SECOND PASS VOLTAGE, LOWER THAN FIRST PASS VOLTAGE, TO REMAINING WORD LINES OTHER THAN ADJACENT WORD LINES, AMONG UNSELECTED WORD LINES
S1405
END

FIG. 15


START
S1501
APPLY OPERATING VOLTAGE TO SELECTED WORD LINE
S1503
OPERATING VOLTAGE ≤ REFERENCE VOLTAGE?
NO
YES
S1509
APPLY SECOND PASS VOLTAGE TO UNSELECTED WORD LINES
S1505
APPLY FIRST PASS VOLTAGE TO WORD LINES ADJACENT TO SELECTED WORD LINE, AMONG UNSELECTED WORD LINES
S1507
APPLY SECOND PASS VOLTAGE, LOWER THAN FIRST PASS VOLTAGE, TO REMAINING WORD LINES OTHER THAN ADJACENT WORD LINES, AMONG UNSELECTED WORD LINES
END