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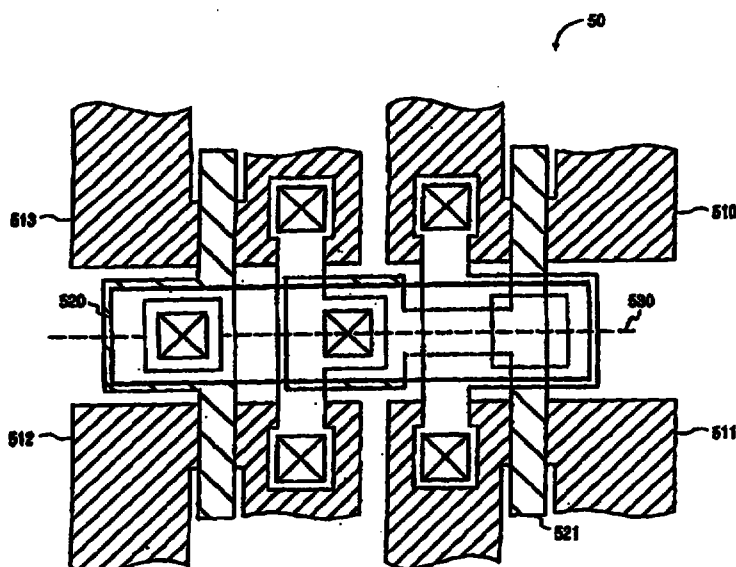
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(54) Title: **MEMORY CELL DESIGN WITH VERTICALLY STACKED CROSSOVERS**



(57) Abstract

A memory cell (50) with vertically stacked crossovers (520, 521). In prior memory cells, crossover connections within the memory cell were implemented in the same device layer. This wasted valuable design space, since the crossovers were therefore required to sit side-by-side in the layout design. The present invention implements crossovers in different materials on different device layers. The crossovers may therefore be vertically stacked on top of each other, reducing the area of the memory cell.