COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION

Field of the Invention

This invention relates generally to semiconductor devices, and more specifically to a copper interconnect structure within a semiconductor device and its method of formation.

Background of the Invention

In the semiconductor industry, conductive interconnects have traditionally been formed using aluminum. However, conductive interconnects having a resistance lower than that given by aluminum are now required to meet the speed requirements of advanced semiconductor devices. Copper has recently been proposed as a replacement for traditional aluminum interconnects because of its lower resistance. Copper unlike aluminum, is highly mobile in many of the materials that are currently used to fabricate semiconductor devices. Thus, the use of copper interconnects in semiconductor devices requires the use of copper barrier layers to prevent unwanted copper diffusion within the semiconductor device. Adhesion of the barrier layer to the copper interconnect, however, is problematic and frequently causes semiconductor devices to fail. Therefore, a need exists for a metallization process that allows semiconductor devices with improved reliably to be fabricated with copper interconnects.

Brief Description of the Drawings

FIGs. 1-7 illustrate, in cross-section, process steps in accordance with one embodiment of the invention.

Detailed Description of the Drawings

Shown in FIG. 1 is a portion 5 of a semiconductor device structure in accordance with one embodiment of the present invention. The semiconductor device structure comprises a semiconductor substrate 10, field isolation regions 12, a transistor 14, conductive plugs 24, a dielectric layer 22, an etch stop layer 26, and a dielectric layer 28. Transistor 14 comprises source/drain regions 16, a gate dielectric layer 18, and a gate electrode 20. In one embodiment, semiconductor substrate 10 is a monocrystalline silicon substrate. Alternatively, semiconductor substrate 10 may be a silicon-on-insulator substrate, a silicon-on-sapphire substrate, or the like.

In one embodiment, field isolation regions 12 are trench isolation regions which are formed using conventional etching and chemical mechanical polishing techniques. Alternatively, field isolation regions 12 may be field oxide regions which are formed using conventional techniques, such as local oxidation of silicon (LOCOS), poly-buffered LOCOS (PBL), polysilicon encapsulated local oxidation (PELOX), or the like.

In one embodiment, gate dielectric layer 18 is a layer of thermal silicon dioxide which is formed by thermally oxidizing a portion of semiconductor substrate 10. Alternatively, gate dielectric layer 18 may be a layer of silicon nitride, a layer of silicon oxynitride, a layer of chemically vapor deposited silicon dioxide, a nitrided oxide layer, or a combination thereof.

In one embodiment, gate electrode 20 is a layer of polysilicon. Alternatively, gate electrode 20 may be a metal layer, such as tungsten or molybdenum, a metal nitride layer, such as titanium nitride or tungsten nitride, or a combination thereof. In addition, gate electrode 20 may be a polycide layer comprising a metal silicide layer, such as tungsten silicide, titanium silicide, or cobalt silicide, overlying a polysilicon layer.

In one embodiment, dielectric layer 22 is a layer of plasma deposited oxide which is formed using TEOS as a source gas. Alternatively, dielectric layer 22 may be a layer of silicon nitride, a layer of PSG, a layer of BPSG, an SOG layer, a silicon oxynitride layer, a polyimide layer, or a combination thereof.

In one embodiment, conductive plugs 24 are formed using a titanium/ titanium nitride barrier layer and a tungsten contact fill. After being deposited portions of the tungsten and the underlying titanium/titanium nitride barrier layer are removed using conventional etching or chemical mechanical polishing techniques to form conductive plugs 24. Alternatively, conductive plugs 24 may be formed using polysilicon as a contact fill material.

In one embodiment, etch stop layer 26 is a layer of silicon oxynitride which is formed using conventional plasma deposition techniques. Alternatively, etch stop layer 26 may be a layer of plasma deposited silicon nitride, a boron nitride layer, or the like.

In one embodiment, dielectric layer 28 is a layer of plasma deposited oxide which is formed using TEOS as a source gas. Alternatively, dielectric layer 28 may be a layer of silicon nitride, a layer of PSG, a layer of BPSG, an SOG layer, a silicon oxynitride layer, a polyimide layer, or the like. In addition, a combination of the foregoing dielectric materials may also be used to form dielectric layer 28.

In FIG. 2, a portion of dielectric layer 28 and a portion of etch stop layer 26 are then removed to expose a portion of conductive plugs 24 and form interconnect openings 29. A conductive barrier layer 30 is then formed within interconnect openings 29. In one embodiment, conductive barrier layer 30 is a layer of tantalum nitride. Alternatively, conductive barrier layer 30 may be a layer of titanium nitride, a layer of tungsten nitride, a layer of tantalum silicon nitride, a layer of tantalum, a titanium-tungsten layer (TiW), or the like. Conductive barrier layer 30 may be deposited using conventional sputtering or chemical vapor deposition techniques.

A first copper layer 32 is then formed overlying conductive barrier layer 30. First copper layer 32 has a thickness which is insufficient to fill interconnect openings 29, as shown in FIG. 2. In one embodiment, first copper layer 32 is deposited using a sputter deposition process. Alternatively, first copper layer 32 may be formed using a chemical vapor deposition process.

An electroplating process is then used to form a second copper layer 34 overlying first copper layer 32. Second copper layer 34 has a thickness which is sufficient to fill interconnect openings 29, as shown in FIG. 2. In

one embodiment, second copper layer 34 is deposited using a plating solution comprising copper (Cu), copper sulfate (Cu_2SO_4), sulfuric acid (H_2SO_4), and chloride ions, such as those from hydrochloric acid (HCl). In this particular embodiment, the electric current density is modified near the edges of the semiconductor substrate during the copper electroplating process in order to improve the copper electroplating uniformity, as is described in U.S. patent application serial number 08/856,459, which is assigned to the assignee of the present application. The subject matter of U. S. patent application serial number 08/856,459 is expressly incorporated herein by reference. Alternatively, second copper layer 34 may be formed using other electroplating techniques and other electroplating solutions. In addition, second copper layer 34 may be formed using other techniques, such as chemical vapor deposition.

In FIG. 3, portions of second copper layer 34, first copper layer 32 and conductive barrier layer 30 are removed to form copper interconnects 39 within interconnect openings 29, wherein copper interconnects 39 comprise a remaining portion 36 of conductive barrier layer 30, a remaining portion 37 of first copper layer 32, and a remaining portion 38 of first copper layer 34. In particular embodiments wherein conductive barrier layer 30 comprises titanium, tungsten, or tantalum, copper interconnects 39 may be formed with a chemical mechanical polishing process that uses a polishing slurry comprising hydrogen peroxide, ammonium citrate, alumina, 1,2,4-triazole, and deionized water, as is described in U.S. patent application serial number 08/954,190, which is assigned to the assignee of the present application. The subject matter of U. S. patent application serial number 08/954,190 is expressly incorporated herein by reference. Alternatively, copper interconnects 39 may be formed using conventional etching techniques, such as ion-beam milling, reactive ion-beam etching, and plasma etching, or using a combination of etching and polishing techniques.

A copper barrier layer 40 comprising silicon and nitrogen is then formed overlying copper interconnects 39. Copper barrier layer 40 is used to prevent copper atoms within copper interconnects 39 from diffusing into dielectric layers which are subsequently deposited over copper interconnects 39. In one embodiment, copper barrier layer 40 has an absorption coefficient (k) that ranges from approximately 0.0 to

approximately 0.15 for photoresist exposure wavelengths at or below 365 nanometers. More specifically, copper barrier layer 40 has an absorption coefficient (k) that ranges from approximately 0.0 to approximately 0.15 at photoresist exposure wavelengths of 365 nanometers and 248 nanometers.

In order to improve the adhesion between copper interconnects 39 and copper barrier layer 40, copper interconnects 39 are exposed to a silicon-free plasma that comprises hydrogen. The silicon-free plasma comprising hydrogen is generated using a silicon-free source gas or silicon-free source gases that are supplied to the plasma chamber. For example, in one embodiment a silicon-free plasma comprising hydrogen is generated using only ammonia (NH_3) as a source gas to generate a plasma consisting essentially of hydrogen and nitrogen. In this particular embodiment, the plasma consisting essentially of hydrogen and nitrogen is generated under the following conditions: a deposition pressure of approximately 8.0 torr; an ammonia flow rate of approximately 400 sccm; an RF power of approximately 200 watts; a spacing of approximately 650 mils, and a deposition temperature of approximately 400 degrees centigrade. Alternatively, a silicon-free plasma comprising hydrogen may be generated using only hydrogen (H_2) as a source gas or using hydrogen in combination with an inert source gas, such as nitrogen (N_2), helium (He), or argon (Ar). It is believed that the plasma process removes copper oxide from the exposed surface of copper interconnects 39, which can degrade adhesion between copper barrier layer 40 and copper interconnects 39. Specifically, it is believed that hydrogen in the plasma reacts with copper oxide on the surface of the copper interconnect to form volatile water which is pumped away, and nitrogen in the plasma assists in the reduction of the copper oxide by impinging on the copper surface. In addition, by performing this cleaning process within the same chamber as the subsequent copper barrier layer deposition, the cleaned copper surface is not re-exposed to air and re-oxidized prior to deposition. It is important to note that the foregoing plasma process improves adhesion without degrading the resistance of the copper interconnect and without degrading the leakage current between adjacent copper interconnects.

In one embodiment, copper barrier layer 40 is a layer of silicon oxynitride ($Si_xO_yN_z$). In this particular embodiment, copper barrier layer 40 is formed in an Applied Materials Centura plasma deposition system mounted with a DXZ chamber using the following deposition conditions:

a deposition pressure of approximately 5.0 torr; a silane flow rate of approximately 73 sccm; a nitrous oxide flow rate of approximately 92 sccm; a nitrogen flow rate of approximately 3900 sccm; an RF power of approximately 500 watts; a spacing of approximately 475 mils, and a deposition temperature of approximately 400 degrees centigrade. At a photoresist exposure wavelength of approximately 365 nanometers the foregoing silicon oxynitride layer has a refractive index of approximately 1.66 and an absorption coefficient of approximately 0.0.

In an alternative embodiment, copper barrier layer 40 is a layer of plasma deposited silicon nitride (Si_xN_y). In this particular embodiment, copper barrier layer 40 is formed in an Applied Materials Centura plasma deposition system mounted with a DXZ chamber using the following deposition conditions: a deposition pressure of approximately 5.0 torr; a silane flow rate of approximately 100 sccm; an ammonia flow rate of approximately 140 sccm; a nitrogen flow rate of approximately 4000 sccm; an RF power of approximately 450 watts; a spacing of approximately 610 mils, and a deposition temperature of approximately 400 degrees centigrade. At a photoresist exposure wavelength of approximately 365 nanometers the foregoing silicon nitride layer has a refractive index of approximately 2.05 and an absorption coefficient of approximately 0.0.

It is important to note that copper barrier layer 40 may be reliably integrated with inlaid copper metallization because it adheres to copper interconnects 39 and because it does not adversely effect the resistance of copper interconnects 39 or the leakage current between adjacent inlaid copper interconnects. Specifically, it has been found that the leakage current between inlaid copper interconnects spaced approximately 2400 angstroms apart is less than one nanoampere when they are covered by copper barrier layer 40. Thus, the present invention also allows semiconductor devices having low leakage currents to be fabricated with copper interconnects.

In one embodiment, an antireflective layer 41 containing silicon and nitrogen is then formed abutting copper barrier layer 40. Antireflective layer 41 has a thickness ranging from approximately 5 nanometers to approximately 100 nanometers. Antireflective layer 41 has an absorption coefficient (k) that ranges from approximately 0.2 to approximately 1.0 for photoresist exposure wavelengths at or below 365

nanometers. Specifically, antireflective layer 41 has an absorption coefficient (k) that ranges from approximately 0.2 to approximately 1.0 at photoresist exposure wavelengths of 365 nanometers and 248 nanometers. Thus, for the same photoresist exposure wavelength, copper barrier layer 40 will have an absorptive coefficient which is less than the absorptive coefficient for antireflective layer 41.

In one embodiment, antireflective layer 41 is a layer of silicon oxynitride ($Si_xO_yN_z$). In this particular embodiment, antireflective layer 41 is formed in an Applied Materials Centura plasma deposition system mounted with a DXZ chamber using the following deposition conditions: a deposition pressure of approximately 5.0 torr; a silane flow rate of approximately 300 sccm; a nitrous oxide flow rate of approximately 92 sccm; a nitrogen flow rate of approximately 3900 sccm; an RF power of approximately 520 watts; a spacing of approximately 475 mils, and a deposition temperature of approximately 400 degrees centigrade. At a photoresist exposure wavelength of approximately 365 nanometers the foregoing silicon oxynitride layer has a refractive index of approximately 2.8 and an absorption coefficient of approximately 0.3.

It should be appreciated that the optical properties of copper barrier layer 40 and antireflective layer 41 may be individually tailored by adjusting their respective deposition processes. For example, if the silane flow rate used to deposit antireflective layer 41, discussed above, is changed to approximately 330 sccm this results in the silicon oxynitride layer having an absorption coefficient of approximately 0.40 at a photoresist exposure wavelength of approximately 365 nanometers. The absorptive coefficient of antireflective layer 41 increases because the higher silane flow rate increases the silicon concentration in the silicon oxynitride layer. Similarly, decreasing the silane flow rate will decrease the silicon concentration in the silicon oxynitride layer and decrease its absorption coefficient. Therefore, the optical properties of antireflective layer 41 and copper barrier layer 40 can be independently tailored. For example, copper barrier layer 40 can be formed to have a silicon concentration which is less than the silicon concentration of antireflective layer 41, and thus copper barrier layer 40 can have an absorptive coefficient which is less than that of antireflective layer 41 for the same photoresist exposure wavelength. In addition, it is noted that components other than silicon, oxygen, and nitrogen may be included in the silicon oxynitride layers used to form

copper barrier layer 40 and antireflective layer 41. Furthermore, components other than silicon and nitrogen may be included in the silicon nitride layer used to form copper barrier layer 40. For example, hydrogen may be present in these nitride layers.

An interlevel dielectric layer 48 is formed overlying antireflective layer 41. In one embodiment, interlevel dielectric layer 48 comprises dielectric layer 42, etch stop layer 44 and dielectric layer 46, as shown in FIG. 4.

Dielectric layer 42 may be a layer of plasma deposited oxide which is deposited using TEOS as a source gas. Alternatively, dielectric layer 42 may be a layer of PSG, a layer of BPSG, an SOG layer, a polyimide layer, a low dielectric constant insulator, or the like.

Etch stop layer 44 may be a layer of plasma deposited silicon oxynitride. Alternatively, etch stop layer 44 may be a layer of plasma deposited silicon nitride, a layer of born nitride, or the like.

Dielectric layer 46 may be a layer of plasma deposited oxide which is formed using TEOS as a source gas. Alternatively, dielectric layer 46 may be a layer of PSG, a layer of BPSG, an SOG layer, a polyimide layer, a low dielectric constant insulator, or the like. It should be appreciated that interlevel dielectric layer 48 need not be formed using different dielectric material. For example, interlevel dielectric layer 48 could be formed using a single dielectric material, such as plasma deposited oxide, PSG, BPSG, SOG, polyimide, a low dielectric constant insulator, or the like.

A photoresist mask 51 is then formed overlying dielectric layer 48. Photoresist mask 51 is formed using electromagnetic radiation having a selected photoresist exposure wavelength, such as 365 nanometers or 248 nanometers. It is important to note that antireflective layer 41 reduces reflective notching in photoresist mask 51 which can result when photoresist overlying highly reflective copper interconnects 39 is lithographically exposed. Photoresist mask 51 is then used to pattern a portion of underlying dielectric layer 48, as shown in FIG. 5. More specifically, a portion of dielectric layer 46 and etch stop layer 44 are removed to form an interconnect opening 52 within dielectric layer 48. Photoresist mask 51 is then removed after interconnect opening 52 has been formed.

In FIG. 6, a photoresist mask 53 is then formed overlying dielectric layer 48. Photoresist mask 53 is formed using electromagnetic radiation having a selected photoresist exposure wavelength, such as 365 nanometers or 248 nanometers. It is important to note that antireflective layer 41 reduces reflective notching in photoresist mask 53 which can result when photoresist overlying highly reflective copper interconnects 39 is lithographically exposed. Photoresist mask 53 is then used to pattern a portion of underlying dielectric layer 48, as shown in FIG. 6. More specifically, a portion of dielectric layer 42, antireflective layer 41, and copper barrier layer 40 are removed to form a via opening 54 that exposes a portion of copper interconnects 39. This also results in the formation of a dual inlaid opening 50 within dielectric layer 48, wherein dual inlaid opening 50 comprises interconnect portion 52 and via portion 54. Photoresist mask 53 is then removed after dual inlaid opening 50 has been formed within dielectric layer 48.

In FIG. 7, a second conductive barrier layer is then formed within dual inlaid openings 50. In one embodiment, the second conductive barrier layer is a layer of tantalum nitride. Alternatively, the second conductive barrier layer may be a layer of titanium nitride, a layer of tungsten nitride, a layer of tantalum silicon nitride, a layer of tantalum, a titanium-tungsten layer (TiW), or the like. The second conductive barrier layer may be deposited using conventional sputtering or chemical vapor deposition techniques.

A third copper layer is then formed overlying the second conductive barrier layer. The third copper layer has a thickness which is insufficient to fill dual in-laid openings 50, as shown in FIG. 7. In one embodiment, the third copper layer is formed using a sputter deposition process. Alternatively, the third copper layer may be formed using a chemical vapor deposition process.

An electroplating process is then used to form a fourth copper layer overlying the third copper layer. The fourth copper layer has a thickness which is sufficient to fill dual inlaid opening 50. In one embodiment, the fourth copper layer is deposited using a plating solution comprising copper (Cu), copper sulfate (Cu_2SO_4), sulfuric acid (H_2SO_4), and chloride ions, such as those from hydrochloric acid (HCl). In this particular embodiment, the electric current density is modified near the edges of the semiconductor

substrate during the copper electroplating process in order to improve the copper electroplating uniformity, as is described in U.S. patent application serial number 08/856,459, which is assigned to the assignee of the present application. The subject matter of U. S. patent application serial number 08/856,459 is expressly incorporated herein by reference. Alternatively, the fourth copper layer may be formed using other electroplating techniques and other electroplating solutions. In addition, the fourth copper layer may be formed using other techniques, such as chemical vapor deposition.

Portions of fourth copper layer, the third copper layer and the second conductive barrier layer are then removed to form copper interconnects 62 within dual inlaid openings 50, wherein copper interconnects 62 comprise a remaining portion 57 of the second conductive barrier layer, a remaining portion 59 of the third copper layer, and a remaining portion 60 of the fourth copper layer. In particular embodiments wherein the second conductive barrier layer comprises titanium, tungsten, or tantalum, copper interconnects 62 may be formed with a chemical mechanical polishing process that uses a polishing slurry comprising hydrogen peroxide, ammonium citrate, alumina, 1,2,4-triazole, and deionized water, as is described in U.S. patent application serial number 08/954,190, which is assigned to the assignee of the present application. The subject matter of U. S. patent application serial number 08/954,190 is expressly incorporated herein by reference. Alternatively, copper interconnects 62 may be formed using conventional etching techniques, such as ion-beam milling, reactive ion-beam etching, and plasma etching, or using a combination of etching and polishing techniques.

A copper barrier layer 64 comprising silicon and nitrogen is then formed overlying copper interconnects 62, as previously described in FIG. 3. If additional levels of interconnect are not required, then copper barrier layer 64 serves as a final device passivation layer and bond pad openings (not shown) are subsequently formed through it. Alternatively, if additional levels of interconnect are required then the steps described in FIG. 3 through FIG. 7 are repeated.

Thus it is apparent that there has been provided, in accordance with the present invention, a metallization process that allows semiconductor devices to be reliability fabricated using copper interconnects. Although the invention has been described and illustrated with reference to specific embodiments, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations may be made without departing from the spirit and scope of the invention. Therefore, it is intended that this invention encompass all variations and modifications as fall within the scope of the appended claims.

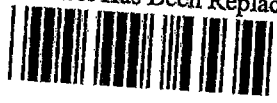


Claims

1. A method for forming a copper interconnect structure within a semiconductor device comprising the steps of:
providing a semiconductor substrate;
forming a dielectric layer overlying the semiconductor substrate;
patterning the dielectric layer to form an opening within the dielectric layer;
forming a copper layer overlying the semiconductor substrate, the copper layer lying within the opening;
polishing the copper layer to form a copper interconnect within the opening, the copper interconnect having an upper surface;
exposing the copper interconnect to a plasma comprising hydrogen to remove copper oxide from the upper surface of the copper interconnect and form a cleaned copper surface; and
forming a copper barrier layer overlying the cleaned copper surface, wherein the cleaned copper surface is not re-oxidized prior to forming the copper barrier layer.

2. A method for forming a copper interconnect structure within a semiconductor device comprising the steps of:
providing a semiconductor substrate;
forming a dielectric layer overlying the semiconductor substrate;
patterning the dielectric layer to form an opening within the dielectric layer;
forming a copper layer overlying the semiconductor substrate, the copper layer lying within the opening;
polishing the copper layer to form a copper interconnect within the opening, the copper interconnect having an upper surface;

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removing copper oxide from the upper surface of the copper interconnect to form a cleaned copper surface; and

forming a copper barrier layer overlying the cleaned copper surface.

3. A method for forming a copper interconnect structure within a semiconductor device comprising the steps of:

providing a semiconductor substrate;

forming a dielectric layer overlying the semiconductor substrate;

patterning the dielectric layer to form an opening within the dielectric layer;

forming a copper layer overlying the semiconductor substrate, the copper layer lying within the opening;

polishing the copper layer to form a copper interconnect within the opening, the copper interconnect having an upper surface;

exposing the copper interconnect to a plasma comprising hydrogen and nitrogen to remove copper oxide from the upper surface of the copper interconnect and form a cleaned copper surface; and

forming a copper barrier layer overlying the cleaned copper surface, wherein the cleaned copper surface is not re-oxidized prior to forming the copper barrier layer.

4. A method for forming a copper interconnect structure within a semiconductor device comprising the steps of:

providing a semiconductor substrate;

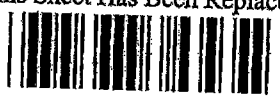
forming a dielectric layer overlying the semiconductor substrate;

patterning the dielectric layer to form an opening within the dielectric layer;

forming a copper layer overlying the semiconductor substrate, the copper layer lying within the opening;

polishing the copper layer to form a copper interconnect within the opening, the copper interconnect having an upper surface;

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exposing the copper interconnect to a silicon-free plasma comprising hydrogen to remove copper oxide from the upper surface of the copper interconnect and form a cleaned copper surface; and

forming a copper barrier layer overlying the cleaned copper surface, wherein the step of exposing the copper interconnect and the step of forming the copper barrier layer are performed in a same chamber.

5. A method for forming a copper interconnect structure within a semiconductor device comprising the steps of:

providing a semiconductor substrate;

forming a dielectric layer overlying the semiconductor substrate;

patterning the dielectric layer to form an opening within the dielectric layer;

forming a copper layer overlying the semiconductor substrate, the copper layer lying within the opening;

polishing the copper layer to form a copper interconnect within the opening, the copper interconnect having an upper surface;

exposing the copper interconnect to a plasma comprising hydrogen and nitrogen to remove copper oxide from the upper surface of the copper interconnect and form a cleaned copper surface; and

forming a copper barrier layer comprising silicon and nitrogen overlying the cleaned copper surface, wherein the step of exposing the copper interconnect and the step of forming the copper barrier layer are performed in a same chamber.

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