

PATENT SPECIFICATION

(11) 1 503 939

1 503 939

- (21) Application No. 9916/75, (22) Filed 10 March 1975,
(31) Convention Application No. 49/027115
(32) Filed 11 March 1974
(31) Convention Application No. 49/082185
(32) Filed 19 July 1974 in
(33) Japan (JP)
(44) Complete Specification published 15 March 1978
(51) INT CL² H03K 3/286 3/35
(52) Index at acceptance

H3T 1CX 1M2P 2J 2T2X 2T3F 2T3J 2T3TX 2T4 3J 3N 3X 4C
4D 5E



(54) SEMICONDUCTOR SWITCH/

(71) We, HITACHI, LTD., a Corporation of Japan, of 5-1, 1-chome, Marunouchi, Chiyoda-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a semiconductor switch.

Semiconductor switches of PNP construction (hereinafter referred to as a PNP switch) include PNP diodes with only an anode and a cathode taken out, three-terminal thyristors with a cathode gate control terminal taken out in addition to the anode and the cathode and also four-terminal thyristors with an anode gate control terminal taken out additionally. They are used with various control devices as a switch having a self-holding function.

These PNP switches, however, have the disadvantage that, in their cut-off state, they are undesirably closed (rendered conductive) upon application of a rapid forward voltage between their anode and cathode. This is known as the dv/dt effect or rate effect, and a number of methods have been suggested to avoid this phenomenon.

Some common methods consist in connecting a resistor between the cathode gate G_K and cathode K of the PNP switch or in connecting a resistor to the anode gate G_A of the PNP switch so that the switch is reverse biased between the anode A and anode gate G_A with an end of the resistor maintained at a high potential. In the former method, it is necessary to reduce greatly the resistance of the resistor in order to obtain a capability for prevention of the erroneous turning on of the PNP switch due to transient voltage (dv/dt) (this capability hereinafter being referred to as a dv/dt bearing capacity), due to the fact that the voltage drop across the resistor must not exceed the built-in voltage

between the cathode gate G_K and cathode K, even though the displacement current flows in the resistor through the junction capacity between the cathode gate and the anode gate. Assuming the junction capacity to be 2pF, for instance, the resistance value of the resistor must be lower than 600 Ω , if the dv/dt bearing capacity of 500 v/ μ s is to be achieved. As a result, the gate driving current and holding current are increased by the amount of current flowing in the resistor, leading to the disadvantage that in the case under consideration, for instance, a superfluous driving current of approximately 1mA is required. The latter method, on the other hand, requires that an end of the resistor be maintained at higher potential than the anode, and has the disadvantage that the device is capable of being protected when the anode changes to a higher potential whereas it is not when the cathode changes to a lower potential.

A conventional semiconductor switch is shown in Figs. 1 and 2 of the accompanying drawings and is as disclosed in the United States Patent No. 3,609,413. Incidentally, component elements in Fig. 1 and Fig. 2 are denoted by the same reference numerals as those in Fig. 1 and Fig. 3 of the drawings attached to the specification of the quoted patent.

By utilizing the junction capacity between an emitter 19 and the base of the transistor T_1 in the case of Fig. 1 and the capacitor 34 in the case of Fig. 2, a transient voltage applied to the anode is differentiated and the transistor T_1 , or T_2 , is energized in order to prevent the dv/dt effect of the PNP switch 10 (shown as SCR 10 in the quoted patent). In the circuit of Fig. 1 having an emitter 19, a base and another emitter 18 of the transistor T_1 , connected between the anode and cathode, the breakdown voltage of the base-emitter coupling is at most 5 to 10V, thus making this circuit usable only at about 5V or less, resulting in the loss of the advantage of a

50

55

60

65

70

75

80

85

90

PNPN switch that the breakdown voltage thereof is high both in positive and negative directions. By contrast, the circuit shown in Fig. 2 has the shortcoming of the difficulty encountered in producing it in the form of integrated circuitry since the capacitor 34 is included. Further, in applications of the circuits of Fig. 1 and Fig. 2 where pulses arriving at the anode at a high frequency and, say, 1ms in period are alternately used for firing and cutting off the device, useless charges remain in the base of the transistor T_1 or T_2 , resulting in the dv/dt bearing capacity being greatly reduced.

According to the present invention, there is provided a semiconductor switch comprising: a PNPN switch having at least three PN-junctions and having a P-type anode, an N-type gate, a P-type gate and an N-type cathode; switching means having input, output, and control terminals; a passive electrical element; and driver means for driving the control terminal of said switching means; the input and output terminals of said switching means and said passive element both being connected in parallel across one of said PN-junctions at one end of said PNPN switch, with said driver means arranged to supply to the control terminal of said switching means a current derived from a current flowing through a PN-junction at the other end of said PNPN switch thereby driving said switching means.

The invention will be further described with reference to the accompanying drawings, in which:

Fig. 1 and Fig. 2 are circuit diagrams showing conventional semiconductor devices;

Fig. 3 is a diagram showing an equivalent circuit of the semiconductor switch according to a first embodiment of the present invention;

Fig. 4 is a circuit diagram equivalent to Fig. 3 and showing the case where the PNPN transistor becomes active in response to a step voltage applied to the anode thereof;

Fig. 5 is a diagram showing an equivalent circuit of second embodiment of semiconductor switch according to the invention wherein the two transistors are of multi-collector construction;

Fig. 6 is a partial sectional view of the circuit of Fig. 5 wherein part of the circuit is integrated;

Fig. 7, 8 and 9 are diagrams showing equivalent circuits of third, fourth and fifth embodiments of the semiconductor switch according to the invention;

Fig. 10 is a diagram showing an equivalent circuit of a sixth embodiment of the invention used as a bidirectional speech path switch including a plurality of

semiconductor switches of the invention connected in parallel in opposite directions;

Fig. 11 is a partial sectional view of the circuit of Fig. 10 part of which is integrated; and

Fig. 12 shows waveforms of AC current and voltage in the case where a capacitive load is inserted.

In Fig. 3, showing a diagram of an equivalent circuit of a first embodiment of the semiconductor switch according to the invention, reference symbols Q_1 and Q_2 show an NPN transistor and a PNP transistor respectively constituting a PNPN switch, symbols Q_3 and Q_4 transistors, and R_1 and R_2 resistors, which, together with the transistors Q_3 and Q_4 , make up an active circuit and are connected in parallel to the PNPN switch. Symbol E shows a power supply, and symbol R a series resistance of the line in which the switch is inserted.

This PNPN switch has a positive feedback loop extending from the base of transistor Q_1 via the collector of transistor Q_1 , the base of transistor Q_2 and the collector of transistor Q_2 back to the base of transistor Q_1 . Upon receipt of a gate current, the transistors Q_1 and Q_2 enter an active state, and when the gain of the positive feedback loop reaches one or more, the device is rapidly switched, so that both the transistors Q_1 and Q_2 are turned on at the same time. As a result, the circuit between the anode A and cathode K conducts, and this conductive state is maintained.

As shown in the drawing, the semiconductor switch has also a negative feedback loop extending from the base of transistor Q_4 via the collector of transistor Q_4 , the base of transistor Q_3 , the collector of transistor Q_3 and the base of transistor Q_1 back to the base of transistor Q_4 . If this complicated circuit including both positive and negative feedback loops at the same time is to effect a switching operation with a feedback action of a loop gain of one or more the determinant of the circuit of Fig. 3 must be negative. Let the current gains of the transistors Q_1 , Q_2 , Q_3 and Q_4 be β_1 , β_2 , β_3 and β_4 respectively, and the condition for a negative circuit determinant of the circuit of Fig. 3 is approximately expressed by

$$\beta_1(\beta_2 - \beta_3\beta_4) - 1 > 0 \quad (1)$$

It will be seen that the left side of this inequality (1) represents an effective positive feedback gain. When the characteristics of the transistors are determined to satisfy this condition, the switching operation of the whole circuit of Fig. 3 is made possible. The negative feedback circuit compensates for the

variations in current gain resulting from possible variations in temperature or quality of product lots, thus bringing about a stable effective positive feedback gain.

As to the protection against the dv/dt effect, the state of the circuit when a transient voltage is impressed may be discussed with reference to Fig. 4. Since the base and emitter of transistors Q_1 and Q_2 of Fig. 3 are short-circuited with each other through resistors R_2 and R_1 , respectively, neither the transistor Q_1 nor transistor Q_2 operates until the voltage drop in the resistors R_2 and R_1 reaches to the turn-on voltage thereof (generally, approximately 0.6V). Therefore, by way of explanation, the transistors Q_1 and Q_2 are omitted from the circuit of Fig. 4. In this drawing, the capacitance C_1 is a junction capacitance between the base and collector of the transistor Q_4 , and the capacitance C_2 a junction capacitance between the base and collector of the transistor Q_3 . Referring to the closed state of switch S , the following approximate inequality (2) must be satisfied in order that the potential at the terminal 3 is always higher in the transient state than that at the terminal 4:

$$C_1 R_1 > \frac{(1+\beta_2)}{(1+\beta_4)} C_2 R_2 \quad (2)$$

In other words, the condition that the potential at the terminal 3 is always higher than that at the terminal 4 in Fig. 4 is equivalent to the fact in Fig. 3 that, before the potential at the terminal 4 reaches to the turn-on voltage of the transistor Q_1 , if ever, the potential at the terminal 3 takes a sufficient value to energize the transistor Q_3 . Therefore, by determining the circuit constants to satisfy the inequality (2), the transient current flowing from the collector of the transistor Q_2 , namely, the current supposed to flow in the base of the transistor Q_1 , bypasses the transistor Q_1 and flows into the transistor Q_3 in a saturated state. As a result, the transistor Q_1 is not turned on, so that the whole circuit of Fig. 3 is maintained in nonconducting state, thus achieving a great stability against a transient state. This advantage is attained without any power supply or other external control circuit or even when the anode potential changes to a high level or the cathode potential is decreased.

As will be understood from the foregoing description, the circuit of Fig. 3 satisfying both the inequalities (1) and (2) at the same time has the following advantages:

(a) A very great dv/dt bearing capacity is

achieved regardless of the potential at the anode or cathode;

(b) In view of the fact that the absolute value of the ratio between the values of resistors R_1 and R_2 , expressed by the inequality (2) can be selected as desired, the value of the resistor R_2 may be rendered very high as compared with the conventional devices, with the result that the circuit is capable of being triggered with very high sensitivity by applying a gate current to the base of transistor Q_1 .

(c) The fact that the ratio between the resistance values of resistors R_1 and R_2 is constant offers a great convenience in integrating the circuits and provides a stable circuit against any possible variations in resistance due to variations in the quality of product lots.

(d) Due to the fact that the circuit comprises component elements facilitating circuit integration and that the transistors Q_3 and Q_4 are connected in the same mode of polarity as the transistors Q_1 and Q_2 making up the original PNP switch, the advantage that the PNP switch has a high breakdown voltage both in positive and negative directions remains unlost.

(e) The fact that the connection of transistors Q_1 and Q_2 is substantially similar to that of transistors Q_3 and Q_4 permits the circuit to operate always stably even against high speed pulses applied thereto.

An additional qualitative description will be made of the semiconductor switch according to the first embodiment of the invention shown in Fig. 3. In the embodiment under consideration, the transistors Q_3 and Q_4 function to correct the effective positive feedback gain and, during the transient time, the transistor Q_3 causes the PNP switch to be shortcircuited between the cathode gate G_K and the cathode K . The resistor R_2 determines on one hand a gate sensitivity, but contributes to dv/dt bearing capacity against a slow rise of a voltage or a small dv/dt value so that it is possible to use a high resistance value of resistor R_2 . The resistor R_1 , on the other hand, contributes to providing the circuit with a necessary time constant. By the way, the resistor R_1 may be increased substantially infinitely in value or eliminated in so far as it suffices if the inequality (2) is satisfied. The results of tests conducted by the inventor show that the PNP switch and an incidental active circuit having the transistor characteristics of $\beta_1 = \beta_2 = 20$, $\beta_3 = 1.5$, $\beta_4 = 0.05$ and $C_1 = C_2 = 2pF$ were 500 $v/\mu s$ or more in dv/dt bearing capacity in the presence of resistors R_1 of about 50 $K\Omega$ and R_2 about 20 $K\Omega$, resulting in the gate sensitivity of about 30 μA . This compares with a low (approximately 15 $v/\mu s$) dv/dt bearing

capacity in the case where the same gate sensitivity is obtained by inserting a resistor between the cathode gate G_K and cathode K of the PNP switch as in the prior art. Thus, the dv/dt bearing capacity has been improved about 30 times by the invention. By the way, in determining the value of the time constant of the circuit by the resistor R_2 , the prevention of erroneous turning on of the PNP switch by leak current at high temperatures is another factor to be taken into consideration.

The diagram of Fig. 5 shows an equivalent circuit of the semiconductor switch according to the second embodiment of the invention, in which the transistors Q_2 and Q_4 in the circuit of Fig. 3 are replaced by a multi-collector transistor which is quite suitable for the purpose of circuit integration.

Referring to Fig. 6 showing a partial sectional view of the construction of integrated circuits including the transistors Q_1 , Q_2 and Q_4 of the equivalent circuit shown in Fig. 5, reference numeral 4 shows an anode gate region, numeral 5 a cathode gate region, numeral 6 a cathode region, numeral 7 an anode region, numeral 8 an anode gate contact region, and numeral 9 the collector region of the transistor Q_4 . The NPN transistor Q_1 is made up of the regions 4, 5 and 6; the lateral PNP transistor Q_2 of the regions 7, 4 and 5; and the lateral PNP transistor Q_4 of the regions 7, 4 and 9. If a high breakdown voltage is to be obtained while employing lateral transistors as in the case of Fig. 6, the current gain of the transistor Q_2 is small and therefore the current gain of the transistor Q_4 is very small value as derived from the inequality (1). Under this condition, the capacity of C_1 may be any other capacitive element than a junction capacity of transistors if its value satisfies the inequality (2).

In view of the fact that the inequality (2) is satisfied even if β_4 is made zero by eliminating the transistor Q_4 , the same effective operation as that of the circuit of Fig. 6 may be performed by inserting the capacitor C_1 capable of satisfying the inequality (2) in place of the transistor Q_4 . In other words, the same advantage results from inserting a capacitive element between the base of transistor Q_2 and the base of the transistor Q_3 of the circuit shown in Fig. 5.

An equivalent circuit of the semiconductor switch according to the third embodiment of the invention is shown in Fig. 7, wherein a diode D is inserted between the base of the transistor Q_2 and the base of the transistor Q_3 .

The equivalent circuit of the semiconductor switch according to the fourth embodiment of the invention as

shown in Fig. 8 is characterized by the capacitor C inserted between the base of the transistor Q_2 and the base of the transistor Q_3 . Incidentally, the capacitor C_g in the drawing which is connected in parallel to the resistor R_2 is for protecting the circuit from the transient voltage applied from the gate terminal G_K .

The diagram of Fig. 9 shows an equivalent circuit of the semiconductor switch according to the fifth embodiment of the invention, in which the short-circuiting transistor Q_3 in the equivalent circuit according to the first embodiment of the invention shown in Fig. 3 is connected to the PNP transistor Q_2 side, and which operates in the same manner as the circuit of Fig. 3.

Fig. 10 shows the sixth embodiment of the invention, which is used as a speech path switch having bidirectional characteristics by connecting a plurality of semiconductor switches according to the invention, and shows an equivalent circuit simulating the case in which a ringing signal of the telephone is passed.

In the drawing under consideration, reference symbols Q_1 and Q_2 show PNP and NPN transistors respectively making up the PNP switch, symbol Q_3 a switching transistor for protection of the device from the dv/dt effect, and symbol Q_4 a PNP transistor comprising a P-type anode and N-type cathode which is produced by forming another P-type region in the anode gate region of the PNP switch. Symbol Q_5 shows an insulated-gate field effect transistor for voltage control, symbol R_2 a resistor for protecting the device from a small dv/dt effect, and symbol R_1 a resistor for preventing the transistor Q_3 from being turned on under normal operating conditions or due to a small dv/dt effect and at the same time serving as a discharge path of the stored charges. Reference numeral 21 shows a cathode gate driving circuit, numeral 22 a signal source, numeral 23 a capacitive load, and numeral 24 an insulated-gate driving circuit for the insulated-gate field effect transistors Q_5 . The circuit of Fig. 10 refers to the PNP switch in a single stage, as the operating principle is the same regardless of the number of stages in which the PNP switches are connected.

Reference is made to Fig. 11 showing a partial sectional view of an example of the construction of the device of Fig. 10, in which the transistors Q_1 , Q_2 , Q_3 and Q_4 are included in integrated circuits. In the drawing in question, reference numeral 4 shows an anode gate region, numeral 5 a cathode gate region, numeral 6 a cathode region, numeral 7 an anode region, and numeral 8 an N^+ -type region for reducing

the emitter-grounded current gain h_{FE} of the transistor Q_4 and used for taking out an anode gate electrode. Reference numeral 9 shows a collector region of the transistor Q_4 , numeral 1 an oxide film, numeral 2 an aluminum electrode, symbol A an anode electrode, symbol G_K a cathode gate electrode, symbol K a cathode, GI the gate electrode of the field effect transistor Q_3 , and symbol Q_{4C} the collector electrode of the transistor Q_4 .

Let us consider the case in which the switches S_1 and S_2 are closed to allow an AC signal to pass the PNP switch as shown in Fig. 10. Under this condition, the waveform of current $i(t)$ leads in phase the voltage waveform $v(t)$ by a maximum phase difference of about 90° as shown in the diagram of Fig. 12. When the current $i(t)$ is reduced to a point below a self-holding level where the gate current must be supplied to maintain the current, the cathode voltage is at a positive or negative maximum or thereabouts. In the event that the cathode voltage level is negative, the gate current is capable of being supplied even if the driving voltage of the cathode gate driving circuit 21 is low. In this case, the field effect transistors Q_3 are unable to be turned on with a low driving voltage. On the contrary, at a positive level of the cathode, supply of current from the cathode gate driving circuit 21 requires a high voltage. Since each of the substrate of the field effect transistors Q_3 is at a high positive potential, however, the field effect transistors Q_3 are capable of being turned on and hence current can be supplied from the anode terminal to cathode gate, by applying a low negative driving voltage from the insulated gate driving circuit 24 to the insulated gate of the field effect transistors Q_3 . Also, in the case where the load 23 is inductive, the device can be easily driven by way of the field effect transistor at a positive cathode level, or by way of the cathode gate at a negative cathode level. In spite of the fact that the driving circuit 24 of the field effect transistor is shown in the form of a negative power supply in the circuit of Fig. 10, the gate may of course be maintained at earth level if the threshold voltage V_{th} of the field effect transistor is reduced, or alternatively, the device may be driven with a low positive voltage from a positive power supply. Further, the driving circuits 21 and 24 may take the form of pulse-producing driving circuits.

Furthermore, since the anode gate is also used as a current control terminal, three additional configurations are available based on different combinations of the current control element and the voltage control element. Such possibilities include a method in which the anode gate is used as

the current control element and the voltage control is made by connecting an N-channel field effect transistor between anode gate and cathode; a method in which the cathode gate is used as the current control element and a P-channel field effect transistor is inserted between anode gate and cathode; or a method in which the anode gate is used as the current control terminal and an N-channel field effect transistor is inserted between the anode and cathode gate. Each of these field effect transistors may be integrated with the PNP switch as shown in Fig. 11 or alternatively be provided separately.

Next, let us consider the case in which the voltage transient dv/dt is applied between the anode and cathode when the PNP switch of Fig. 10 is in cut-off state. First, when a large dv/dt is involved, the base current flows to the transistor Q_3 through the base-collector junction of the transistor Q_4 whereupon the transistor Q_3 is turned on, so that, by absorbing the current flowing through the base-collector junction of the transistor Q_4 in the saturated region of the transistor Q_3 , it is possible to prevent the PNP switches Q_1 and Q_2 from being closed. On the contrary, the PNP switch will be unable to be closed in the event that the transistor Q_3 conducts in the saturated region even under the normal operating condition. Therefore, to prevent such a situation, a resistor R_2 is inserted between the base and emitter of the transistor Q_3 . As a result, the transistor Q_3 is not turned on when a small dv/dt is applied, in which case the resistor R_1 is used for protection. In this way, unlike the conventional device, the resistor R_1 may be used to protect the device from a small dv/dt effect and therefore increased in resistance, with the result that the PNP switch may be closed with a small cathode gate current. In view of the fact that the transistor Q_3 may be operated only during the transient period when the dv/dt is applied, the circuit for supplying a base current thereto may take the form of a capacitive element, and either a diode or a capacitor may be employed in place of the transistor Q_4 . Of course, the capacitive elements may be connected in parallel to the resistor R_1 . Further, the device according to the invention may be arranged in a configuration based on the same operating principle as that of the preceding embodiments or such that a transistor for dv/dt protection and an impedance element may be inserted between the anode and anode gate of the PNP switch, so that the transistor for dv/dt protection may be driven by a capacitive element.

As will be understood from the foregoing description, in the above embodiments of

70

75

80

85

90

95

100

105

110

115

120

125

130

semiconductor switch the active circuit network inserted in parallel to the PNPN switch, together with part of the positive feedback loop of the PNPN switch, makes up a negative feedback circuit; and a current substantially in phase with the current flowing in the base resistor R_2 of the transistor Q_1 through the PNP transistor Q_2 including the junction capacitance C_j is rendered to flow in the parallel-connected active circuit network, so that the base current if the transistor Q_1 is bypassed by the transistor Q_2 , whose collector is connected to the base of the transistor Q_1 , thus making it possible to maintain the effective DC positive feedback loop gain of the whole device more than one.

Furthermore, in Figure 10 the PNPN switch is provided with a voltage control terminal taking advantage of a field effect transistor, which, in combination with a conventional current control system, permits the PNPN switch to be closed with a small control voltage even against floating of the cathode potential level. In addition, the parallel connection of an impedance element and a switching element for protection of the device from the dv/dt effect makes possible a PNPN switch with a large dv/dt bearing capacity which is capable of being closed with a small control current.

WHAT WE CLAIM IS:—

1. A semiconductor switch comprising: a PNPN switch having at least three PN-junctions and having a P-type anode, an N-type gate, a P-type gate and an N-type cathode; switching means having input, output, and control terminals; a passive electrical element; and driver means for driving the control terminal of said switching means; the input and output terminals of said switching means and said passive element both being connected in parallel across one of said PN-junctions at one end of said PNPN switch, with said driver means arranged to supply to the control terminal of said switching means a current derived from a current flowing through a PN-junction at the other end of said PNPN switch thereby driving said switching means.

2. A semiconductor switch as claimed in claim 1, wherein said PNPN switch includes an NPN transistor and a PNP transistor, an N-type collector of said NPN transistor being connected to an N-type base of said PNP transistor, and a P-type collector of said PNP transistor being connected to a P-type base of said NPN transistor.

3. A semiconductor switch as claimed in claim 1, wherein said switching means is an NPN transistor connected at its collector and emitter to the P-type gate and N-type

cathode of said PNPN switch, respectively, said NPN transistor being connected at its base to said driver means.

4. A semiconductor switch as claimed in claim 3, wherein said driver means comprises a PNP transistor connected at its emitter and base to the P-type anode and N-type gate of said PNPN switch, respectively, said PNP transistor being connected at its collector to the base of said NPN transistor.

5. A semiconductor switch as claimed in claim 3, wherein said driver means comprises a P-type collector disposed adjacent to the region of said N-type gate, and connected to the base of said NPN transistor.

6. A semiconductor switch as claimed in claim 3, wherein said driver means comprises a capacitive element via which the base of said NPN transistor is connected to said N-type gate of said PNPN switch.

7. A semiconductor switch according to claim 6, wherein the capacitive element is formed by a diode.

8. A semiconductor switch according to Claim 6, wherein the capacitive element is a capacitor.

9. A semiconductor switch as claimed in claim 1, wherein said semiconductor switch includes a field effect transistor having source, gate and drain terminals, the source and drain terminals of said field effect transistor being connected to said P-type anode and P-type gate of said PNPN switch whereby said gate terminal of said field effect transistor can be used for voltage control of said semiconductor switch.

10. A semiconductor switch as claimed in claim 1, wherein said semiconductor switch includes a field effect transistor having source, gate and drain terminals, said field effect transistor comprising said P-type anode and P-type gate of said PNPN switch and an insulated electrode disposed between said P-type anode and P-type gate of said PNPN switch, said insulated electrode being the gate terminal of said field effect transistor.

11. A semiconductor switch as claimed in any preceding claim, wherein said passive element is a resistor.

12. A semiconductor switch as claimed in claim 1, wherein said switching means comprises a PNP transistor connected at its emitter and collector to the P-type anode and N-type gate of said PNPN switch, respectively, said PNP transistor being connected at its base to said driver means.

13. A semiconductor switch claimed in claim 12, wherein said driver means comprises an NPN transistor connected at its emitter and base to the N-type cathode

semiconductor switch the active circuit network inserted in parallel to the PNPN switch, together with part of the positive feedback loop of the PNPN switch, makes up a negative feedback circuit; and a current substantially in phase with the current flowing in the base resistor R_2 of the transistor Q_1 through the PNP transistor Q_2 including the junction capacitance C_j is rendered to flow in the parallel-connected active circuit network, so that the base current if the transistor Q_1 is bypassed by the transistor Q_2 whose collector is connected to the base of the transistor Q_1 , thus making it possible to maintain the effective DC positive feedback loop gain of the whole device more than one.

Furthermore, in Figure 10 the PNPN switch is provided with a voltage control terminal taking advantage of a field effect transistor, which, in combination with a conventional current control system, permits the PNPN switch to be closed with a small control voltage even against floating of the cathode potential level. In addition, the parallel connection of an impedance element and a switching element for protection of the device from the dv/dt effect makes possible a PNPN switch with a large dv/dt bearing capacity which is capable of being closed with a small control current.

WHAT WE CLAIM IS:—

1. A semiconductor switch comprising: a PNPN switch having at least three PN-junctions and having a P-type anode, an N-type gate, a P-type gate and an N-type cathode; switching means having input, output, and control terminals; a passive electrical element; and driver means for driving the control terminal of said switching means; the input and output terminals of said switching means and said passive element both being connected in parallel across one of said PN-junctions at one end of said PNPN switch, with said driver means arranged to supply to the control terminal of said switching means a current derived from a current flowing through a PN-junction at the other end of said PNPN switch thereby driving said switching means.

2. A semiconductor switch as claimed in claim 1, wherein said PNPN switch includes an NPN transistor and a PNP transistor, an N-type collector of said NPN transistor being connected to an N-type base of said PNP transistor, and a P-type collector of said PNP transistor being connected to a P-type base of said NPN transistor.

3. A semiconductor switch as claimed in claim 1, wherein said switching means is an NPN transistor connected at its collector and emitter to the P-type gate and N-type

cathode of said PNPN switch, respectively, said NPN transistor being connected at its base to said driver means.

4. A semiconductor switch as claimed in claim 3, wherein said driver means comprises a PNP transistor connected at its emitter and base to the P-type anode and N-type gate of said PNPN switch, respectively, said PNP transistor being connected at its collector to the base of said NPN transistor.

5. A semiconductor switch as claimed in claim 3, wherein said driver means comprises a P-type collector disposed adjacent to the region of said N-type gate, and connected to the base of said NPN transistor.

6. A semiconductor switch as claimed in claim 3, wherein said driver means comprises a capacitive element via which the base of said NPN transistor is connected to said N-type gate of said PNPN switch.

7. A semiconductor switch according to claim 6, wherein the capacitive element is formed by a diode.

8. A semiconductor switch according to Claim 6, wherein the capacitive element is a capacitor.

9. A semiconductor switch as claimed in claim 1, wherein said semiconductor switch includes a field effect transistor having source, gate and drain terminals, the source and drain terminals of said field effect transistor being connected to said P-type anode and P-type gate of said PNPN switch whereby said gate terminal of said field effect transistor can be used for voltage control of said semiconductor switch.

10. A semiconductor switch as claimed in claim 1, wherein said semiconductor switch includes a field effect transistor having source, gate and drain terminals, said field effect transistor comprising said P-type anode and P-type gate of said PNPN switch and an insulated electrode disposed between said P-type anode and P-type gate of said PNPN switch, said insulated electrode being the gate terminal of said field effect transistor.

11. A semiconductor switch as claimed in any preceding claim, wherein said passive element is a resistor.

12. A semiconductor switch as claimed in claim 1, wherein said switching means comprises a PNP transistor connected at its emitter and collector to the P-type anode and N-type gate of said PNPN switch, respectively, said PNP transistor being connected at its base to said driver means.

13. A semiconductor switch claimed in claim 12, wherein said driver means comprises an NPN transistor connected at its emitter and base to the N-type cathode



(14)

7

1,503,939

7

and P-type gate of said PNP switch, respectively, said NPN transistor being connected at its collector to the base of said PNP transistor.

8 or 9 or Figures 10, 11. and 12 of the accompanying drawings.

10

- 5 14. A semiconductor switch constructed and arranged to operate substantially as hereinbefore described with reference to Figures 3 and 4, Figures 5 and 6, Figures 7.

J. A. KEMP & CO.,
Chartered Patent Agents,
14, South Square,
Gray's Inn,
London, WC1R 5EU.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1978
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
which copies may be obtained.



* C L M S *