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Description

Method for producing wiring arrangements having solder bumps

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The number of connections on integrated circuits is becoming ever greater, while said integrated circuits are at the same time becoming miniaturized to an ever greater extent. The difficulties expected in the course of this increase in miniaturization in the application of solder paste and component mounting are intended to be overcome by new housing forms, where emphasis may be given here in particular to single-chip, few-chip or multi-chip modules in the ball grid array package (DE-Z productronic 5, 1994, pages 54, 55). These modules are based on a plated-through substrate, on which contact is made with the chips for example via contact-making wires or by means of flip-chip mounting. The ball grid array (BGA) is situated on the underside of the substrate, and is often also referred to as a solder grid array or solder bump array. The ball grid array comprises solder bumps arranged over the area on the underside of the substrate, which allow surface mounting on the printed circuit boards or assemblies. The arrangement of the solder bumps over an area allows large numbers of connections to be realized in a coarse grid of 1.27 mm, for example.

DE-C-195 35 622 discloses a method for applying solder bumps to connection pads distributed over the area of a substrate, in which disk-shaped solder moldings are positioned by means of a multiple suction gripper in the desired configuration on the connection pads and then remelted to form spherical solder bumps.

The invention specified in claim 1 is based on the problem of providing a method for producing wiring arrangements having solder bumps which enables the



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solder bumps to be produced simply, rapidly and economically.

The invention is based on the insight that solder layers applied to the connection pads of a
5 conductor pattern

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can be remelted practically automatically to form solder bumps if conductor regions of reduced width are used to prevent the molten solder from flowing away via the adjoining conductor tracks. In this case, the
5 molten solder on the conductor regions of reduced width flows toward the connection pads and, accordingly, increases the volume of the solder bumps that are produced there. The conductor regions of reduced width which are necessary for forming the solder bumps can be
10 realized practically without any additional outlay during the creation of the conductor pattern of the wiring arrangement.

Advantageous refinements of the method according to the invention emerge from claims 2 to 15.
15 In accordance with claims 2 and 3, the conductor regions of reduced width can be formed in a particularly simple manner by a constriction of the conductor tracks or by holes introduced in the central region of the conductor tracks.

20 The geometry - specified in claim 4 - of the connection pads and of the conductor regions of reduced width enables optimum formation of the solder bumps by remelting the applied solder layer.

The development according to claim 5 enables
25 the solder bumps to be additionally enlarged, since the molten solder on the solder supply structures also flows toward the connection pads. In this case, optimum conditions are produced if the geometry of the corresponding solder supply structures which is
30 specified in claim 6 is adhered to.

In accordance with claim 7, solder layers made of a tin-lead alloy are particularly well suited to the formation of solder bumps and also with regard to the requirements made of the solder bumps.

The refinement according to claim 8 enables the solder layers to be applied particularly simply and reliably by means of electrodeposition of metal. Moreover, during the electrodeposition of the solder
5 layers, the thickness of the latter, which determines the size of the solder bumps, can easily be monitored and, if appropriate, varied as well.

The development according to claim 9 enables simple cathodic contact to be made with the conductor
10 pattern during the electrodeposition of solder layers.

The refinement according to claim 10 enables selective remelting of the solder layers without heating the entire wiring arrangement. Since the remelting of the solder layers can be performed
15 extremely rapidly, moreover, with the aid of a laser beam, the thermal loading of the wiring arrangements is minimal.

The development according to claim 11 enables a further reduction in the thermal loading of the wiring
20 arrangement since here the solder layers are melted selectively only in the regions required for forming the solder bumps. These regions comprise the connection pads, the conductor regions of reduced width and - if present - in accordance with claim 12 the solder supply
25 structures as well.

The development according to claim 13 enables the solder layers to be remelted very rapidly with particularly low thermal loading of the wiring arrangement.

30 In accordance with claim 14, Nd:YAG lasers having a wavelength of 1.06 μm have proved particularly successful for remelting solder layers in order to form solder bumps.

In principle, the laser remelting of solder
35 layers can also be performed with a diode laser array or with a strip-like laser beam. In accordance with claim 15, however,

the laser remelting with the aid of a deflectable laser beam is preferred since this results in very high flexibility and enables targeted selection of the regions to be melted. Moreover, those regions of a solder layer which are to be melted can be scanned
5 extremely rapidly with a deflectable laser beam.

Exemplary embodiments of the invention are illustrated in the drawing and are described in more detail below.

10 In the figures:

Figure 1 to Figure 6 show different method stages in the production of a wiring arrangement and the formation of solder bumps on the
15 connection pads of said wiring arrangement,

Figure 7 shows the finished wiring arrangement after a semiconductor module has been soldered on,

20 Figure 8 shows a variant with a plurality of solder supply structures leading toward the connection pads, and

25 Figure 9 shows a variant for the formation of conductor structures of reduced width by virtue of holes introduced centrally in the conductor tracks.

Figure 1 shows an electrically insulating
30 substrate S with a metallization layer M applied on one side. This metallization layer M is a thin copper coating or a layer applied by the chemical deposition of copper. The metallization layer M is then patterned with an Nd:YAG laser having a wavelength of $1.06\text{ }\mu\text{m}$,
35 this laser patterning being indicated by a laser beam LS1 in Figure 1.

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In accordance with Figure 2, connection pads P1 and conductor tracks LZ are produced in the course of the laser patterning, the connection pads P1 each

being connected to the conductor tracks LZ, which extend further, via conductor regions LB1 of reduced width. The wiring arrangement additionally has a collective line SL which is connected to the individual
5 connection pads P1 via solder supply structures LS, which are likewise of reduced width compared with the conductor tracks LZ. The collective line SL enables cathodic contact to be made with the entire conductor pattern and thus electrodeposition of metal onto the
10 conductor pattern.

In accordance with Figure 3, a reinforcing layer V made of copper and a solder layer L made of a tin-lead alloy are successively applied to the conductor pattern by electrodeposition of metal. The
15 electrical isolation of the collective line SL from the rest of the conductor pattern is initiated by a laser beam, indicated by an arrow LS2 in Figure 3. In this case, an Nd:YAG laser having a wavelength of $0.355 \mu\text{m}$ or $1.06 \mu\text{m}$ is used to remove the solder layer in those
20 regions of the solder supply structures LS which directly adjoin the collective line SL, the copper of the reinforcing layer V and of the metallization layer M which is uncovered as a result of this being removed, in accordance with Figure 4, by etching down to the
25 surface of the substrate S.

Figure 4 furthermore shows a deflectable laser beam LS3, with which the solder layer L on a connection pad P1 on the conductor region LB1 which leads away therefrom and on the solder supply structure LS which
30 leads away therefrom is in each case melted simultaneously. An Nd:YAG laser having a wavelength of $1.06 \mu\text{m}$ whose laser beam LS3 is greatly defocused is used for this purpose.

In the case of the depicted laser remelting of
35 the solder layer L, the liquid solder flows from the narrow solder supply structure LS and from the narrow conductor region LB1 toward the connection pad P1, so that a solder bump LH is automatically produced there,

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in accordance with Figure 5. The volume of the solder bump LH can, if appropriate, be further

increased by means of measures that will be explained with reference to Figures 8 and 9.

Figure 6 shows the arrangement of a bumpless semiconductor module HB on the wiring arrangement, said module's connection areas AF, comprising a layer sequence of aluminum, nickel and gold, for example, lying directly on the summits of the assigned solder bumps LH. If all the solder bumps LH assigned to the semiconductor module HB are subsequently melted simultaneously for example by reflow soldering or by laser soldering, then the result is reliable soldered connections with the concave form of the solder bumps LH which can be seen from Figure 7.

Figure 8 shows a connection pad, designated by P2 in this case, which is connected to the conductor track LZ, which extends further, via a constricted conductor region LB2. Moreover, a total of three solder supply structures LS ending blind lead to the connection pad P2, which structures correspondingly increase the solder volume of the solder bump produced on the connection pad P2.



Patent claims

1. A method for producing wiring arrangements having solder bumps (LH) for flip-chip mounting or surface mounting, having the following steps:
- 5 formation of a conductor pattern on an electrically insulating substrate (S), connection pads (P1; P2; P3) of the conductor pattern each being connected to the assigned conductor tracks (LZ), which extend further, via a conductor region (LB1; LB2; LB3) of reduced width,
- 10 application of a solder layer (L) to the conductor pattern, at least in the region of the connection pads (P1; P2; P3) and of the conductor regions (LB1; LB2; LB3) of reduced width,
- 15 remelting of the solder layer (L) to form the solder bumps (LH) on the connection pads (P1; P2; P3).
2. The method as claimed in claim 1, characterized in that the conductor regions (LB1; LB2) of reduced width are formed by a constriction of the conductor tracks (LZ).
3. The method as claimed in claim 1, characterized in that the conductor regions (LB3) of reduced width are formed by introducing a hole (LO) in the central region of the conductor tracks (LZ).
- 25 4. The method as claimed in one of the preceding claims, characterized in that connection pads (P1; P2; P3) having area dimensions of between
- 30 $100 \times 100 \mu\text{m}^2$ and $250 \times 250 \mu\text{m}^2$ are formed, and in that conductor regions (LB 1; LB2; LB3) of reduced width are formed with a width of between $10 \mu\text{m}$ and $40 \mu\text{m}$ and a length of between $100 \mu\text{m}$ and $500 \mu\text{m}$.
5. The method as claimed in one of the preceding claims, characterized in that additional solder supply structures (LS) are produced during the formation of the conductor pattern,
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at least one solder supply structure (LS), which has a reduced width compared with the width of the conductor tracks (LZ), leading away from each of the individual connection pads (P1; P2; P3).

5 6. The method as claimed in claim 5, characterized in that solder supply structures (LS) are formed with a width of between 10 μm and 40 μm and a length of between 100 μm and 500 μm .

7. The method as claimed in one of the preceding
10 claims, characterized in that a solder layer (L) composed of a tin-lead alloy is applied to the conductor pattern.

8. The method as claimed in one of the preceding claims, characterized in that the solder layer (L) is
15 applied to the conductor pattern by electrodeposition of metal.

9. The method as claimed in claim 8, characterized in that cathodic contact is made with the conductor pattern during the electrodeposition of metal via a
20 collective line (SL) connected to all of the connection pads (P1; P2; P3), and in that the collective line (SL) is separated after the deposition of metal.

10. The method as claimed in one of the preceding claims, characterized in that the solder layer (L) is
25 remelted with the aid of a laser beam (LS3).

11. The method as claimed in claim 10, characterized in that the solder layers (L) are each remelted selectively in the region of the connection pads (P1; P2; P3) and of the conductor regions
30 (LB1; LB2; LB3) of reduced width which lead away therefrom.



12. The method as claimed in claims 5 and 11, characterized in that the solder layers (L) are each remelted selectively in the region of the connection pads (P1; P2; P3), of the conductor regions (LB1; LB2; LB3) of reduced width which lead away therefrom, and of the solder supply structures (LS) which lead away therefrom.
13. The method as claimed in one of claims 10 to 12, characterized in that the solder layers (L) are remelted with the aid of a greatly defocused laser beam (LS3).
14. The method as claimed in one of claims 10 to 13, characterized in that the solder layers (L) are remelted with the laser beam (LS3) of an Nd:YAG laser having a wavelength of 1.06 μm .
15. The method as claimed in one of claims 10 to 14, characterized in that the solder layers (L) are remelted with the aid of a deflectable laser beam (LS3).



Abstract

Method for producing wiring arrangements having solder bumps

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The conductor pattern is configured in such a way that connection pads (P1) are each connected to the conductor tongues (LZ), which extend further, via a conductor region (LB1) of reduced width. A solder layer applied to the conductor pattern is preferably remelted by means of a laser beam, the solder flowing toward the connection pads (P1) and forming solder bumps there.

10

Figure 2

FIG 1

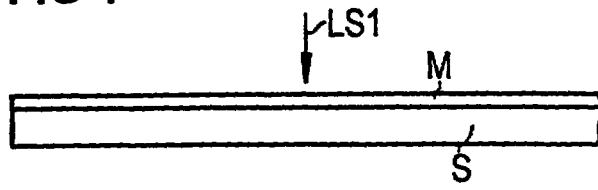


FIG 2

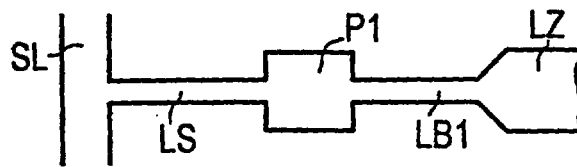


FIG 3

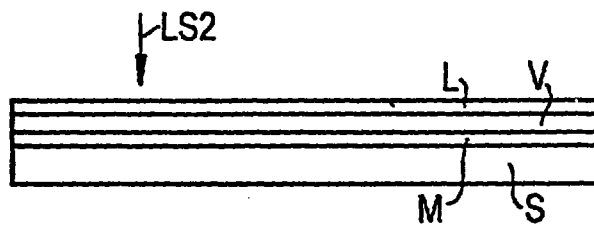


FIG 4

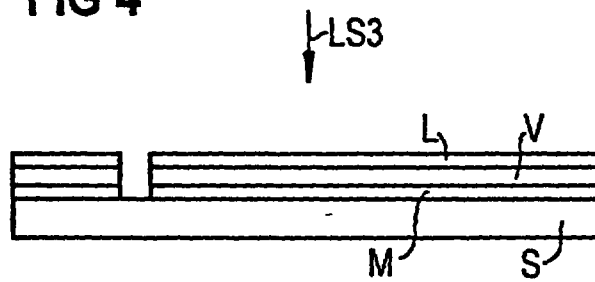


FIG 5

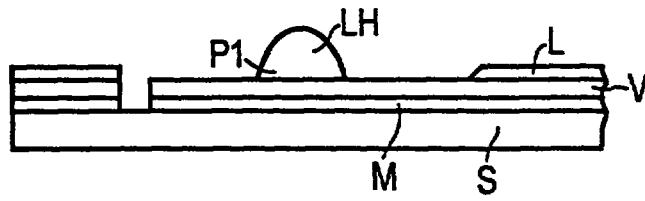


FIG 6

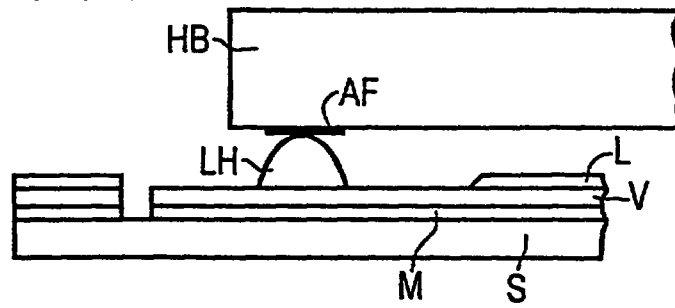


FIG 7

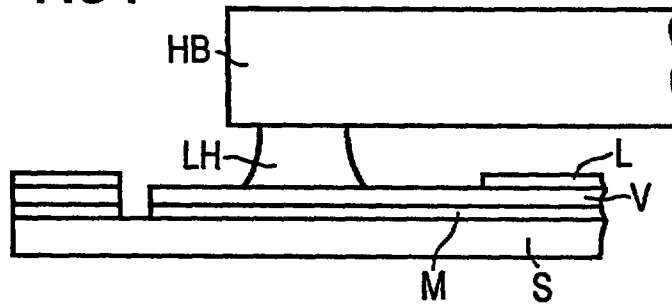


FIG 8

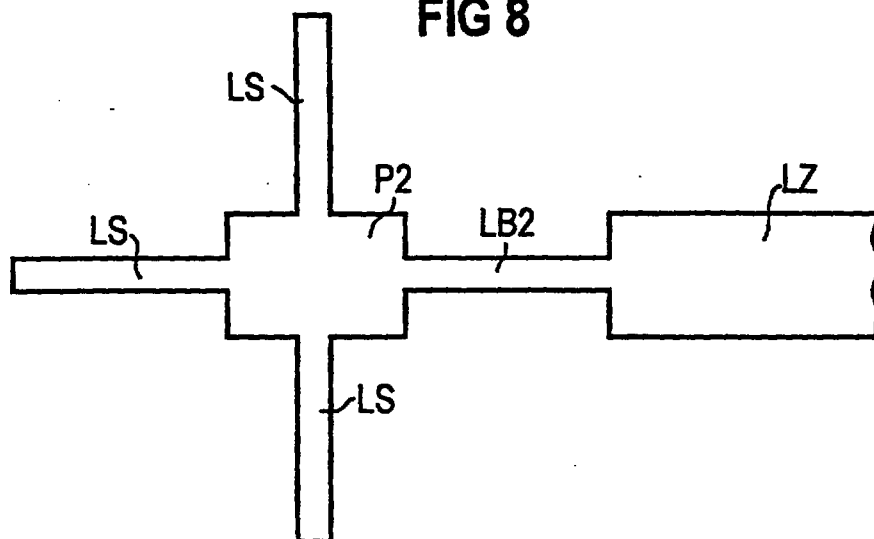
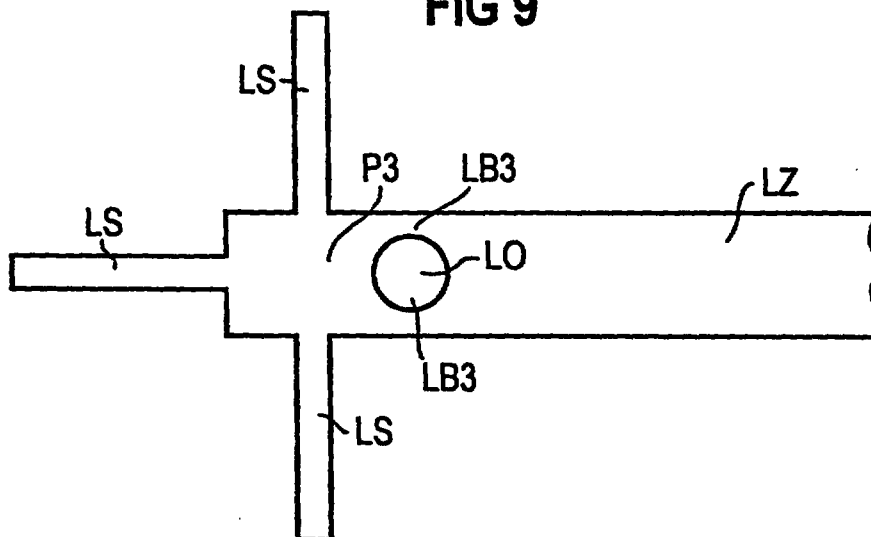


FIG 9



Description

Method for producing wiring arrangements having solder bumps

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The number of connections on integrated circuits is becoming ever greater, while said integrated circuits are at the same time becoming miniaturized to an ever greater extent. The
10 difficulties expected in the course of this increase in miniaturization in the application of solder paste and component mounting are intended to be overcome by new housing forms, where emphasis may be given here in particular to single-chip, few-chip or multi-chip
15 modules in the ball grid array package (DE-Z productronic 5, 1994, pages 54, 55). These modules are based on a plated-through substrate, on which contact is made with the chips for example via contact-making wires or by means of flip-chip mounting. The ball grid
20 array (BGA) is situated on the underside of the substrate, and is often also referred to as a solder grid array or solder bump array. The ball grid array comprises solder bumps arranged over the area on the underside of the substrate, which allow surface
25 mounting on the printed circuit boards or assemblies. The arrangement of the solder bumps over an area allows large numbers of connections to be realized in a coarse grid of 1.27 mm, for example.

DE-C-195 35 622 discloses a method for applying
30 solder bumps to connection pads distributed over the area of a substrate, in which disk-shaped solder moldings are positioned by means of a multiple suction gripper in the desired configuration on the connection pads and then remelted to form spherical solder bumps.

WO 93/02831 A discloses a method for producing wiring arrangements having solder bumps, which method has the following steps:

- 5 - formation of a conductor pattern on an electrically insulating substrate, connection pads of the conductor pattern each being connected to the assigned conductor tracks, which extend further,
- 10 - application of a solder layer to the connection pads and the conductor tracks,
- remelting of the solder layer in a bath to form the solder bumps on the connection pads.

15 In one configuration of the method, the connection pads are provided in the crossover region of two, three or four conductor tracks. In another configuration of the method, the connection pads have a greater width than the conductor tracks which extend further.

20 The invention specified in claim 1 is based on the problem of providing a method for producing wiring arrangements having solder bumps which enables the solder bumps to be produced simply, rapidly and economically.

25 The invention is based on the insight that solder layers applied to the connection pads of a conductor pattern



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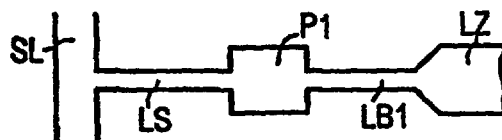
1. A method for producing wiring arrangements having solder bumps (LH) for flip-chip mounting or surface mounting, having the following steps:
- 5 - formation of a conductor pattern on an electrically insulating substrate (S), connection pads (P1; P2; P3) of the conductor pattern each being connected to the assigned conductor tracks (LZ), which extend further, via conductor regions (LB1; LB2; LB3) of reduced width compared with the
10 width of the conductor tracks (LZ),
 - application of a solder layer (L) to the conductor pattern, at least in the region of the connection pads (P1; P2, P3) and of the conductor regions (LB1; LB2; LB3) of reduced width,
 - 15 - remelting of the solder layer (L) to form the solder bumps (LH) on the connection pads (P1; P2; P3).

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<p>(21) International application number: PCT/EP99/03802</p> <p>(22) International filing date: 1 June 1999 (01.06.99)</p> <p>(30) Data relating to the priority: 198 24 633.1 2 June 1998 (02.06.98) DE</p> <p>(71) Applicant (for all designated States except US): SIEMENS S. A. [BE/BE]; Chaussee de Charleroi 116, B-1060 Brussels (BE).</p> <p>(72) Inventors; and</p> <p>(75) Inventors/Applicants (US only): ASCHENBRENNER, Rolf [DE/DE]; Unter den Eichen 57 c, D-12203 Berlin (DE). KLÖSER, Joachim [DE/DE]; Wartburgstrasse 53 a, D-10823 Berlin (DE). JUNG, Erik [DE/DE]; Flatowallee 16/836, D-14055 Berlin (DE). BOONE, Luc [BE/BE]; Karel de Stoutelaan 6, B-8020 Oostkamp (BE). DE STEUR, Hubert [BE/BE]; Treinstraat 1, B-9031 Drongen (BE). HEERMAN, Marcel [BE/BE]; Azaleastrasse 6, B-9200 Merelbeke (BE). VAN PUYMBROECK, Jozef [BE/BE]; Korenbloemstraat 17, B-8020 Oostkamp (BE).</p> <p>(74) Attorney: EPPING, Wilhelm; Siemens S.A., Postfach 22 13 17, D-80503 Munich (DE).</p>		<p>(81) Designated states: CN, JP, KR, SG, US, European Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</p> <p>Published With the International Search Report.</p>

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(57) Abstract

According to the invention, the conductor pattern is configured such that the connection pads (P1) are respectively connected via a conductor region with a reduced width (LB1) to the conductor tabs (LZ) which extend the conductor. A solder layer deposited on the conductor pattern is preferably remelted by a laser beam, whereby the solder flows up to the connection pads (P1) and forms solder bumps there.

(57) Zusammenfassung

Das Leitermuster wird so ausgestaltet, daß Anschluß-Pads (P1) jeweils über einen in der Breite reduzierten Leiterbereich (LB1) mit den weiterführenden Leiterzungen (LZ) verbunden sind. Eine auf das Leitermuster aufgebrachte Lötsschicht wird vorzugsweise mittels eines Laserstrahls umgeschmolzen, wobei das Lot zu den Anschluß-Pads (P1) hin fließt und sich dort Löthöcker bilden.