

ABSTRACT

A three-dimensional semiconductor memory device includes a peripheral logic structure on a semiconductor substrate. A horizontal semiconductor layer is on the peripheral logic structure and includes a cell array region and a connection region. Electrode structures extend in a first direction on the horizontal semiconductor layer and are spaced apart in a second direction intersecting the first direction. A pair of the electrode structures adjacent to each other are symmetrically disposed to define a contact region partially exposing the horizontal semiconductor layer. A through via structure is on the contact region and connects the electrode structures to the peripheral logic structure. Each of the electrode structures includes a plurality of gate insulation regions extending along the first direction on the connection region. The gate insulation regions have different lengths from each other in the first direction.

FIG. 3A