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LUMINANCE PROCESSING SYSTEM

Abstract

A circuit for compressing and expanding video data comprises a FIFO line memory and an interpolator. A timing circuit generates control signals for writing data into the line memory and for reading data from the line memory to compress and expand the data. The interpolator smooths the data compressed or expanded in the FIFO line memory. A switching network selectively establishes a first signal path in which the line memory precedes the interpolator for implementing the data expansion and a second signal path in which the interpolator precedes the line memory for implementing the data compression. The switching network is controlled according to selected display formats requiring compression or expansion, for example by a microprocessor.

Fig. 1

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