DUAL CAPACITOR STRUCTURE FOR IMAGERS AND METHOD OF FORMATION

FIELD OF THE INVENTION

[0001] The invention relates to capacitor structures for solid state imaging devices, including CMOS and CCD imaging devices.

BACKGROUND OF THE INVENTION

[0002] There are a number of different types of semiconductor-based imagers, including charge coupled devices (CCDs), photo diode arrays, charge injection devices and hybrid focal plane arrays. CCDs are often employed for image acquisition for small size imaging applications. However, CCD imagers suffer from a number of disadvantages. For example, they are susceptible to radiation damage, they exhibit destructive read out over time, they require good light shielding to avoid image smear and they have a high power dissipation for large arrays.

[0003] Because of the inherent limitations in CCD technology, there is an interest in CMOS imagers for possible use as low cost imaging devices. CMOS imagers have a number of advantages, including for example low voltage operation and low power consumption. CMOS imagers are also compatible with integrated on-chip electronics (control logic and timing, image processing, and signal conditioning such as A/D conversion); CMOS imagers allow random access to the image data, and have lower fabrication costs as compared with the conventional CCD since standard CMOS processing techniques can be used. A fully compatible CMOS sensor technology enabling a higher level of integration of an image array with associated processing circuits would be beneficial to many digital applications.

[0004] A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photo diode, a photogate or a photoconductor overlying a doped region of a substrate for accumulating photo-generated charge in the underlying portion of the substrate.

[0005] In a conventional CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to a floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge. The charge at the floating diffusion node is typically converted to a pixel output voltage by a source follower output transistor. The photosensitive element of a CMOS imager pixel is typically either a depleted p-n junction photodiode or a field induced depletion region beneath a photogate. For photodiodes, image lag can be eliminated by completely depleting the photodiode upon readout.

[0006] In CCD, CMOS and other types of imagers, capacitors are employed in conjunction with other device components for charge storage and/or in analog signal processing circuits. As a result of the inability of the capacitors to fully collect and store the electric charge collected by the photosensitive area, conventional imagers typically suffer from poor signal to noise ratios and poor dynamic range. Additionally, conventional imagers may also suffer from poor operation due to other factors that can affect capacitor function. For example, as P-channel devices in the peripheral area have different requirements from N-channel devices in the active area of a pixel cell, an active area capacitor may require a different capacitance (for example, a higher capacitance) than the capacitance of a capacitor formed on the peripheral area. Current technological processes fail to provide, however, an optimized process for the formation of active

and peripheral area capacitors having different structural characteristics, which in turn entail different performance characteristics of the capacitors.

[0007] Accordingly, there are needed improved imagers and imaging devices, which provide for improved in-pixel capacitors and peripheral analog capacitors. Optimized methods of fabricating a pixel array exhibiting these improvements in capacitor function are also needed.

SUMMARY OF THE INVENTION

[0008] The present invention provides imaging devices comprising in-pixel and peripheral capacitors. The capacitors used in peripheral circuits have different requirements from the in-pixel or active capacitors. In one embodiment, dual stack capacitors comprising two dielectric layers may be provided in both the active pixel area and the peripheral area to achieve low leakage and high capacitance. In another embodiment, a dual dielectric capacitor may be provided in one of the active or the peripheral areas, and a single dielectric capacitor is provided in the other of the active or peripheral areas. In yet another embodiment, a single dielectric capacitor is provided in both the active and the peripheral areas, but the dielectric of the active area is different from the dielectric of the peripheral area. The invention also provides methods of forming such capacitor structures.

[0009] These and other features and advantages of the invention will be more apparent from the following detailed description that is provided in connection with the accompanying drawings and illustrated exemplary embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 is a top view of portions of a CMOS imager integrated circuit according to a first exemplary embodiment of the invention.

[0011] Fig. 2 is a schematic cross-sectional view of the structure of Fig. 1 taken along line A-A and at an initial stage of processing.

[0012] Fig. 3 is a schematic cross-sectional view of the structure of Fig. 1 at a stage of processing subsequent to that shown in Fig. 2.

[0013] Fig. 4 is a schematic cross-sectional view of the structure of Fig. 1 at a stage of processing subsequent to that shown in Fig. 3.

[0014] Fig. 5 is a schematic cross-sectional view of the structure of Fig. 1 at a stage of processing subsequent to that shown in Fig. 4.

[0015] Fig. 6 is a schematic cross-sectional view of a CMOS imager integrated circuit according to a second exemplary embodiment of the invention.

[0016] Fig. 7 is a schematic cross-sectional view of the structure of Fig. 6 at a stage of processing subsequent to that shown in Fig. 6.

[0017] Fig. 8 is a schematic cross-sectional view of the structure of Fig. 6 at a stage of processing subsequent to that shown in Fig. 7.

[0018] Fig. 9 is a schematic cross-sectional view of the structure of Fig. 6 at a stage of processing subsequent to that shown in Fig. 8.

[0019] Fig. 10 a schematic cross-sectional view of a CMOS imager integrated circuit according to a third exemplary embodiment of the invention.

[0020] Fig. 11 is a schematic cross-sectional view of the structure of Fig. 10 at a stage of processing subsequent to that shown in Fig. 10.

[0021] Fig. 12(a) is a schematic cross-sectional view of the structure of Fig. 10 at a stage of processing subsequent to that shown in Fig. 11.

[0022] Fig. 12(b) is a schematic cross-sectional view of the structure of Fig. 10 at a stage of processing subsequent to that shown in Fig. 12(a).

[0023] Fig. 13 is a schematic cross-sectional view of the structure of Fig. 10 at a stage of processing subsequent to that shown in Fig. 12(b).

[0024] Fig. 14 is a schematic cross-sectional view of the structure of Fig. 10 at a stage of processing subsequent to that shown in Fig. 13.

[0025] Fig. 15 illustrates a block diagram of a CMOS imager device having a pixel array, wherein the imager device may be combined with a processor in a single integrated circuit fabricated according to the present invention.

[0026] Fig. 16 illustrates a schematic diagram of a computer processor system which may utilize an imaging device, for example, a CMOS imaging device constructed in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0027] In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural and logical

changes may be made without departing from the spirit or scope of the present invention.

[0028] The terms "substrate" and "wafer" can be used interchangeably in the following description and may include any semiconductor-based structure. The structure should be understood to include silicon, silicon-on insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide. When reference is made to the substrate in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0029] The term "pixel" refers to a discrete picture element unit cell containing a photoconductor and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative pixel according to one embodiment of the invention is illustrated in the figures and description herein. An array or combination of pixels together may comprise a photoconductor array for use in a CMOS or CCD imager device. Typically, fabrication of all pixels of a photoconductor array will proceed simultaneously in a similar fashion.

[0030] Referring now to the drawings, where like elements are designated by like reference numerals, Figs. 1-16 illustrate methods for improving the performance of capacitors in CMOS and CCD imaging devices conducted in accordance with embodiments of the present invention. The break symbol (\\) in Figs. 2-14 represents a spatial separation between pixel array region 58 with N-channel transistors and P-channel devices in the peripheral region 59.

[0031] Figs. 1-5 illustrate a first embodiment of the present invention, according to which capacitors 84, 93 (Figs. 1, 5) are formed in active area and peripheral area, respectively, of semiconductor substrate 70. Portions of pixel region 58 and peripheral region 59 are formed in semiconductor substrate 70 at a surface of which a CMOS imager integrated circuit may be fabricated. The CMOS fabrication process begins with a lightly-doped P-type or N-type silicon substrate, for example, or lightly-doped epitaxial silicon on a heavily doped substrate. Pixel region 58 of substrate 70 includes components of a pixel cell circuitry within an array of pixels, while peripheral portion 59 includes representative components formed at the periphery of the array, and employed for timing and control or readout of signals from pixel cells. Source/drain regions (not shown) may be implanted into substrate 70 using any suitable method, including ion implantation, to form lightly doped or heavily doped source/drain regions.

[0032] Fig. 1 also illustrates transistors 76, 94 and capacitors 84, 93 which are formed in the active pixel region 58 and in the peripheral region 59. Transistors 76, 94 and capacitors 84, 93 each comprise a layer of insulating material 88. Insulating material 88 may be a layer of tetraethyl orthosilicate (TEOS) formed by conventional deposition processes, for example thermal oxidation or chemical vapor deposition (CVD). Insulating material 88 may be optionally formed as a nitride, oxide, ON (oxide-nitride), NO (nitride-oxide), ONO (oxide-nitride-oxide), or other insulating material.

[0033] Fig. 1 also illustrates a photosensor 90 in the pixel region 58. Photosensor 90 may be formed as a photodiode for accumulating photo-generated charge in an underlying portion of the substrate, as depicted in Figs 1-9. Photosensor 90 may include, for example, a photosensitive p-n-p junction region formed at or beneath the upper surface of substrate 70

by conventional techniques. It should be understood that the imagers of the invention may include a photogate, photoconductor, or other image to charge converting device, in lieu of a photodiode, as the initial accumulator for photo-generated charge. Photosensor 90 may be formed at or beneath the upper surface of substrate 70, and may also be constructed in any arrangement, orientation, shape and geometry, to be integrated with other components of a semiconductor device.

[0034] Although not depicted in Fig. 1, pixel region 58 may comprise other N-channel devices (not shown), and peripheral region 59 may comprise other P-channel devices (not shown). For example, pixel region 58 may include N-channel transistors controlled by a transfer gate and reset gate (not shown), each formed by depositing and patterning a polysilicon stack. The polysilicon stack can be formed, for example, by depositing and patterning a layer of gate oxide, a layer of doped polysilicon, and a layer of oxide or nitride.

[0035] Reference is now made to Fig. 2, which illustrates a cross-sectional view of the CMOS image sensor of Fig. 1, taken along line A-A and after initial processing, but prior to formation of transistors 76, 94 and capacitors 84, 93 in the pixel region 58 and in the periphery region 59. For exemplary purposes, the substrate 70 may be a silicon substrate and may include a surface oxide layer, treated herein as part of one substrate. However, as noted above, the invention has equal application to other semiconductor substrates.

[0036] Fig. 2 also illustrates trench isolation regions 128 formed in the substrate 70 by a conventional process. For example, the trench isolation regions 128 may be formed by an STI process, according to which trenches are first tched in the doped active layer or substrate 70 via a directional etching process, such as Reactive Ion Etching (RIE), or with

a preferential anisotropic etchant used to etch into the substrate 70 to a sufficient depth, generally about 1000 Å to 5000 Å. The trenches are then filled with an insulating material, for example, silicon dioxide, silicon nitride, ON (oxide-nitride), NO (nitride-oxide), or ONO (oxide–nitride-oxide). The insulating materials may be formed by various chemical vapor deposition (CVD) techniques such as low pressure chemical vapor deposition (LPCVD), high density plasma (HDP) deposition, or any other suitable method for depositing an insulating material within a trench. While the trench isolation regions 128 may be formed by an STI process, it should be understood that the isolation regions 128 may instead be formed using a Local Oxidation of Silicon (LOCOS) process.

[0037] Also illustrated in Fig. 2 is floating diffusion region 125 formed in the substrate 70 and acting as a sensing node. A transfer gate (not shown) transfers photoelectric charges generated in photosensor 90 to floating diffusion region 125. Trench isolation regions 128 and diffusion regions 125 may also be doped after various fabrication steps via a masked ion implantation.

[0038] Referring still to Fig. 2, a gate oxide layer 81 is formed over the surface of substrate 70. A first electrode layer 210 is subsequently formed over gate oxide layer 81 and trench isolation regions 128. Electrode layer 210 may be formed of any suitable electrode material, including but not limited to poly, poly/WSi, poly/WN/W, and poly/silicide. Electrode layer 210 may optionally be planarized after formation, using any suitable planarizing technique.

[0039] Dielectric layers 214 and 218 are then consecutively formed over electrode layer 210, as also shown in Fig. 2. Dielectric layers 214 and 218 each may be formed of an oxide, metal oxide, HfO_x, nitride, Al_2O_3, Ta_2O_5, or BST material, or any other nonconductor of direct electric

current. Electrode layer 220 is then formed over dielectric layer 218. Electrode layer 220 may be formed of any suitable electrode material, including but not limited to polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$ and poly/$MoSi_2$. Electrode layers 210 and 220 each may be formed to any suitable thickness, for example from about 50 Angstroms to about 1,000 Angstroms. Layers 210, 214, 218 and 220 each may be deposited by any suitable technique, including chemical vapor deposition (CVD) techniques such as low pressure chemical vapor deposition (LPCVD) or high density plasma (HDP) deposition. Dielectrics used in the invention may each be formed to any suitable thickness, for example from about 10 Angstroms to about 500 Angstroms, and with any desired shape and geometry.

[0040] Fig. 3 illustrates a stage of processing subsequent to that shown in Fig. 2 and, in particular, the patterning of the electrode layer 220. Although electrode layer 220 is shown in Fig. 3 patterned with generally straight sidewalls above layers 210, 214, 218 and trench isolation regions 128, electrode layer 220 may optionally be patterned with any other suitable shape and geometry.

[0041] Referring now to Fig. 4, insulating layer 88 is formed to cover patterned electrodes 220 as well as dielectric layer 218. Insulating layer 88 may be a layer of tetraethyl orthosilicate (TEOS) formed by conventional deposition processes, for example thermal oxidation or chemical vapor deposition (CVD). Insulating layer 88 may optionally be formed as a nitride, oxide, ON (oxide-nitride), NO (nitride-oxide), ONO (oxide-nitride-oxide), or other insulating material. Insulating layer 88 may also be formed with any desired thickness, and may be optionally planarized after formation.

[0042] Subsequent to the formation of the insulating layer 88 of Fig. 4, pixel transistor 76, pixel capacitor 84, periphery transistor 94, and periphery capacitor 93 are formed by patterning and etching portions of layers 210, 214, 218 and insulating layer 88, as shown in Fig. 5. The order of the process steps for transistor and capacitor formation may be varied as is required or convenient for a particular process flow. For example, the gate stacks may be formed before, or after, or in between the steps for forming the capacitors. The dual stack capacitors 84, 93 consisting of dielectrics 214, 218 shown in Fig. 5 provide low leakage and high capacitance.

[0043] An elevated-temperature drive step may also be conducted, after which the N and P-channel devices shown in Fig. 5 are fully formed. Additionally, the structures shown in Fig. 5 may be covered with a number of translucent or transparent insulating and passivation layers (not shown) formed over the image device. Such insulating and passivation layers may include SiO_2, TEOS, BPSG, nitride, PSG, BSG, or SOG which can be planarized. Conventional processing steps may also be carried out to form, for example, contacts in the insulating layers to provide electrical connection with implanted source/drain regions and other wiring to connect gate lines and other connections in the pixel. Other conventional processing steps may also be carried out to complete the formation of additional components, for example, filters and lenses. The order of the process steps may be varied as is required or convenient for a particular process flow.

[0044] Figs. 6-9 illustrate a second exemplary embodiment for the formation of in-pixel capacitor 184 (Fig. 9) and peripheral capacitor 193 (Fig. 9) in accordance with the present invention. Fig. 6 depicts an IC device after initial processing, but prior to formation of transistors 176, 194 and capacitors 184, 193 in the pixel region 58 and in the periphery

region 59 of Fig. 9. The structure of Fig. 6 is similar in part to that of Fig. 2, to the extent that both structures comprise the first electrode layer 210 and the two dielectric layers 214, 218; the structure of Fig. 6 differs, however, from the structure of Fig. 2 in that a photoresist layer 230 (Fig. 6) is formed in lieu of the electrode layer 220 (Fig. 2).

[0045] The photoresist layer 230 is formed over and in contact with the dielectric layer 218 to allow patterning of the dielectric layer 218 in the peripheral region 59, as illustrated in Fig. 6. After selective etching and removal of the exposed portion of dielectric layer 218 in the periphery 59, and stripping of photoresist layer 230, the resulting structure is shown in Fig. 7. In this manner, the pixel region 58 of Fig. 7 comprises two dielectric layers 214, 218 whereas only the single dielectric layer 214 remains in the periphery region 59. As in the previous embodiment, electrode layer 210 may be formed of any suitable electrode material, including but not limited to poly, poly/WSi, poly/WN/W, and poly/silicide. Dielectric layers 214 and 218 each may be formed of an oxide, metal oxide, HfO_x, nitride, Al_2O_3, Ta_2O_5, or BST material, or any other nonconductor of direct electric current. Layers 210, 214, 218 may be deposited by any suitable technique, including chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD) or high density plasma (HDP) deposition.

[0046] Fig. 8 illustrates a stage of processing subsequent to that shown in Fig. 7. Subsequent to the patterning of the dielectric layer 218, electrode layer 220 of Fig. 8 is deposited and patterned over dielectric layer 218 in the pixel region 58 and over dielectric layer 214 in the periphery 59. As in the previously-described embodiment, electrode layer 220 may be formed of any suitable electrode material, including but not limited to polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$ and poly/$MoSi_2$. Layers 210, 214, 218 and 220 may be

deposited by any suitable technique, including chemical vapor deposition (CVD) techniques such as low pressure chemical vapor deposition (LPCVD) or high density plasma (HDP) deposition. Electrode layer 220 is shown patterned with generally straight sidewalls above layers 214 and 218; however, electrode layer 220 may be patterned with any other suitable shape and geometry.

[0047] Fig. 9 illustrates a stage of processing subsequent to that shown in Fig. 8. Insulating layer 88, for example, a layer of tetraethyl orthosilicate (TEOS), is formed to cover patterned electrodes 220 as well as dielectric layers 214, 218. After selective etching and patterning of layers 210, 214, 218 and insulating layer 88, the resulting pixel transistor 176, pixel capacitor 184, periphery transistor 194, and periphery capacitor 193 are formed, as shown in Fig. 9. The periphery capacitor 193 comprises a single dielectric 214, whereas the in-pixel capacitor 184 comprises two dielectrics 214, 218. Alternatively, the periphery capacitor may be formed comprising two or more dielectrics and the pixel capacitor comprising a single dielectric.

[0048] An elevated-temperature drive step may also be performed, after which the N and P-channel devices shown in Fig. 9 are fully formed. The structures shown in Fig. 9 may also be covered with a number of translucent or transparent insulating and passivation layers (not shown) formed over the image device. Such insulating and passivation layers may include SiO_2, TEOS, BPSG, nitride, PSG, BSG, or SOG which can be planarized. Conventional processing steps may also be carried out to form, for example, contacts in the insulating layers to provide electrical connection with implanted source/drain regions and other wiring to connect gate lines and other connections in the pixel.

[0049] Figs. 10-14 illustrate yet a third exemplary embodiment of the invention for the construction of in-pixel capacitor 284 (Fig. 14) and peripheral capacitor 293 (Fig. 14) in the pixel region 58 and in the periphery 59. Fig. 10 depicts an IC device after initial processing, but prior to formation of transistors 276, 294 and capacitors 284, 293 of Fig. 14. The structure of Fig. 10 is similar in part to that of Fig. 6, to the extent that both structures comprise first electrode layer 210 and the first dielectric layer 214 formed over and in contact with the first electrode layer 210; the structure of Fig. 10 differs, however, from the structure of Fig. 6 in that only one dielectric layer is employed in Fig. 10 and, thus, the photoresist layer 230 (Fig. 10) is formed directly over, and in contact with, the first dielectric layer 214.

[0050] As in the previously described embodiments, trench isolation regions 128 and floating diffusion region 125 are formed in the substrate 70, as shown in Fig. 10. Gate oxide layer 81 is formed over the surface of substrate 70 and a first electrode layer 210 is then formed over gate oxide layer 81 and trench isolation regions 128. Electrode layer 210 may be formed of any suitable electrode material, including but not limited to poly, poly/WSi, poly/WN/W, and poly/silicide. Dielectric layer 214 is subsequently formed over electrode layer 210 by any suitable technique, including CVD, LPCVD or HDP deposition. Dielectric layer 214 may be formed of an oxide, metal oxide, HfO_x, nitride, Al_2O_3, Ta_2O_5, or BST material, or any other nonconductor of direct electric current. A layer of photoresist 230 is then deposited for patterning of the dielectric layer 214 in the peripheral region 59, as also shown in Fig. 10. After selective etching and removal of the exposed portion of dielectric layer 214 in the periphery 59, the resulting structure is shown in Fig. 11. The resist layer 230 has been stripped using an oxygen–containing plasma.

[0051] As shown in Fig. 12(a), a second dielectric layer 215 is deposited on both the periphery and array. Dielectric layer 215 may be formed of an oxide, nitride, metal oxide, Al_2O_3, Ta_2O_3, BST, HfO_x, or any other insulator. This dielectric layer may be deposited by any suitable technique such as CVD, LDCVD, or HDP but not limited to these deposition methods. Dielectric 215 is different from dielectric 214. Also shown in Fig. 12(a) is another photoresist layer 330 which covers at least one periphery capacitor region.

[0052] Alternatively, the process steps may be modified such that a dielectric is first applied in the periphery 59, with appropriate masking steps, followed by deposition of a different dielectric in pixel region 58.

[0053] Reference is now made to Fig. 12(b). In Fig. 12(b), the dielectric layer 215 has been removed from the pixel region using a selective etch which may be a wet or a dry etch. The dielectric 215 in the periphery region is protected by the photoresist layer 330 and is not removed. After the selective etch, the photoresist layer 330 is removed using an oxygen containing plasma.

[0054] Reference is now made to Fig. 13. Electrode layer 220 is deposited and patterned over dielectric layer 214 in the pixel region 58 and over dielectric layer 215 in the periphery 59. Electrode layer 220 may be formed of any suitable electrode material, including but not limited to polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$ and poly/$MoSi_2$. As in the previously described embodiments, insulating layer 88 is subsequently formed to cover patterned electrodes 220 as well as dielectric layers 214 and 215, as illustrated in Fig. 14.

[0055] After selective etching and patterning of layers 210, 214, 215 and of insulating layer 88, the resulting pixel transistor 276, pixel capacitor 284, periphery transistor 294, and periphery capacitor 293 are

formed, as shown in Fig. 14. The periphery capacitor 293 comprises a single dielectric 215, whereas the pixel capacitor 284 comprises a single dielectric 214, which is different from the dielectric 215. Alternatively, the periphery capacitor 293 may be formed of two or more dielectrics and the pixel capacitor 284 may be formed of two or more different dielectrics.

[0056] An elevated-temperature drive step may also be performed, after which the N and P-channel devices shown in Fig. 14 are fully formed. The structures shown in Fig. 14 may also be covered with a number of translucent or transparent insulating and passivation layers (not shown) formed over the image device. Conventional processing steps may also be carried out to form, for example, contacts in the insulating layers to provide electrical connection with implanted source/drain regions and other wiring to connect gate lines and other connections in the pixel.

[0057] Fig. 15 illustrates a block diagram of a CMOS imager device 808 having a pixel array 800 containing a plurality of pixels arranged in rows and columns. The pixels of each row in array 800 are all turned on at the same time by a row select line, and the pixels of each column are selectively output by respective column select lines. The row lines are selectively activated by a row driver 810 in response to row address decoder 820. The column select lines are selectively activated by a column selector 860 in response to column address decoder 870. The pixel array is operated by the timing and control circuit 850, which controls address decoders 820, 870 for selecting the appropriate row and column lines for pixel signal readout. The pixel column signals, which typically include a pixel reset signal (V_{rst}) and a pixel image signal (V_{sig}), are read by a sample and hold circuit 881 associated with the column selector 860. A differential signal ($V_{rst} - V_{sig}$) is produced by differential amplifier 862 for each pixel which is amplified and digitized by analog to digital converter 875 (ADC). The analog to digital converter 875 supplies the digitized

pixel signals to an image processor 880 which forms a digital image. Image processor 880 may include circuits for signal amplification, row addressing, column addressing, white balance, color correction, image correction, and defect correction.

[0058] If desired, the imaging device 808 described above with respect to Fig. 15 may be combined with a processor in a single integrated circuit. Fig. 16 illustrates an exemplary processing system 900 which may utilize an imaging device, for example, a CMOS imager 808 incorporating an imaging device constructed in accordance with embodiments of the invention illustrated in Figs. 2-14. Any one of the electronic components shown in Fig. 16, including CPU 901, may be fabricated as an integrated circuit for use in processing images formed in accordance with the imager and methods of the present invention.

[0059] As illustrated in Fig. 16, the processing system 900 includes one or more processors 901 coupled to a local bus 904. A memory controller 902 and a primary bus bridge 903 are also coupled the local bus 904. The processing system 900 may include multiple memory controllers 902 and/or multiple primary bus bridges 903. The memory controller 902 and the primary bus bridge 903 may be integrated as a single device 906.

[0060] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908 which include at least one memory device 100. The memory components 908 may be a memory card or a memory module. Examples of memory modules include single inline memory modules (SIMMs) and dual inline memory modules (DIMMs). The memory components 908 may include one or more additional devices 909. For example, in a SIMM or DIMM, the additional device 909 might be a configuration memory, such as a

serial presence detect (SPD) memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively, other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 includes peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller 902 may implement a cache coherency protocol. If the memory controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0061] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, an miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and an legacy device interface 920. The primary bus bridge 903 may also be coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0062] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be an local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an

universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers 919. The legacy device interface 920 is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system 900.

[0063] The processing system 900 illustrated in Fig. 16 is only an exemplary processing system with which the invention may be used. While Fig. 16 illustrates a processing architecture especially suitable for a general purpose computer, such as a workstation, it should be recognized that well known modifications can be made to configure the processing system 900 to become more suitable for use in a variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU 901 coupled to memory components 908 and/or memory devices 100. These electronic devices may include, but are not limited to audio/video processors and recorders, and digital cameras and/or recorders. The CMOS imager devices of the present invention, when coupled to a pixel processor, for example, may be implemented in digital cameras and video processors and recorders. Modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0064] While the invention is preferably directed to methods for forming imager devices with distinct pixel capacitors and periphery capacitors, and structures incorporating such pixel capacitors and periphery capacitors, one skilled in the art will recognize that the invention can be used to form any type of imager device for integration with one or more processing components in a semiconductor device. For example, although the invention is described above for use in a CMOS image

sensor, the invention is not limited to such and may be used in any suitable image sensor, for example, CCD image sensors.

[0065] The last (output) stage of a CCD image sensor provides sequential pixel signals as output signals, and uses a floating diffusion node, source follower transistor, and reset gate in a similar manner to the way these elements are used in the pixel of a CMOS imager. Accordingly, the pixels formed using the capacitors of the present invention may be employed in CCD image sensors as well as CMOS image sensors. The imager devices of the present invention may also be formed as different size megapixel imagers, for example imagers having arrays in the range of about 0.1 megapixels to about 20 megapixels.

[0066] It should again be noted that although the invention has been described with specific reference to imaging devices comprising distinct pixel capacitors and periphery capacitors, the invention has broader applicability and may be used in any imaging apparatus. Similarly, the processes described above are but a few of many that may be used. The above description and drawings illustrate preferred embodiments which achieve the objects, features and advantages of the present invention. Although certain advantages and preferred embodiments have been described above, those skilled in the art will recognize that substitutions, additions, deletions, modifications and/or other changes may be made without departing from the spirit or scope of the invention. Accordingly, the invention is not limited by the foregoing description but is only limited by the scope of the appended claims.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a CMOS imaging device having different in-pixel capacitors and periphery capacitors, comprising the steps of:

forming at least one photosensor;

forming a first electrode layer over said substrate in a pixel region and a periphery region;

forming a first dielectric layer over said first electrode layer;

forming a second dielectric layer over said first dielectric layer; and

forming a second electrode layer over said second dielectric layer.

2. The method of claim 1, wherein said first electrode layer is formed of a material selected from the group consisting of a poly, poly/WSi, poly/WN/W, poly/silicide, poly/metal and metal.

3. The method of claim 1, wherein said first dielectric layer and said second dielectric layer are formed of a material independently selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, BST, metal oxide and HfO_x.

4. The method of claim 1, wherein said second electrode layer is formed of a material selected from the group consisting of a polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$, poly/$MoSi_2$, poly/metal and metal.

5. The method of claim 1, wherein said photosensor is one of a photodiode, photogate or photoconductor.

6. The method of claim 5, wherein said photodiode is a p-n-p photodiode.

7. A method of forming an imaging device having both single dielectric capacitors and dual dielectric capacitors, the method comprising the steps of:

forming at least one photosensor;

forming a first electrode layer over said substrate in a pixel region and a periphery region;

forming a first dielectric layer over said first electrode layer;

forming a second dielectric layer over said first dielectric layer;

removing said second dielectric layer in one of said pixel region and said periphery region; and

patterning a second electrode layer in said pixel region and said periphery region, such that one of said pixel region and said periphery region comprises said first dielectric layer, and the other of said pixel region and said periphery region comprises both said first dielectric layer and said second dielectric layer.

8. The method of claim 7, wherein said first dielectric layer is different from said second dielectric layer.

9. The method of claim 7, wherein said first electrode layer is formed of a material selected from the group consisting of a poly, poly/WSi, poly/WN/W, poly/silicide, poly/metal and metal.

10. The method of claim 7, wherein said first dielectric layer and said second dielectric layer are formed of a material independently selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, BST, metal oxide and HfO_x.

11. The method of claim 7, wherein said second electrode layer is formed of a material selected from the group consisting of a polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$, poly/$MoSi_2$, poly/metal and metal.

12. The method of claim 7, wherein said photosensor is one of a photodiode, photogate, or photoconductor.

13. The method of claim 12, wherein said photodiode is a p-n-p photodiode.

14. The method of claim 7, wherein removing said second dielectric layer comprises a photoresist masking process.

15. The method of claim 7, wherein removing said second dielectric layer comprises a wet or dry etch process.

16. The method of claim 7, wherein removing said second dielectric layer comprises removing said second dielectric from said pixel region.

17. The method of claim 7, wherein removing said second dielectric layer comprises removing said second dielectric from said periphery region.

18. An imaging device, comprising:

a semiconductor substrate;

at least one photosensor;

a first electrode layer over said substrate in a pixel region and a periphery region of said imaging device;

a first dielectric layer over said first electrode layer;

a second dielectric layer over said first dielectric layer; and

a second electrode layer over said second dielectric layer.

19. The device of claim 18, wherein said first electrode layer is formed of a material selected from the group consisting of a poly, poly/WSi, poly/WN/W, poly/silicide, poly/metal and metal.

20. The device of claim 18, wherein said photosensor is one of a photodiode, photogate or photoconductor.

21. The device of claim 18, wherein said first dielectric layer comprises a material selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, BST, metal oxide and HfO_x.

22. The device of claim 18, wherein said second dielectric layer comprises a material selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, BST, metal oxide and HfO_x.

23. The device of claim 18, wherein said second electrode layer is formed of a material selected from the group consisting of a polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$, poly/$MoSi_2$, poly/metal and metal.

24. An imaging device, comprising:

a substrate;

at least one photosensor;

at least one in-pixel capacitor formed in the pixel array region of said substrate, said at least one in-pixel capacitor comprising a first electrode, a first plurality of dielectric layers and a second electrode; and

at least one peripheral capacitor formed in a peripheral region of said substrate, said peripheral region being adjacent said pixel array region, said at least

one peripheral capacitor comprising said first electrode, a second plurality of dielectric layers, and said second electrode.

25. The device of claim 24, wherein the capacitance of said at least one in-pixel capacitor is different from the capacitance of said at least one peripheral capacitor.

26. The device of claim 24, wherein the capacitance of said at least one in-pixel capacitor is greater than the capacitance of said at least one peripheral capacitor.

27. The device of claim 24, wherein the capacitance of said at least one peripheral capacitor is greater than the capacitance of said at least one in-pixel capacitor.

28. The device of claim 24, wherein said first electrode is formed of a material selected from the group consisting of a poly, poly/WSi, poly/WN/W, poly/silicide, poly/metal and metal.

29. The device of claim 24, wherein said first plurality of dielectric layers and said second plurality of dielectric layers are formed of a material independently selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, BST, metal oxide and HfO_x.

30. The device of claim 24, wherein said second electrode layer is formed of a material selected from the group consisting of a polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$, poly/$MoSi_2$, poly/metal and metal.

31. The device of claim 24, wherein said photosensor is one of a photodiode, photogate or photoconductor.

32. The device of claim 31, wherein said photodiode is a p-n-p photodiode.

33. The device of claim 24, wherein said first plurality of dielectric layers is different from said second plurality of dielectric layers.

34. The device of claim 24, wherein at least one of said first plurality of dielectric layers is different from one of said second plurality of dielectric layers.

35. The device of claim 24, wherein said first plurality of dielectric layers is similar to said second plurality of dielectric layers.

36. The device of claim 24, wherein the imaging device is a CMOS imager.

37. A CMOS imager system, comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging device comprising:

a semiconductor substrate;

at least one photosensor;

a first electrode layer over said substrate in a pixel region and a periphery region of said imaging device;

a first dielectric layer over said first electrode layer;

a second dielectric layer over said first dielectric layer; and

a second electrode layer over said second dielectric layer.

38. The CMOS imager system of claim 37, wherein said processor comprises circuits for signal amplification, row addressing, column addressing, white balance, color correction, image correction, and defect correction.

39. A CCD imaging device, comprising:

a semiconductor substrate;

at least one photosensor;

a first electrode layer over said substrate in a pixel region and a periphery region of said imaging device;

a first dielectric layer over said first electrode layer;

a second dielectric layer over said first dielectric layer; and

a second electrode layer over said second dielectric layer.

40. The device of claim 39, wherein said first electrode layer is formed of a material selected from the group consisting of a poly, poly/WSi, poly/WN/W, poly/silicide, poly/metal and metal.

41. The device of claim 39, wherein said first dielectric layer is formed of a material selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, BST, metal oxide and HfO_x.

42. The device of claim 39, wherein said second dielectric layer is formed of a material selected from the group consisting of an oxide, nitride, Al_2O_3, Ta_2O_5, BST, metal oxide and HfO_x.

43. The device of claim 39, wherein said second electrode layer is formed of a material selected from the group consisting of a polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$, poly/$MoSi_2$, poly/metal and metal.

44. A CCD imager system, comprising:

(i) a processor; and

(ii) a CCD imaging device coupled to said processor, said CCD imaging device comprising:

a semiconductor substrate;

at least one photosensor;

a first electrode layer over said substrate in a pixel region and a periphery region of said imaging device;

a first dielectric layer over said first electrode layer;

a second dielectric layer over said first dielectric layer; and

a second electrode layer over said second dielectric layer, wherein at least one of said first dielectric layer and second dielectric layer differs between said pixel region and said periphery region to form different in-pixel capacitors and periphery capacitors.

45. The CCD imager system of claim 44, wherein said processor comprises circuits for signal amplification, row addressing, column addressing, white balance, color correction, image correction, and defect correction.

46. An imaging device, comprising:

a substrate;

at least one photosensor;

a first type capacitor in the array and in the periphery, wherein the first type capacitor in the array is the same as the first type capacitor in the periphery; and wherein the first type capacitor comprises a first electrode, a first plurality of dielectric layers and a second electrode; and

a second type capacitor in the array, wherein the second type capacitor comprises said first electrode, a second plurality of dielectric layers, and said second electrode.

47. An imaging device, comprising:

a substrate;

at least one photosensor;

a first type capacitor in the array and in the periphery, wherein the first type capacitor in the array is the same as the first type capacitor in the periphery, and wherein the first type capacitor comprises a first electrode, a first plurality of dielectric layers and a second electrode; and

a second type capacitor in the array and in the periphery, wherein the second type capacitor in the array is the same as the second type capacitor in the periphery, and wherein the second type capacitor comprises said first electrode, a second plurality of dielectric layers, and said second electrode.

48. An imaging device, comprising:

a substrate;

at least one photosensor;

a first type capacitor in the array and in the periphery, wherein the first type capacitor in the array is the same as the first type capacitor in the periphery, and wherein the first type capacitor comprises a first electrode, a first plurality of dielectric layers and a second electrode; and

a second type capacitor in the periphery, wherein the second type capacitor comprises said first electrode, a second plurality of dielectric layers, and said second electrode.

49. A CCD imager system, comprising:

(i) a processor; and

(ii) a CCD imaging device coupled to said processor, said CCD imaging device comprising:

a semiconductor substrate;

at least one photosensor;

a first type capacitor in the array and in the periphery, wherein the first type capacitor in the array is the same as the first type capacitor in the periphery, and wherein the first type capacitor comprises a first electrode, a first plurality of dielectric layers and a second electrode; and

a second type capacitor in the periphery, wherein the second type capacitor comprises said first electrode, a second plurality of dielectric layers, and said second electrode.