CLAIMS

1. A system comprising:

a plurality of machines comprising a first generation machine, a second generation machine, and a third generation machine, each of the plurality of machines comprising a machine version;

the first, second and third generation machines comprising different machine versions, the first generation machine executing a first virtual machine (1920) and a virtual architecture level, the second generation machine executing a second virtual machine (1950) and the virtual architecture level, and the third generation machine executing a third virtual machine (1980) and the virtual architecture level, wherein the system is characterised by:

the virtual architecture level being configured to provide a compatibility level for a complex interruptible instruction to the first, second and third virtual machines,

the compatibility level being architected for a lowest common denominator machine version across the plurality of machines,

the compatibility level comprising a lowest common denominator indicator (1931) identifying the lowest common denominator machine version,

the complex interruptible instruction having a state that is required to be saved out and meets formatting requirements,

the compatibility level comprises a parameter block format (1930) associated with the lowest common denominator indicator (1931),

the compatibility level comprises a local parameter block format for the complex interruptible instruction for each of the plurality of machines, the local parameter block format being architected for the machine version local to each of the plurality of machines,

the lowest common denominator indicator (1931) is generated by a machine of the plurality of machines to first execute the complex interruptible instruction, and

the lowest common denominator indicator (1931) is propagated from the machine of the plurality of machines to first execute the complex interruptible instruction to a remaining number of the plurality of machines.

2. The system of claim 1, wherein the lowest common denominator indicator (1931) within the compatibility level is controlled through a series of facility bits that identify which functions are available in a particular virtual machine.

3. The system of any preceding claim, wherein the complex interruptible instruction comprises a DEFLATE Conversion Call instruction.

4. The system of claim 1, wherein the complex interruptible instruction comprises an instruction from a complex set of instructions running on an accelerator.

5. A method comprising:

executing a first virtual machine (1920) and a virtual architecture level by a first generation machine of a plurality of machines, each of the plurality of machines comprising a machine version;

executing a second virtual machine (1950) and the virtual architecture level by a second generation machine of the plurality of machines;

executing a third virtual machine (1980) and the virtual architecture level by a third generation machine of the plurality of machines; characterised by:

providing, by the virtual architecture level, a compatibility level for a complex interruptible instruction to the first, second and third virtual machines,

the compatibility level being architected for a lowest common denominator machine version across the plurality of machines,

the compatibility level comprising a lowest common denominator indicator (1931) identifying the lowest common denominator machine version,

wherein the complex interruptible instruction comprises a state that is required to be saved out and meets formatting requirements,

wherein the compatibility level comprises a parameter block format (1930) associated with the lowest common denominator indicator (1931),

wherein the compatibility level comprises a local parameter block format for the complex interruptible instruction for each of the plurality of machines, the local parameter block format being architected for the machine version local to each of the plurality of machines,

wherein the lowest common denominator indicator (1931) is generated by a machine of the plurality of machines to first execute the complex interruptible instruction, and

wherein the lowest common denominator indicator (1931) is propagated from the machine of the plurality of machines to first execute the complex interruptible instruction to a remaining number of the plurality of machines.

6. The method of claim 5, wherein the lowest common denominator indicator (1931) within the compatibility level is controlled through a series of facility bits that identify which functions are available in a particular virtual machine.

7. The method of claim 5, wherein the complex interruptible instruction comprises a DEFLATE Conversion Call instruction.

8. The method of claim 5, wherein the complex interruptible instruction comprises an instruction from a complex set of instructions running on an accelerator.

9. A computer program product comprising a computer readable storage medium having program instructions embodied therewith, the program instructions executable to cause operations comprising all the steps of any of method claims 5 to 8.