THIS SHEET HAS BEEN REPLACED

Abstract.

The capacitor of a DRAM cell is formed by depositing a layer of doped polysilicon patterning the layer of doped polysilicon to define the extent of the capacitor's lower electrode and then depositing a first layer of hemispherical-grained silicon (HSG-Si) on the layer of doped polysilicon. Growth of the first layer of HSG-Si is interrupted and then a second layer of HSG-Si is grown. In one aspect, growth of the first layer of HSG-Si may be interrupted by either cooling the deposition substrate or stopping deposition for a period of time and then reinitiating deposition to provide a second layer of HSG-Si on the surface of the electrode. The interruption of the growth of the first layer, whether by cooling or by delay, is sufficient if the reinitiated growth initiates in a manner that is independent of the first process; *i.e.*, the second layer of HSG-Si grows independently. In a different aspect of the invention, growth of the first layer may be interrupted by removing the electrode from the deposition system and performing an etch back operation. After the etch back operation, the electrode is reintroduced to the deposition system and a second layer of HSG-Si is grown on the etched surface. This textured silicon structure forms the lower electrode of the DRAM capacitor.

(Fig. 3)

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