

Description

This invention relates to circuits for amplifying signals produced by a magnetoresistive element used to read data recorded on a magnetisable recording element, and more particularly to such circuits for protecting the magnetoresistive element from the occurrence of undesirably large currents.

A magnetic transducer referred to as a magnetoresistive (MR) sensor or head has been shown to be capable of reading data from a surface magnetised at high linear densities. An MR sensor detects magnetic field signals through the resistance changes of a read element made from a magnetoresistive material. This resistance change is a function of the magnitude and direction of magnetic flux being sensed by the element.

US-A-4,492,997 discloses an MR head in which the MR element is a two terminal device connected to serve as a portion of the negative feedback resistor of an amplifier circuit so that the amplifier circuit serves both to supply a drive current to the MR element and to amplify the signal derived from the MR element.

US-A-4,660,113 discloses an MR sensor in which the MR element has three terminals with the centre terminal connected to ground potential. The outputs from the other two terminals are differentially amplified by a differential amplifier to eliminate external noise signals picked up by the head.

In magnetic recording technology it is continually desired to improve the areal density at which information can be recorded and reliably read. This desire has led to a trend toward greater bit density along a magnetic recording track and a shrinking track width. The greater bit density requires increasingly narrow transducing gaps, increasingly narrow track width, and progressively lower flying height to record and read data reliably.

The MR elements needed to meet these requirements are generally small. This factor, along with the lower flying height, leads to an increased chance of damage to the MR element due to currents flowing between the element and its environment. One example is the current caused by intermittent contact between the element and the magnetic recording disk which can lead to intermittent short circuits of the element to the magnetic disk substrate potential. Another example is the current flowing due to galvanic corrosion between the material of the element and the disk magnetic coating or substrate materials in a humid atmosphere.

US-A-4,706,138 and US-A-4,712,144 disclose circuits for amplifying signals produced by an MR element. These circuits have been shown to operate effectively in amplifying signals produced by the small MR sensors described above.

A protection circuit according to the precharacterizing part of claim 1 is known from EP-A-0 181 467, which discloses a feedback circuit preventing from overload to the MR element by keeping the maximum supply voltage to the MR element constant for all operating temperatures.

However, neither the above-mentioned patent specifications nor any other known documents disclose a circuit for protecting the MR element from these damaging currents in the environment of the MR element.

The object of the present invention is to provide a protection circuit for an MR element which prevents damage to the MR element due to currents to or from the adjacent magnetic recording medium.

The invention relates to a protection circuit for a magnetoresistive (MR) element having a first terminal and a second terminal. A first current source is coupled to the first terminal of the MR element to produce a bias current through the MR element, and a second current source is coupled to the second terminal of the MR element to produce a reference current.

According to the invention the protection circuit also includes circuit means coupled across the first and second terminals of the MR element for sensing the centre potential of the MR element at a position substantially midway between the first terminal and the second terminal of the MR element, and feedback circuit means responsive to the sensed centre potential of the MR element to adjust the current output of the first current source to maintain the centre potential to a predetermined reference voltage.

To prevent damage to the MR element in the event of contact between the MR element and conductive areas of the magnetic recording medium, this reference voltage is preferably chosen such that the discharge current of the (parasitic) capacitance between the MR element and the substrate is kept small. Preferably, this reference voltage is equal to the substrate voltage.

The signal across the MR element can be amplified to produce a signal voltage varying as a function of the magnetic flux being sensed by the MR element. According to another feature of the invention a second feedback circuit may be provided to compensate the dc voltage sensed across the MR element, essentially removing this dc voltage produced by the bias current across the head and leaving only the signal voltage.

In order that the invention may be more readily understood an embodiment will now be described with reference to the accompanying drawings, in which:-

Fig. 1 is a block diagram of the basic concept of a protection circuit constructed for a magnetoresistive element,

Fig. 2 is a circuit diagram of a first feedback loop included in the circuit illustrated in Fig. 1,

Fig. 3 is a graph showing the short circuit current for an MR element protected by the circuit illustrated in Fig. 1,

Fig. 4 is a circuit diagram of a second feedback loop included in the circuit illustrated in Fig. 1,

Fig. 5 is a more detailed circuit diagram of the feedback loop illustrated in Fig. 4,

Fig. 6 is a Bode diagram illustrating the frequency response of the signal path of an amplifier constructed according to Figs 1, 2, 4 and 5,

Fig. 7 is a more detailed circuit diagram of the amplifier and biasing circuit components illustrated in Fig. 5,

Fig. 8 is a circuit diagram of a complete preamplifier for two read heads including magnetoresistive elements incorporating the circuits illustrated in Figs. 1, 2, 4, 5 and 6 and showing nodes related to and capable of switching from one head to another, and

Fig. 9 is a graph showing the transient response during head switching of the preamplifier illustrated in Fig. 8 for three separate conditions.

The basic concept for the implementation of a low-noise and high-bandwidth differential preamplifier having short circuit protection for a magnetoresistive (MR) element usable in a read head will now be described with reference to Fig. 1. A first current source I_{ref} is coupled to a first terminal of the MR element R_h and a second current source $J1$ is coupled to a second terminal of the MR element R_h . A first feedback loop is provided to control current source $J1$ relative to I_{ref} so that the MR element is properly biased and the electrical centre of R_h is set to a desired potential V_{centre} . The first feedback loop comprises a resistor network comprising equal resistors R connected across the MR element R_h to derive the electrical-centre potential and a differential amplifier B which compares this electrical-centre potential and a desired potential V_{centre} . The resistors R are much greater in resistance than R_h . The output of differential amplifier B is coupled to control the second current source $J1$. This protection circuit operates on the basis of maintaining the current into the MR element equal to the current out of the MR element to null any ground return current that might flow when any exposed portion of the element is short circuited to the magnetisable disk substrate with which the magnetoresistive element is being used and which is usually grounded. To that end the controllable current source $J1$ is made to respond only slowly to the control signal from amplifier B . A short-duration conductive contact between the MR element and the disk will therefore not upset the current balance between current source $J1$ and current source I_{ref} . In addition, the electrical centre voltage of the element can be maintained at any desired potential. To protect against short circuits to a conductive area of the magnetic recording medium, the desired potential would logically be selected as ground potential to protect also against any capacitive discharge of the parasitic capacitance from the MR element and its connecting leads to ground. Should it be desired to protect the MR element from galvanic corrosion damage, a small negative potential of the same order of magnitude as the galvanic cell voltage of the pertinent material combination would be selected as the desired potential, V_{centre} .

A second feedback loop is provided inside gain block A to suppress the large dc component of the bias voltage developed across the MR element, which results in amplification of only the small high-frequency (data) signal.

The detailed circuit of the first feedback loop of Fig. 1 is shown in Fig. 2. The currents i_b represent the non-zero base biasing currents needed for the input transistors of gain block A in Fig. 1. Resistors $R16$, $R17$, and $R2$ develop the MR element centre potential for the differential amplifier B which comprises transistors $Q3$ and $Q4$. Resistors $R4$ and $R5$ are used to control the loop gain of the first feedback loop. Capacitor $C2$ sets the dominant time constant of the feedback loop which determines the response time of $J1$ in Fig. 1 to a change in the electrical centre potential. The PNP Darlington pair consisting of $Q1$ and $Q2$ are used to ensure a high impedance at the base of $Q1$ to minimise capacitance needed even with low beta PNP devices. Diodes $D1$ and $D1a$ thermally compensate the loop. Current source $J7$ is used both as a biasing source for the differential amplifier B and as a feedforward current to ensure minimum steady state error under all statistical conditions. Although V_{centre} can have a wide range of voltage potentials, for purposes of protecting the MR element from short circuits to a conductive asperity on a disk with a grounded substrate, this potential is chosen as ground potential. As pointed out above, galvanic corrosion protection can be provided by choosing V_{centre} to be a small negative voltage.

If V_{centre} is at ground potential and diodes $D1$ and $D1a$ have similar base-to-emitter voltages as do $Q1$ and $Q2$, then the following applies:

$$V_{cm} = \left(\frac{R1' J7}{2R3'} - J1 - 2ib \right) \frac{\frac{R16 + R2}{2}}{1 + \frac{R2R1'}{R3'(R4' + R5')}} \quad [1]$$

where

V_{cm} = actual voltage at centre of MR element

$$R1' = (4 \frac{V_i}{J7} + R1c) \parallel \beta_p R3'$$

where $\parallel$ means in parallel with

$$R3' = \frac{V_i}{J7} + R3$$

$$R16 = R17 = R2$$

$$R4' = R5' = R4 + 2 \frac{V_i}{J7}$$

$V_t = 26 \text{ mV}$

β_p = current gain of PNP devices

ib = base current of input stage to preamplifier

$$I_{sib} = \frac{-Rh(J1 + ib)}{2Rh + 3R16} \quad [2]$$

$$I_{sit} = -I_{sib} \quad [3]$$

$$I_{sfb} = \frac{\frac{J7}{2} - ib \frac{R3'}{R1'}}{\frac{R3'}{R1'} + \frac{RhR16}{(2Rh + 3R16)(R4' + R5')}} \frac{3R16 + Rh}{3R16 + 2Rh} \quad [4]$$

$$I_{sft} = \left\{ \frac{J7}{2} + \frac{(J1 + ib)R16Rh}{(R4' + R5')(3Rh + 3R16)} \right\} \frac{R1'}{R3'} - \frac{(3R16 + Rh)(ib + J1)}{(3R16 + 2Rh)} - ib \quad [5]$$

where

I_{sib} = initial short circuit current from most negative head terminal to ground (time = 0+)

I_{sit} = initial short circuit current from most positive head terminal to ground

I_{sfb} = final short circuit current from most negative head terminal to ground (time = ∞)

I_{sft} = final short circuit current from most positive head terminal to ground

$$\tau' = R1'C2$$

$$GL = \text{Loop Gain} = \frac{R1'R2}{R3'(R4' + R5')} \quad [6]$$

$$\tau = \frac{\tau'}{GL} = \text{dominant closed loop time constant} \quad [7]$$

The short circuit current in accordance with the above equations is shown in Fig. 3. The current starts at I_{sf} at time $t=0$ and has an exponential characteristic up to a final current of I_{sf} . The characteristic shown is dominated by a relatively slow loop response needed for a low maximal allowed short circuit current. This is indicated by the "max safe level" threshold in Fig. 3. To ensure that the short circuit current never exceeds the "max safe level", the duration of the short circuit cannot exceed a maximum asperity contact time. By reference to Equation (1) it can be seen that current J7 (Fig. 2) acts as a feedforward current which can set the steady state error to zero in the nominal case. Since most short circuits between the magnetisable recording medium and the MR element are transitory in nature, the circuit provides adequate short circuit protection.

It is important to provide short circuit protection even for the transitory short circuits which may occur, since these transitory short circuits can result in erosion of a micro-area of the material forming the MR element. The cumulative effect of this erosion of micro-areas produces a recession of the sensing edge of the MR element which faces the magnetisable recording medium, and this recession results in a significant reduction in the sensitivity of the MR element. Of course, short circuit currents of a larger magnitude have greater impact which may result in a greater and more rapid decrease in sensitivity of the MR element. The circuit described above provides adequate short circuit protection against these transitory short circuits and can keep these currents well below a safe maximum allowable level. It also provides protection for capacitive discharge damage to the MR element. It can provide protection from galvanic corrosion as well.

Greatly increased short circuit protection can also be achieved by considering a nonlinear effect, that of slew rate limitation, which can be dominant over the linear time constant of the biasing loop described above, upon the proper selection of certain component values.

When a short circuit to ground occurs at either end of the MR element, then a charging current I_{Δ} for capacitor C2 can be defined as

$$I_{\Delta} = \frac{J7}{2} + \frac{V_{cm} + (J1 + i_b) \frac{R_h}{2}}{R4' + R5'} \quad [7a]$$

The change in voltage across capacitor C2 needed to cause short circuit currents I_{sfb} or I_{sft} is V_{Δ} where

$$V_{\Delta} = I_{sf} R1' \quad [7b]$$

The time needed to charge the capacitor sufficiently to attain short circuit currents I_{sf} is then T_{Δ} where

$$T_{\Delta} = C2 \frac{V_{\Delta}}{I_{\Delta}} \quad [7c]$$

If J7 is made small and C2 is made large, then the time required before a specified I_{sf} can flow becomes considerably longer, because of the inherent slew rate limitation non-linearity, than the previous linear time constant described above.

Feedback loop number two inside the gain block A in Fig. 1 is shown generally in Fig. 4 in which input devices Q17 and Q18 correspond to amplifier A and amplify the signal voltage V_i at the MR element. Transconductance stage (go) feeds back the amplified signal V_o as a current to the base of current source transistor Q21. Capacitor C1 generates a dominant time constant for the loop, thereby producing a high-pass response of V_o relative to V_i . The total biasing current for the differential input stage consisting of Q17 and Q18 changes as different values of R_h are used. The reason for this is that the voltage developed across resistor R_e is made equal to the biasing voltage across head resistance R_h by adjusting the dc current through Q21 to keep the dc currents through each input device equal. In general R_e can be bypassed by capacitor C_e to generate impedance Z_e in order to reduce the amplifier noise as shown dotted in Fig. 4.

A more detailed schematic of transconductance stage go is shown in Fig. 5. Here, only a fraction of the output signal V_o is fed back by two equivalent resistor divider networks comprising respectively $R9/R11$, and $R10/R12$ and a differential voltage follower consisting of Q8 and Q9, series diodes nD3 and nD4 and bias currents J3 and J4. A voltage to current conversion is accomplished by differential pair Q15 and Q16 and bias source J5. The output currents of this stage are mirrored and the differential current is fed to capacitor C1. The charging current is mirrored by one PNP current mirror consisting of transistors Q12, Q13 and Q14 and resistors R13, R14 and R15. The discharging current is mirrored by a PNP mirror and an NPN

mirror. The PNP mirror consists of transistors Q5, Q6 and Q7, and resistors R6, R7 and R8. The NPN current mirror consists of diode D2 and transistor Q20. Current J2 is used as a feed-forward current which supplies the minimal current needed for the minimum resistance of R_h to the input stage. Current J8 supplies an additional feedforward current which, when combined with feedforward current J2, will result in the correct current supplied to the input stage for the nominal case resistance of R_h being used. Thus currents can be added to (or subtracted from) current J8 via the current output of the second feedback loop to obtain correct biasing currents for the input devices for all values of R_h . Since the NPN mirror may become close to saturation, especially when the collector current of Q21 becomes very small (as it is with a minimum value for the resistance of R_h), it becomes necessary to construct the mirror such that saturation cannot occur. Thus the simple topology of the NPN current mirror is one solution, in tandem with ensuring that the collector current of Q21 will be well above zero even with a minimal value of R_h . This can be done by decreasing the amount of feedforward current from J2 slightly, and increasing the value of feedforward current from J8 correspondingly, relative to the initial settings previously discussed.

The important equations characterising the second feedback loop are:

$$H(s) = \frac{V_o}{V_i} = \frac{-2RL(st'' + 1)}{(sA\tau'' + 1)(R_e + 2re + \gamma K\beta_n R_e \frac{RL}{re'})} \quad [8]$$

Where $H(s)$ does not include the effects of internally applied feedforward current by J2 and J8 and where

$$RL = R9 + R11$$

$$re = \frac{V_t R_e}{J1 R_h}$$

$$\gamma = \frac{R11}{R9 + R11}$$

$$re' = 2 \frac{V_t}{J8}$$

K = current gain of PNP mirrors assuming that the gain of the NPN mirror = 1

β_n = beta of NPN devices

s = Laplace operator

and where:

$$\tau'' = \beta_n C1 (R18 + re'') \quad [9]$$

$$re'' = \frac{V_t}{2J1 \frac{R_h}{R_e} - J2 - \beta_n J8} \quad [10]$$

$$A = \frac{2r_e + R_e}{R_e + 2r_e + \frac{\gamma K \beta n R_e R_L}{r_e}} \quad [11]$$

5

$$V_o(dc) = \frac{(J_2 + \beta n J_8) R_e - 2J_1 R_h}{1 + \frac{2r_e + R_e}{R_L}} \quad [12]$$

10

15 where $V_o(dc)$ is the dc output offset at V_o with internal feedforward and base biasing currents $i_b = J_1 R_h / R_e \beta n$.

The ac response of the amplifier is shown on the Bode plot of Fig. 6. Here, the dominant low frequency pole of the second feedback loop results in the low frequency rolloff shown.

20 The biasing and amplifying circuit components are shown interconnected in Fig. 7. Here, extra diodes are shown in the voltage follower stage to alleviate dynamic range constraints caused by a common-mode voltage change at V_o because the circuit must operate with a range of resistances R_h .

The complete preamplifier capable of switching from one read head to another is shown in Fig. 8. A cascode stage consisting of transistors Q10 and Q11, diodes D11 and D12 and resistor R23 has been included to allow for one of several input stages to be used. Each input stage consists of an amplifying stage connected to an MR element. Each amplifying stage is connected in a dot-OR configuration to the input to the differential cascode stage at nodes n3 and n4. Fig. 7 shows only one such stage consisting of transistors Q17, Q18, Q19a, Q19b, Q26, and Q27, resistors R_e , R17 and R18 and head R_h . Biasing for all input amplifiers is common at node n5. Transistor switches Q19 are then switched ON or OFF by a control signal at node n_c to supply the biasing current to any one of the several input amplifier stages. Concurrently with the aforesaid control signal, control signals at nodes n_a and n_b are also appropriately changed to allow the reference biasing current J_1 to bias the appropriate MR element. Nodes n1, n2, n3, n4, n5 and n6 are common to both each separate input stage and to a part of the amplifier common to all input stages. Control signals at nodes n_a , n_b and n_c are peculiar only to each individual input stage of which only one can be turned on at any one time.

35 Bias current J_5 is made variable to accommodate a fast switching mode which occurs immediately after a switchover. A switchover includes switching from one read head to another or from a standby or write mode to a read mode in a disk file system. A signal of known time duration is sent to the preamplifier by external logic circuitry immediately following a switchover, whereby current J_5 is increased for the duration of the timing signal. Increasing J_5 by a factor of N will correspondingly increase the loop gain of the second feedback loop by N and thus increase the dominant low frequency pole by N . If N is sufficiently large, the otherwise long linear exponential decay associated with the transient response during a switchover can be shortened considerably. Since the charging current and discharging current are also increased by N , any slew rate limiting factor associated with adjusting the voltage across capacitor C1 will also be reduced in short order. Since, during this temporary high gain mode immediately following a switchover, the loop gain has changed, so then has the steady state error at V_o . The steady state error for the nominal case in the high gain mode can be made the same as the steady state error for the nominal case in the normal lower gain mode by also temporarily applying another feedforward current J_6 . This temporary application of feedforward current only during the high gain mode serves to minimise the transient response time in general.

50 The general transient response as seen at V_o is shown in Fig. 9. Here, three different transient responses are shown. Response 1 is that associated with switching from a read head of nominal resistance to another read head of the same resistance. Since this case is exactly what the temporary feedforward current J_6 was designed for, the transient time is the shortest possible. Response 2 represents a switchover from a read head of the lowest specified resistance to a head of the highest specified resistance, while response 3 is the reverse of response 2. In responses 2 and 3, it becomes apparent that the transient response in general is dominated by several distinct effects. The first and most predominant effect is that of the slew rate limitation in the high gain mode immediately following a switchover. This effect is minimised by the aforementioned increase in charging/discharging current available for the capacitor C1. After the slew

rate limitation has subsided, the increased pole frequency of the second feedback loop improves the linear decay to steady state N times faster than expected with the normal loop response. After the high gain mode ends (in this case at 10 s), the normal loop gain of the second feedback loop responds to a change in the steady state error between the high gain and low gain modes for the non-nominal general case. After this
 5 response decays, then the remainder of the transient response is dominated by the lowest pole frequency found in the first feedback loop.

Claims

- 10 1. A protection circuit for a magnetoresistive element (Rh) having a first terminal and a second terminal comprising,
 - a first current source coupled to said first terminal of said magnetoresistive element for producing a bias current (J1) through said magnetoresistive element and
 - 15 a second current source coupled to said second terminal of said magnetoresistive element to produce a reference current (Iref),
 - circuit means (R) coupled across said first and said second terminals of said magnetoresistive element characterised in that the circuit means senses the centre potential of said magnetoresistive element at a position substantially midway between said first terminal and said second terminal; and
 - 20 feedback circuit means (B) responsive to the sensed centre potential of said magnetoresistive element to adjust the current output (J1) of said first current source to maintain said centre potential to a predetermined reference voltage (Vcentre).
2. A protection circuit as claimed in claim 1, characterised in that said circuit means comprises
 - 25 two equal resistors (R) connected in series across said magnetoresistive element and means for sensing the centre potential of said magnetoresistive element at the junction between the two resistors.
3. A protection circuit as claimed in either of the preceding claims characterised in that said feedback circuit means comprises
 - 30 a differential amplifier (B) having two input terminals and an output terminal,
 - means connecting said sensed centre potential to one of said input terminals,
 - means connecting said predetermined reference voltage to the other of said input terminals; and
 - means coupling the output of said amplifier to control the current output of said first current source.
- 35 4. A protection circuit as claimed in any one of the preceding claims, characterised in that said predetermined reference voltage is ground potential.
5. A protection circuit as claimed in any one of claims 1, 2 or 3, characterised in that said predetermined reference voltage is a small negative voltage.
- 40 6. A protection circuit as claimed in any one of the preceding claims characterised in that it further comprises
 - means (A) for amplifying the signal voltage across said magnetoresistive element produced as a function of a magnetic flux sensed by said magnetoresistive element and including a second feedback
 - 45 circuit coupled to feed back a portion of the voltage sensed across said magnetoresistive element to remove the dc voltage due to said bias current and leave only said signal voltage.
7. A protection circuit as claimed in claim 6 characterised in that said second feedback circuit comprises
 - an input circuit having at least two transistors (Q17, Q18) coupled in a differential pair configuration
 - 50 and having the magnetoresistive element coupled between the bases of said transistors,
 - a reference resistor (Re) connected between the emitters of said transistors, and
 - a transconductance stage (Go) coupled between the collectors of said transistors, said transconductance stage having an output coupled to said transistors to supply a feedback current to maintain the dc current through each of said transistors equal so that only the signal voltage due to the magnetic
 - 55 flux being sensed by said magnetoresistive element is coupled to an output terminal.



rate limitation has subsided, the increased pole frequency of the second feedback loop improves the linear decay to steady state N times faster than expected with the normal loop response. After the high gain mode ends (in this case at 10 s), the normal loop gain of the second feedback loop responds to a change in the steady state error between the high gain and low gain modes for the non-nominal general case. After this response decays, then the remainder of the transient response is dominated by the lowest pole frequency found in the first feedback loop.

Claims

- 10 1. A protection circuit for a magnetoresistive element (R_h) having a first terminal and a second terminal comprising,
 - a first current source coupled to said first terminal of said magnetoresistive element for producing a bias current (J_1) through said magnetoresistive element and
 - 15 a second current source coupled to said second terminal of said magnetoresistive element to produce a reference current (I_{ref}),
 - circuit means (R) coupled across said first and said second terminals of said magnetoresistive element characterised in that the circuit means senses the centre potential of said magnetoresistive element at a position substantially midway between said first terminal and said second terminal; and
 - 20 feedback circuit means (B) responsive to the sensed centre potential of said magnetoresistive element to adjust the current output (J_1) of said first current source to maintain said centre potential to a predetermined reference voltage (V_{centre}).
2. A protection circuit as claimed in claim 1, characterised in that said circuit means comprises
 - 25 two equal resistors (R) connected in series across said magnetoresistive element and means for sensing the centre potential of said magnetoresistive element at the junction between the two resistors.
3. A protection circuit as claimed in either of the preceding claims characterised in that said feedback circuit means comprises
 - 30 a differential amplifier (B) having two input terminals and an output terminal, means connecting said sensed centre potential to one of said input terminals, means connecting said predetermined reference voltage to the other of said input terminals; and means coupling the output of said amplifier to control the current output of said first current source.
- 35 4. A protection circuit as claimed in any one of the preceding claims, characterised in that said predetermined reference voltage is ground potential.
5. A protection circuit as claimed in any one of claims 1, 2 or 3, characterised in that said predetermined reference voltage is a small negative voltage.
- 40 6. A protection circuit as claimed in any one of the preceding claims characterised in that it further comprises
 - means (A) for amplifying the signal voltage across said magnetoresistive element produced as a function of a magnetic flux sensed by said magnetoresistive element and including a second feedback circuit coupled to feed back a portion of the voltage sensed across said magnetoresistive element to remove the dc voltage due to said bias current and leave only said signal voltage.
 - 45
7. A protection circuit as claimed in claim 6 characterised in that said second feedback circuit comprises
 - an input circuit having at least two transistors (Q_{17} , Q_{18}) coupled in a differential pair configuration
 - 50 and having the magnetoresistive element coupled between the bases of said transistors,
 - a reference resistor (R_e) connected between the emitters of said transistors, and
 - a transconductance stage (G_o) coupled between the collectors of said transistors, said transconductance stage having an output coupled to said transistors to supply a feedback current to maintain the dc current through each of said transistors equal so that only the signal voltage due to the magnetic flux being sensed by said magnetoresistive element is coupled to an output terminal.
 - 55



Patentansprüche

1. Eine Schutzschaltung für ein magnetoresistives Element R_h mit einem ersten Anschluß und einem zweiten Anschluß, das folgendes umfaßt:
 5 eine erste Stromquelle, die mit dem ersten Anschluß des magnetoresistiven Elements zur Erzeugung eines Vorspannungsstroms (J_1) durch das magnetoresistive Element gekoppelt ist, und
 eine zweite Stromquelle, die mit dem zweiten Anschluß des magnetoresistiven Elements zur Erzeugung eines Vergleichsstroms (I_{ref}) gekoppelt ist,
 wobei die Schaltung durch folgendes gekennzeichnet ist:
 10 ein Schaltmittel (R), das über den ersten und zweiten Anschluß des magnetoresistiven Elements gekoppelt ist, wobei das Schaltmittel das Mittelpotential des magnetoresistiven Elements an einer Position in der Mitte zwischen dem ersten und zweiten Anschluß aufnimmt; und
 ein Rückkopplungsschaltmittel (B), das auf das aufgenommene Mittelpotential des magnetoresistiven Elements anspricht, um den Stromausgang (J_1) der ersten Stromquelle zu regulieren, so daß das
 15 Mittelpotential auf einer festgelegten Vergleichsspannung (V_{Mitte}) gehalten werden kann.
2. Eine Schutzschaltung nach Anspruch 1, die dadurch gekennzeichnet ist, daß das Schaltmittel folgendes umfaßt:
 zwei gleiche Widerstände (R), die seriell über das magnetoresistive Element angeschlossen sind, und
 20 ein Mittel zur Erkennung des Mittelpotentials des magnetoresistiven Elements am Schnittpunkt zwischen den beiden Widerständen.
3. Eine Schutzschaltung nach einem der oben genannten Ansprüche, die dadurch gekennzeichnet ist, daß das Rückkopplungsschaltmittel folgendes umfaßt:
 25 einen Differentialverstärker (B) mit zwei Eingangsanschlüssen und einem Ausgangsanschluß,
 ein Mittel zum Anschluß des aufgenommenen Mittelpotentials an einen der Eingangsanschlüsse,
 ein Mittel zum Anschluß der festgelegten Vergleichsspannung an den anderen Eingangsanschluß, und
 ein Mittel zum Koppeln des Ausgangs des Verstärkers, um den Stromausgang der ersten Stromquelle zu regulieren.
 30
4. Eine Schutzschaltung nach einem der oben genannten Ansprüche, die dadurch gekennzeichnet ist, daß die festgelegte Vergleichsspannung ein Massepotential ist.
5. Eine Schutzschaltung nach einem der Ansprüche 1, 2 oder 3, die dadurch gekennzeichnet ist, daß die
 35 festgelegte Vergleichsspannung eine geringe negative Spannung ist.
6. Eine Schutzschaltung nach einem der oben genannten Ansprüche, die dadurch gekennzeichnet ist, daß sie weiterhin folgendes umfaßt:
 ein Mittel (A) zur Verstärkung der Signalspannung über das magnetoresistive Element, das als Funktion
 40 eines vom magnetoresistiven Element aufgenommenen Magnetflusses erzeugt wird und eine zweite gekoppelte Rückkopplungsschaltung umfaßt, um einen Teil der über das magnetoresistive Element aufgenommenen Spannung zurückzukoppeln, so daß die aufgrund des Vorspannungsstroms entstandene Gleichstromspannung unterdrückt werden kann und nur die Signalspannung übrigbleibt.
- 45 7. Eine Schutzschaltung nach Anspruch 6, die dadurch gekennzeichnet ist, daß die zweite Rückkopplungsschaltung folgendes umfaßt:
 eine Eingangsschaltung mit mindestens zwei Transistoren (Q_{17} , Q_{18}), die als Differentialpaar gekoppelt sind, wobei das magnetoresistive Element zwischen den Basen der Transistoren gekoppelt ist,
 ein Vergleichswiderstand (R_e), der zwischen den Emittern der Transistoren angeschlossen ist, und
 50 eine Transkonduktanzstufe (G_o), die zwischen den Kollektoren der Transistoren gekoppelt ist, wobei die Transkonduktanzstufe einen Ausgang hat, der mit den Transistoren gekoppelt ist, um einen Rückkopplungsstrom zu liefern, so daß der Gleichstrom durch jeden Transistor gleich gehalten werden kann und nur die Signalspannung, die aufgrund des vom magnetoresistiven Element aufgenommenen Magnetflusses entstanden ist, mit einem Ausgangsanschluß gekoppelt wird.

55



Revendications

1. Un circuit de protection pour un élément magnétorésistant (Rh) présentant une première borne et une seconde borne, comprenant:
 - 5 - une première source de Courant raccordée à ladite première borne dudit élément magnétorésistif pour produire un courant de polarisation (J1) au travers dudit élément magnétorésistif et
 - une seconde source de courant raccordée à ladite seconde borne dudit élément magnétorésistif pour produire un courant de référence (Iref),
 - 10 - des moyens à circuits (R) Connectés auxdites première et seconde bornes dudit élément magnétorésistif, caractérisé en ce que les moyens à circuits détectent le potentiel central dudit élément magnétorésistif à une position pratiquement à mi-chemin entre ladite première borne et ladite seconde borne,
 - 15 - et des moyens à circuits de réaction (B) sensibles au potentiel central détecté dudit élément magnétorésistif pour ajuster la sortie de courant (J1) de ladite première source de courant afin de maintenir ledit potentiel central à une tension de référence prédéterminée (Vcentre).
2. Un circuit de protection tel que revendiqué par la revendication 1, caractérisé en ce que lesdits moyens à circuits comprennent:
 - 20 - deux résistances égales (R) connectées en série audit élément magnétorésistif et
 - des moyens pour détecter le potentiel central dudit élément magnétorésistif à la jonction entre les deux résistances.
3. Un circuit de protection tel que revendiqué par l'une quelconque des revendications précédentes, caractérisé en ce que lesdits moyens à circuits de réaction comprennent:
 - 25 - un amplificateur différentiel (B) présentant deux bornes d'entrée et une borne de sortie,
 - des moyens connectant ledit potentiel central détecté à l'une desdites bornes d'entrée,
 - des moyens connectant ladite tension de référence prédéterminée à l'autre desdites bornes d'entrée, et
 - 30 - des moyens raccordant la sortie dudit amplificateur pour contrôler la sortie du courant de ladite première source de courant.
4. Un circuit de protection tel que revendiqué par l'une quelconque des revendications précédentes, caractérisé en ce que ladite tension de référence prédéterminée est le potentiel de masse.
5. Un circuit de protection tel que revendiqué par l'une quelconque des revendications 1, 2 ou 3, caractérisé en ce que ladite tension de référence prédéterminée est une faible tension négative.
6. Un circuit de protection tel que revendiqué par l'une quelconque des revendications précédentes, caractérisé en ce qu'il comprend en outre:
 - 40 - des moyens (A) pour amplifier la tension du signal audit élément magnétorésistif, produite en fonction d'un flux magnétique détecté par ledit élément magnétorésistif et comprenant un second circuit de réaction connecté pour renvoyer une partie de la tension détectée audit élément magnétorésistif afin de retirer la tension de courant continu créée par ledit courant de polarisation et de ne laisser que ladite tension du signal.
 - 45
7. Un circuit de protection tel que revendiqué par la revendication 6 caractérisé en ce que ledit second circuit de réaction comprend:
 - 50 - un circuit d'entrée comprenant au moins deux transistors (Q17, Q18) connectés en paire différentielle et avec l'élément magnétorésistif connecté entre les bases desdits transistors,
 - une résistance de référence (Re) connectée entre les émetteurs desdits transistors, et
 - un étage de transconductance (Go) raccordé entre les collecteurs desdits transistors, ledit étage de transconductance ayant une sortie raccordée auxdits transistors pour délivrer un courant de réaction afin de maintenir les courants continus dans chacun desdits transistors, égaux, de façon
 - 55 que seule la tension de signal due au flux magnétique détecté par ledit élément magnétorésistif, soit raccordée à une borne de sortie.